Analog to Digital (A/D) conversion Techniques

- Successive Approximation type
- Voltage to time conversion (Ramp type)
- Voltage to frequency conversion (Integrating type).
- Dual slope Integrating type ADC
- Flash type ADC

Digital to Analog (D/A) conversion Techniques

- Binary weighted resistor type D/A converter.
- Ladder type:
  1. R-2R ladder type DAC
  2. Inverted R-2R ladder type DAC.

Considerations of A/D and D/A techniques:

- A/D and D/A converters relate analog quantities to digital quantities and vice-versa through an appropriate code.
- Most commonly used code is binary code, in which a no is represented by

$$N = d_n 2^n + d_{n-1} 2^{n-1} + \dots + d_1 2^1 + d_0 2^0$$

(d_n: MSB, d_0: LSB)

where, co-efficients $d_n, d_{n-1}, \dots d_1, d_0$ can either (0 or 1).

Left most bit ie d_n is the 'MSB' & it has a weight (maximum value) which is twice as large as next most significant bit.

∴ Each binary bit has a weight which is twice the weight of next less significant bit.

- For a n-bit converter,

Range of MSB $= \frac{1}{2} \times$ Range of Converter

Range of LSB $= \frac{1}{2^n} \times$ Range of Converter

Full scale o/p voltage of a n-bit converter is:

$$E_0 = E_R \times (d_{n-1} 2^{-1} + d_{n-2} 2^{-2} + \dots + d_1 2^{-(n-1)} + d_0 2^{-n})$$

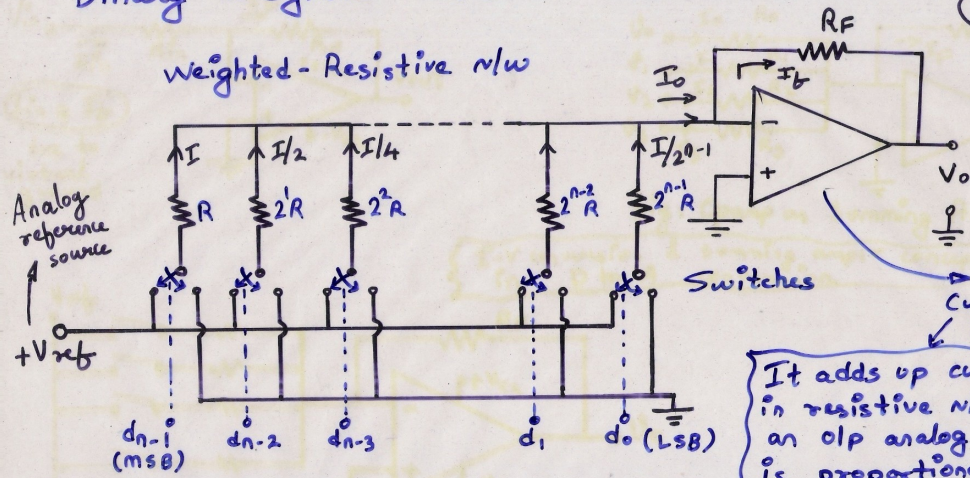
(E_R: Reference voltage)

Resolution = Analog value of LSB $= \frac{\text{Full scale}}{2^n}$

Binary Weighted Resistor D/A Converter:

$$I = \frac{V_{ref}}{R}$$

$$V_0 = -\left(\frac{R_f}{R_{in}}\right) V_{ref}$$



→ Opamp as Current to Voltage Converter.

It adds up currents flowing in resistive n/w to develop an o/p analog voltage which is proportional to digital i/p signal.

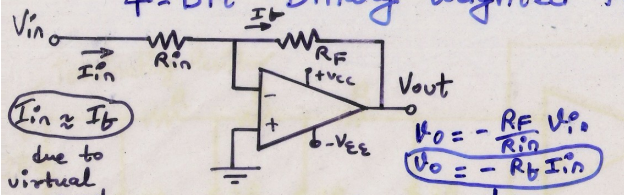
- The resistances in the n/w are weighted ie if resistance for MSB is R, then resistance of next bit is 2R & so on.
- If MSB bit only is '1' by closing the switch, while all other bits as '0' then, $V_0 = V_{ref}/2$.
- If MSB bit (d_{n-1}) and next bit ie (d_{n-2}) are '1', then $V_0 = \left(\frac{1}{2} + \frac{1}{2^2}\right) V_{ref} = 0.75 V_{ref}$
- If only LSB bit (d_0) is '1', o/p vtg $V_0 = V_{ref}/2^n$

$I_0 = (I + I/2 + I/4 + \dots + I/2^{n-1}) = E_R/R \left[1 + \frac{1}{2} + \frac{1}{4} + \dots + \frac{1}{2^{n-1}}\right]$

This is true if all bits are '1'.

General expression: $I_0 = \frac{V_{Ref}}{R}\left[d_{n-1} + \frac{d_{n-2}}{2} + \frac{d_{n-3}}{4} + \dots + \frac{d_1}{2^{n-2}} + \frac{d_0}{2^{n-1}}\right]$

4-bit Binary weighted Resistor D to A Converter.

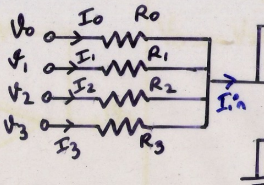


$I_{in} \approx I_f$ due to virtual ground

$V_o = -\frac{R_F}{R_{in}} V_{in}$

$V_o = -R_f I_{in}$

fig: Opamp as Inverting amplr (I-V converter)



$V_o = -I_F R_F$

$I_{in} \approx I_F$

$I_{in} = I_0 + I_1 + I_2 + I_3$

$= \frac{V_0}{R_0} + \frac{V_1}{R_1} + \frac{V_2}{R_2} + \frac{V_3}{R_3}$

fig: Opamp as Summing Amplifier

I-V conversion & summing ampir concepts are used in D to A conversion.

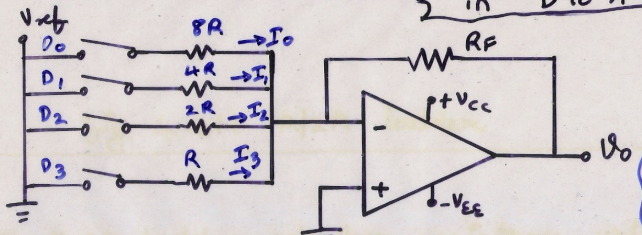


fig: 4-bit Binary weighted D/A converter

- Configuration consists of 4 i/p's having weighted resistances 8R, 4R, 2R & R, corresponding to 4-bit binary i/p's D_0, D_1, D_2, D_3
- Switches are provided for each i/p, so if a s/w is open it means '0' & s/w closed means '1'.
- The '1' or high i/p to binary i/p is obtained from a reference source $+V_{ref}$.

From the diagram, $I_3 = \frac{V_{ref}}{R}$; $I_2 = \frac{V_{ref}}{2R}$; $I_1 = \frac{V_{ref}}{4R}$; $I_0 = \frac{V_{ref}}{8R}$;

$I_{in} = I_0 + I_1 + I_2 + I_3 = \frac{V_{ref}}{R}\left[\frac{1}{8} + \frac{1}{4} + \frac{1}{2} + 1\right] = \frac{V_{ref}}{R}[0.125 + 0.25 + 0.5 + 1] = \frac{V_{ref}}{R}[1.875]$

For a 4-bit D/A converter : $I_{in} = V_{ref}/R\,[D_3 + 2^{-1}D_2 + 2^{-2}D_1 + 2^{-3}D_0]$

Drawback : (Not possible to produce mass weighted resistor DAC)

- Each resistance in n/w has different values ie (R, 2R, 4R, 8R & so on).
- Resistance used for MSB is required to handle a much large current than LSB resistor.

R-2R ladder type D/A Converter

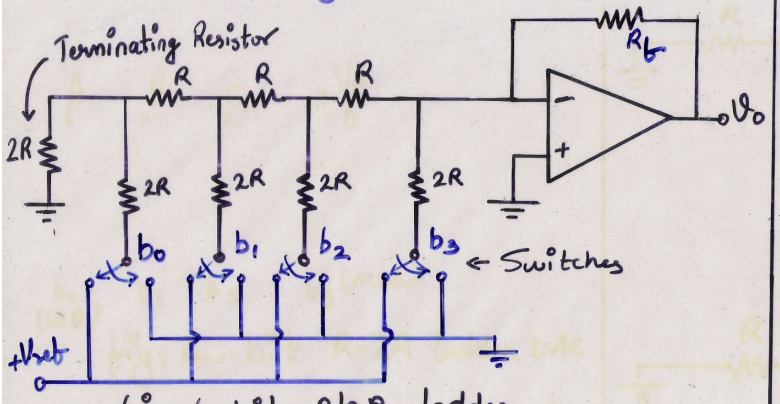


fig: 4-bit R/2R ladder

For n-bit binary i/p, o/p of R-2R ladder is,

$V_o = V_{ref}\,[2^{n-1} b_{n-1} + 2^{n-2} b_{n-2} + \dots + 2b_1 + b_0]$

- In R-2R ladder, only two resistance values are used ie (R and 2R). Hence it is suited for integrated circuit fabrication.
- Here, o/p voltage is a weighted sum of digital binary i/ps.
- Since resistive ladder is a linear n/w, superposition principle can be used for finding total analog voltage for a particular digital i/p.
- Here, o/p voltage is linearly proportional to i/p binary bits and range can be adjusted by changing the reference voltage V_R.

o/p of 4-bit R-2R ladder is

$V_o = -V_{ref}\left[\frac{R_f}{R}\right]\left[\frac{b_3}{2} + \frac{b_2}{4} + \frac{b_1}{8} + \frac{b_0}{16}\right]$

Resolution = $V_{FS}/(2^n - 1)$

n = no of digital inputs

V_{FS} → Value of analog o/p when digital i/p is 1111.

Digital inputs				Analog o/p
b_3	b_2	b_1	b_0	V_o
0	0	0	0	0
0	0	0	1	1/16
0	0	1	0	2/16
0	0	1	1	3/16
0	1	0	0	4/16
0	1	0	1	5/16
0	1	1	0	6/16
0	1	1	1	7/16
1	0	0	0	8/16
1	0	0	1	9/16
1	0	1	0	10/16
1	0	1	1	11/16
1	1	0	0	12/16
1	1	0	1	13/16
1	1	1	0	14/16
1	1	1	1	15/16

R-2R Ladder Exploded

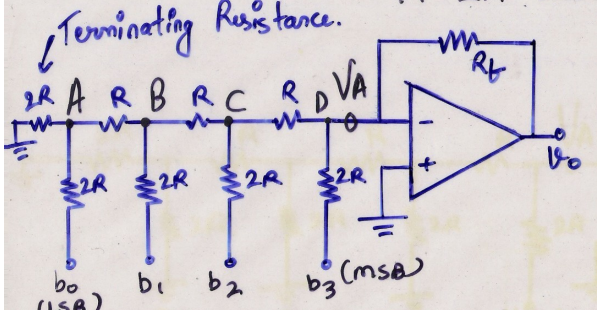
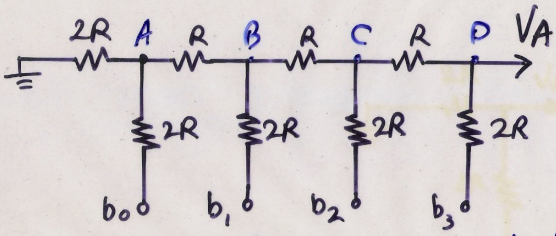


fig: 4-bit R-2R ladder DAC



From this observation, we conclude that resistance looking back from any node towards terminating resistance is 2R.

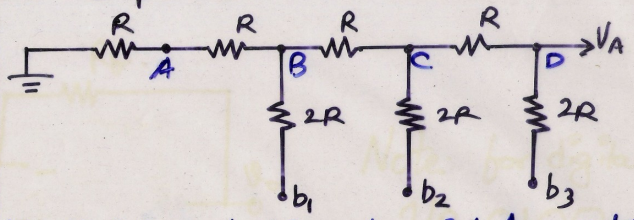


fig: Resistance looking at point A w.r.t ground

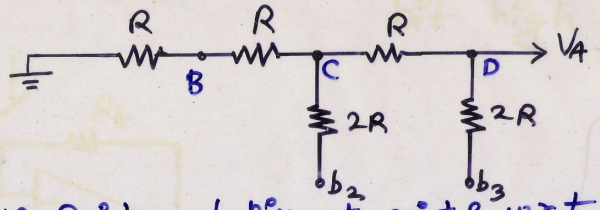


fig: Resistance looking at point B w.r.t ground

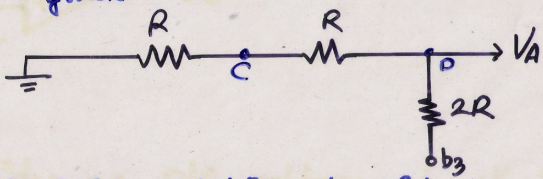
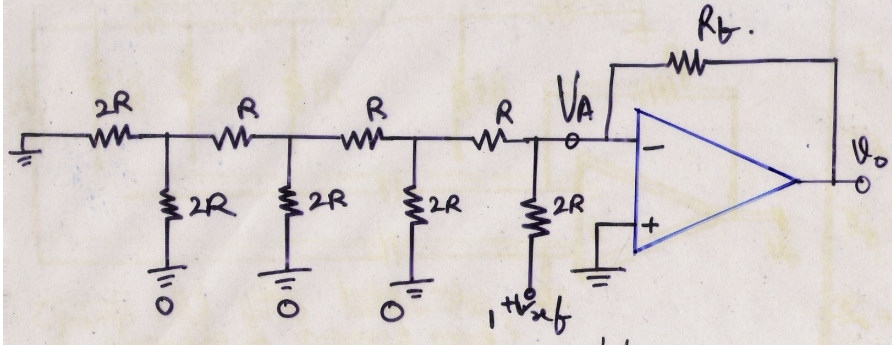


fig: Resistance looking at point C w.r.t ground.

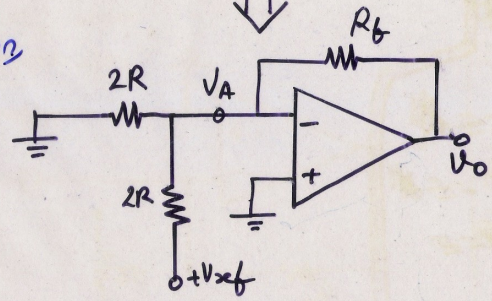
R-2R Ladder Continue.....



Applying Superposition we have

$$V_A = \left(\frac{2R}{2R+2R}\right) V_{ref}$$

$$\boxed{V_A = \frac{V_{ref}}{2}}$$



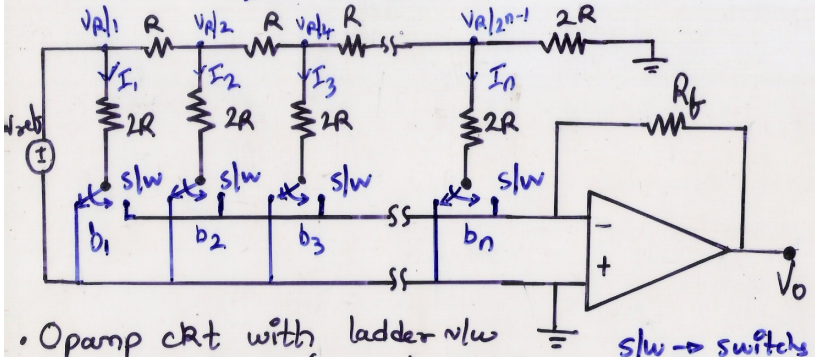
Note: for digital I/P 0100 ie next MSB bit high

$$V_A = \frac{V_{ref}}{4}$$

and so on

Hence a '1' in MSB position provides an O/P voltage of $+V_{ref}/2$

Inverted R-2R Ladder type D/A converter



- Opamp ckt with ladder n/w is operating in 'current mode'

s/w → switch

- In inverted, R-2R ladder type D/A converter, each bit of binary word connects the corresponding switch either to ground or to inverting i/p terminal of opamp which is at virtual ground.
- Since both the positions of switches are at ground potential, current flowing through resistances are constant and it is 'Independent' of switch position.
- All ladder node voltages remains constant with changing i/p bits.

From diagram,

$$I_1 = \frac{V_R}{2R}$$

$$I_2 = \frac{V_R/2}{2R} = \frac{V_R}{4R} = \frac{I_1}{2}$$

$$I_3 = \frac{V_R/4}{2R} = \frac{V_R}{8R} = \frac{I_1}{4}$$

$$I_4 = \frac{V_R/8}{2R} = \frac{V_R}{16R} = \frac{I_1}{8}$$

$$I_n = \frac{V_R/2^{n-1}}{2R} = \frac{I_1}{2^{n-1}}$$

$$V_o = -I_T R_f$$

$$V_o = -R_f [I_1 + I_2 + I_3 + \dots + I_n]$$

$$= -R_f \left[b_1 \cdot \frac{V_R}{2R} + b_2 \cdot \frac{V_R}{4R} + \dots + b_n \frac{V_R}{2^n R} \right]$$

$$V_o = -V_R \left[\frac{R_f}{R}\right] [b_1 2^{-1} + b_2 2^{-2} + \dots + b_n 2^{-n}]$$