Metal oxide Semiconductor Field effect transistor: Basic structure, working of n channel MOSFET Depletion type and study of output and transfer characteristics.

Reference: M.H Rashid, "Microelectronic Circuit Analysis and Circuits", Sedra and Smith, "Microelectronic Circuit Theory and applications".

METAL OXIDE SEMICONDUCTOR FIELD-EFFECT TRANSISTORS

Depletion type MOSFET TOPIC BEGINS:

5.9.6 The Depletion-Type MOSFET

We conclude this section with a brief discussion of another type of MOSFET, the depletion-type MOSFET. Its structure is similar to that of the enhancement-type MOSFET with one important difference: The depletion MOSFET has a physically implanted channel. Thus an n-channel depletion-type MOSFET has an n-type silicon region connecting the n^+ source and the n^+ drain regions at the top of the p-type substrate. Thus if a voltage v_{DS} is applied between drain and source, a current i_D flows for $v_{GS} = 0$. In other words, there is no need to induce a channel, unlike the case of the enhancement MOSFET.

The channel depth and hence its conductivity can be controlled by v_{GS} in exactly the same manner as in the enhancement-type device. Applying a positive v_{GS} enhances the channel by attracting more electrons into it. Here, however, we also can apply a negative v_{GS}, which causes electrons to be repelled from the channel, and thus the channel becomes shallower and its conductivity decreases. The negative v_{GS} is said to **deplete** the channel of its charge carriers, and this mode of operation (negative v_{GS}) is called **depletion mode**. As the magnitude of v_{GS} is increased in the negative direction, a value is reached at which the channel is completely depleted of charge carriers and i_D is reduced to zero even though v_{DS} may be still applied. This negative value of v_{GS} is the threshold voltage of the n-channel depletion-type MOSFET.

The description above suggests (correctly) that a depletion-type MOSFET can be operated in the enhancement mode by applying a positive v_{GS} and in the depletion mode by

applying a negative v_{GS}. This is illustrated in Fig. 5.63, which shows both the circuit symbol for the depletion NMOS transistor (Fig. 5.63a) and its i_D–v_{GS} characteristic. Observe that here the threshold voltage V_t is negative. The i_D–v_{DS} characteristics (not shown) are similar to those for the enhancement-type MOSFET except for the negative V_t. Finally, note that the device symbol denotes the existing channel via the shaded area next to the vertical line.

Depletion-type MOSFETs can be fabricated on the same IC chip as enhancement-type devices, resulting in circuits with improved characteristics, as will be shown in a later chapter.

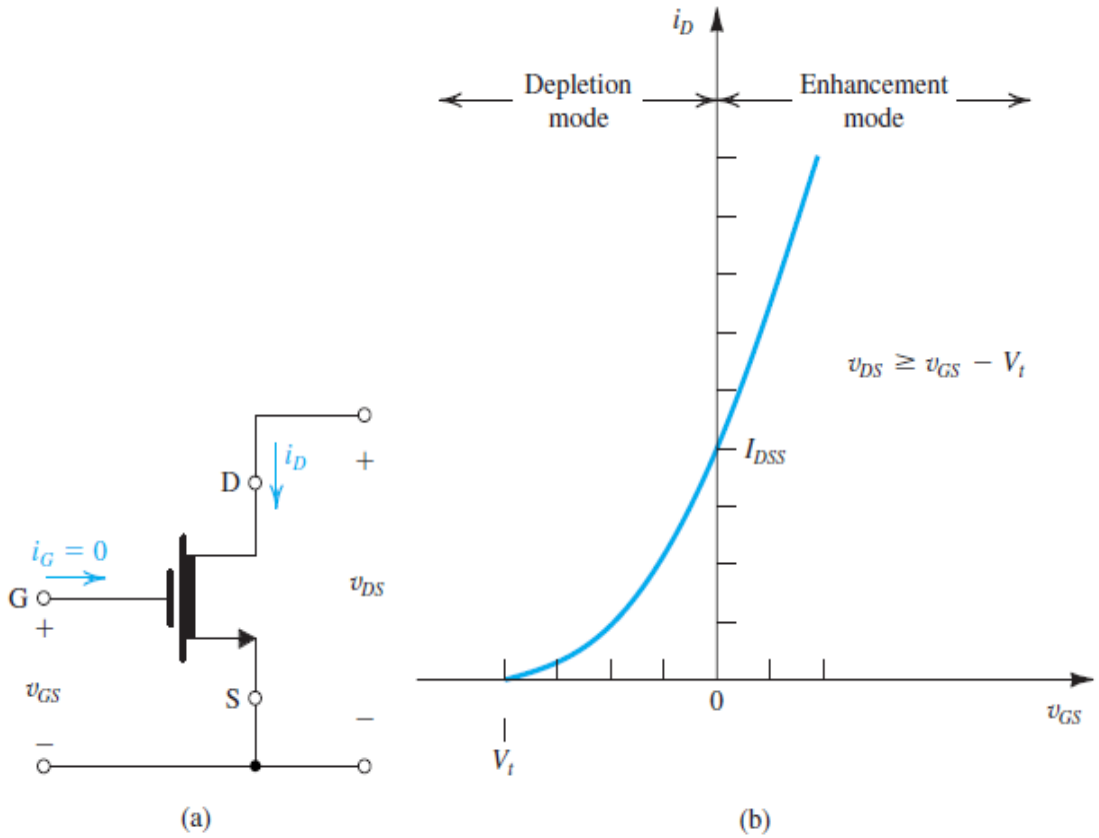

Figure 5.63 The circuit symbol (**a**) and the i_D–v_{GS} characteristic in saturation; (**b**) for an *n*-channel depletion-type MOSFET.

7.4 Depletion MOSFETs

The construction of an *n*-channel depletion MOSFET is very similar to that of an NMOS. An actual channel is formed by adding *n*-type impurity atoms to the *p*-type substrate, as shown in Fig. 7.12(a). The symbol for an *n*-channel depletion MOSFET is shown in Fig. 7.12(b); this symbol is often abbreviated to the one shown in Fig. 7.12(c). Note that the vertical line is bold or darker. An *n*-channel depletion MOSFET is normally operated with a positive voltage between the drain and the source terminals. However, the voltage between the gate and the source terminals can be positive, zero, or negative, whereas in an NMOS v_{GS} is positive.

7.4.1 Operation

The operation of an *n*-channel depletion MOSFET is similar to that of an NMOS. A depletion NMOS is off when its gate-to-source voltage v_{GS} is less than $-V_p$, whereas an NMOS is off when $v_{GS} \leq V_{tN}$. The channel is fully established at $v_{GS} = 0$ for a depletion NMOS and at $v_{GS} = V_{tN}$ for an NMOS. Let us assume that

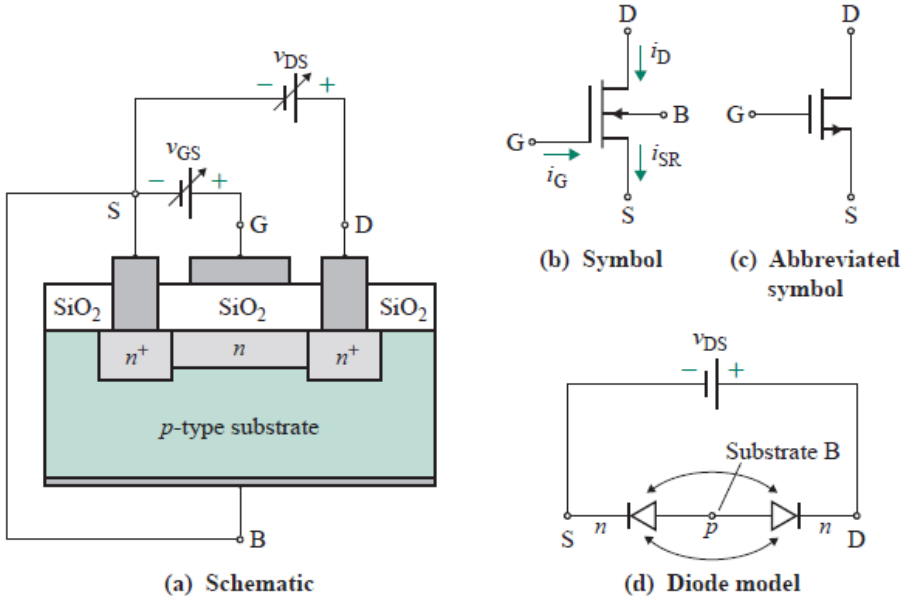

FIGURE 7.12 Schematic and symbols of an *n*-channel depletion MOSFET

the gate-to-source voltage is zero: $v_{GS} = 0$. If v_{DS} is increased from zero to some small value ($\approx$1 V), the drain current follows Ohm's law ($i_D = v_{DS}/r_{DS}$) and is directly proportional to v_{DS}. Any increase in the value of v_{DS} beyond $|V_p|$, known as the *pinch-down voltage*, does not increase the drain current significantly. The region beyond pinch-down is called the *saturation region*. The value of the drain current that occurs at $v_{DS} = |V_p|$ (with $v_{GS} = 0$) is termed the drain-to-source saturation current I_{DSS}. The complete i_D-v_{DS} characteristic for $v_{GS} = 0$ is shown in Fig. 7.13. In practice, there is a very slight increase in drain current i_D as v_{DS} increases beyond $|V_p|$, and the slope of the i_D-v_{DS} characteristic has a finite value. Saturation occurs at the value of v_{DS} at which the gate-to-channel voltage at the drain end equals V_p. That is,

$$v_{GD} = v_{GS} - v_{DS} = V_p \quad \text{or} \quad v_{DS} = v_{GS} - V_p \tag{7.18}$$

If v_{GS} is negative, some of the electrons in the n-channel area will be repelled from the channel and a depletion region will be created below the oxide layer, as shown in Fig. 7.14(a). This depletion region will result in a narrower channel. For $v_{GS} > 0$, a layer of substrate near the n-type channel becomes less p-type and its conductivity is enhanced as shown in Fig. 7.14(b). A positive value of v_{GS} increases the

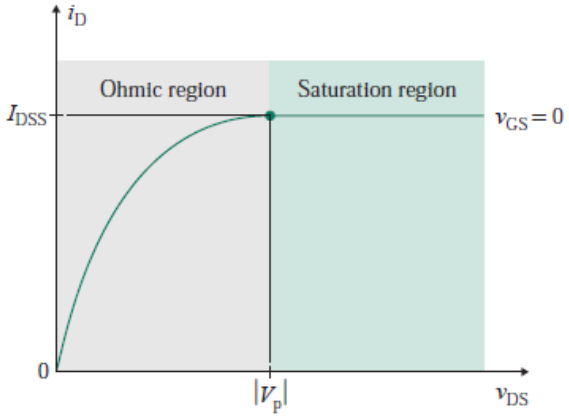

FIGURE 7.13 i_D-v_{DS} characteristic for a constant v_{GS} ($>V_p$)

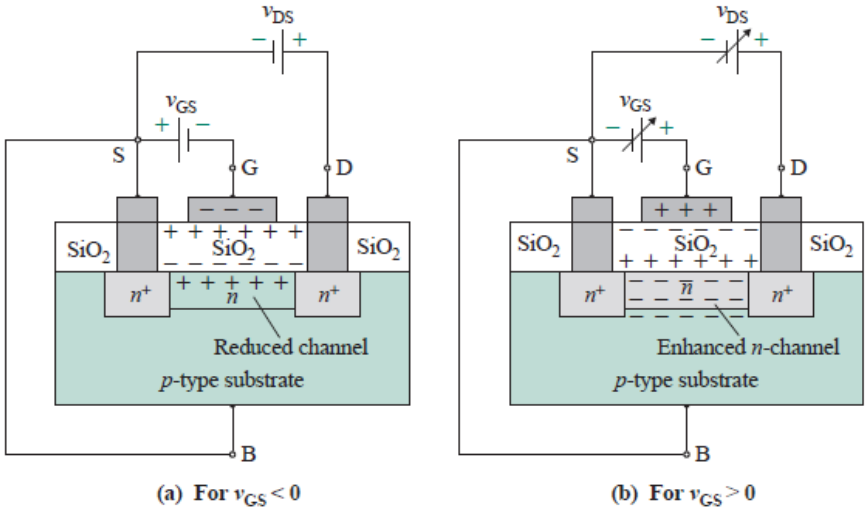

FIGURE 7.14 Channel depletion and enhancement

effective channel width in much the same way as in an NMOS. When the effective channel is increased, the transistor is said to be operating in the enhancement mode. The i_D-v_{DS} characteristics for various values of v_{GS} are shown in Fig. 7.15(a).

7.4.2 Output and Transfer Characteristics

The transfer characteristics are shown in Fig. 7.15(b) for an *n*-channel and a *p*-channel MOSFET. The output characteristics can be divided into three regions: ohmic, saturation, and cutoff.

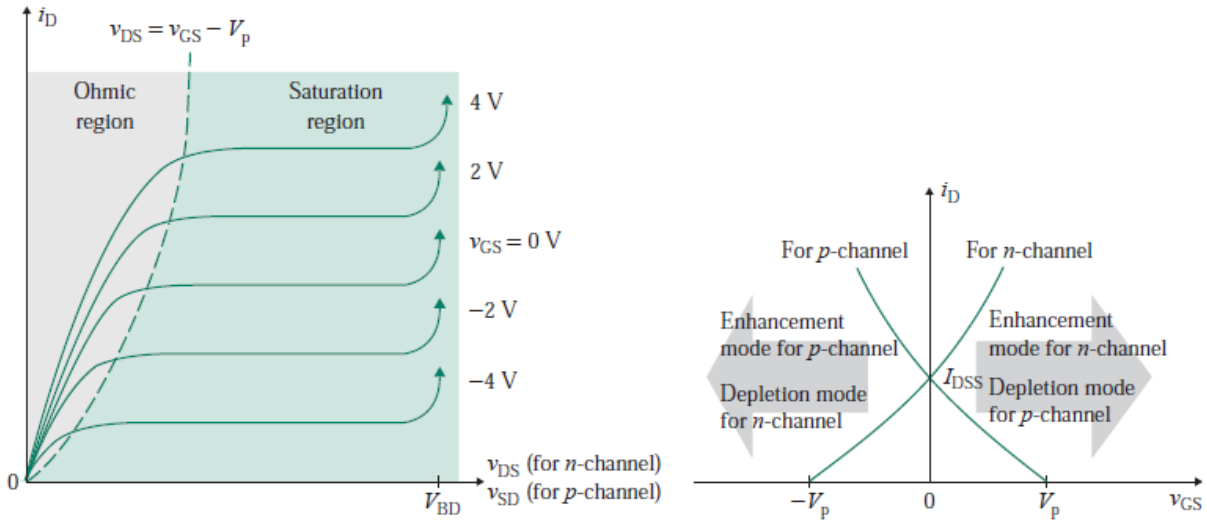

FIGURE 7.15 Drain and transfer characteristics of depletion MOSFETs

Ohmic Region

In the ohmic region, the drain-to-source voltage v_{DS} is low and the channel is not pinched down.

Saturation Region

In the saturation region, $v_{DS} \geq (v_{GS} - V_p)$. The drain-to-source voltage v_{DS} is greater than the pinch-down voltage, and the drain current i_D is almost independent of v_{DS}.

Cutoff Region

In the cutoff region, the gate-to-source voltage is less than the pinch-down voltage. That is, $v_{GS} < V_p$ for the *n*-channel and $v_{GS} > V_p$ for the *p*-channel, and the MOSFET is off. The drain current is zero: $i_D = 0$.

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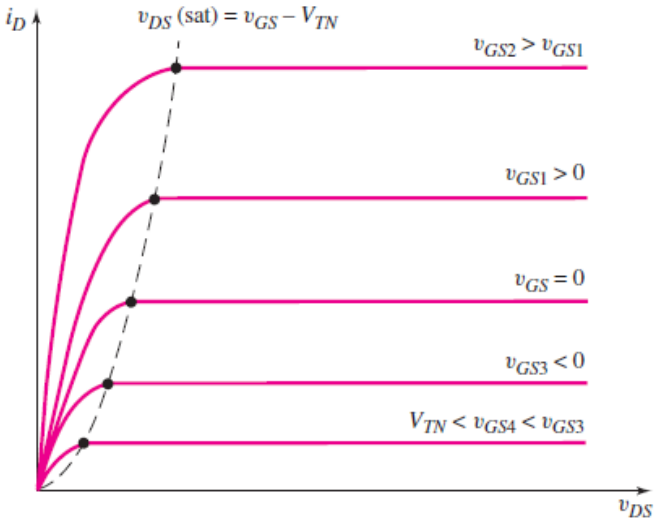

Figure 3.15 Family of i_D versus v_{DS} curves for an n-channel depletion-mode MOSFET. Note again that the v_{DS}(sat) voltage is a single point on each curve.

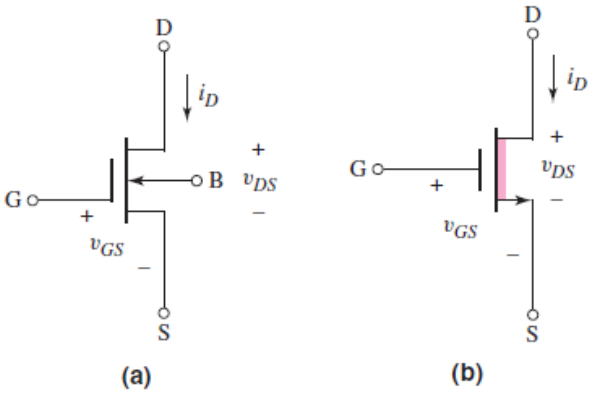

Figure 3.16 The n-channel depletion-mode MOSFET: (a) conventional circuit symbol and (b) simplified circuit symbol