Metal oxide Semiconductor Field effect transistor: Basic structure, types, working of n channel MOSFET Enhancement type and study of output and transfer characteristics.

Reference: Donald A Neamen, "Semiconductor Physics and Devices", Tata McGraw Hill, 4th Edition , M.H Rashid, "Microelectronic Circuit Analysis and Circuits", Boylestad, "Electronic devices and Circuit theory", Sedra and Smith, "Microelectronic Circuit Theory and applications".

METAL OXIDE SEMICONDUCTOR FIELD-EFFECT TRANSISTORS

In this chapter, we introduce a major type of transistor, the metal-oxide-semiconductor field-effect transistor (MOSFET). The MOSFET led to the electronics revolution of the 1970s and 1980s, in which the microprocessor made possible powerful desktop computers, laptop computers, sophisticated handheld calculators, iPods, and a plethora of other electronic systems. The MOSFET can be made very small, so high-density very large scale integration (VLSI) circuits and high-density memories are possible.

Two complementary devices, the n-channel MOSFET (NMOS) and the p-channel MOSFET (PMOS), exist. Each device is equally important and allows a high degree of flexibility in electronic circuit design. The i–v characteristics of these devices are introduced, and the dc analysis and design techniques of MOSFET circuits are developed.

PREVIEW

In this chapter, we will:

- Study and understand the structure, operation, and characteristics of the various types of MOSFETs.

MOSFETs can be made quite small (i.e., requiring a small area on the silicon IC chip), and their manufacturing process is relatively simple (see Appendix A). Also, their operation requires comparatively little power. Furthermore, circuit designers have found ingenious ways to implement digital and analog functions utilizing MOSFETs almost exclusively (i.e., with very few or no resistors). All of these properties have made it possible to pack large numbers of MOSFETs (as many as 2 billion!) on a single IC chip to implement very sophisticated, very-large-scale-integrated (VLSI) digital circuits such as those for memory and microprocessors. Analog circuits such as amplifiers and filters can also be implemented in MOS technology, albeit in smaller, less-dense chips. Also, both analog and digital functions are increasingly being implemented on the same IC chip, in what is known as mixed-signal design.

The objective of this chapter is to develop in the reader a high degree of familiarity with the MOSFET: its physical structure and operation, terminal characteristics, circuit models, and basic circuit applications.

3.1.1 Two-Terminal MOS Structure

The heart of the MOSFET is the metal-oxide-semiconductor capacitor shown in Figure 3.1. The metal may be aluminum or some other type of metal. In most cases, the metal is replaced by a high-conductivity polycrystalline silicon layer deposited on the oxide. However, the term metal is usually still used in referring to MOSFETs. In the figure, the parameter t_{ox} is the thickness of the oxide and ϵ_{ox} is the oxide permittivity.

The physics of the MOS structure can be explained with the aid of a simple parallel-plate capacitor.[1] Figure 3.2(a) shows a parallel-plate capacitor with the top plate at a negative voltage with respect to the bottom plate. An insulator material separates the two plates. With this bias, a negative charge exists on the top plate, a positive charge exists on the bottom plate, and an electric field is induced between the two plates, as shown.

A MOS capacitor with a p-type semiconductor substrate is shown in Figure 3.2(b). The top metal terminal, also called the **gate,** is at a negative voltage with respect to the semiconductor substrate. From the example of the parallel-plate capacitor, we can see that a negative charge will exist on the top metal plate and an electric field will be induced in the direction shown in the figure. If the electric field penetrates the

[1]The capacitance of a parallel plate capacitor, neglecting fringing fields, is $C = \epsilon A/d$, where A is the area of one plate, d is the distance between plates, and ϵ is the permittivity of the medium between the plates.

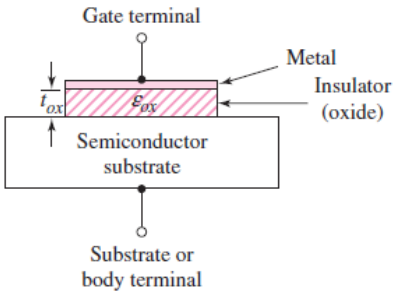

Figure 3.1 The basic MOS capacitor structure

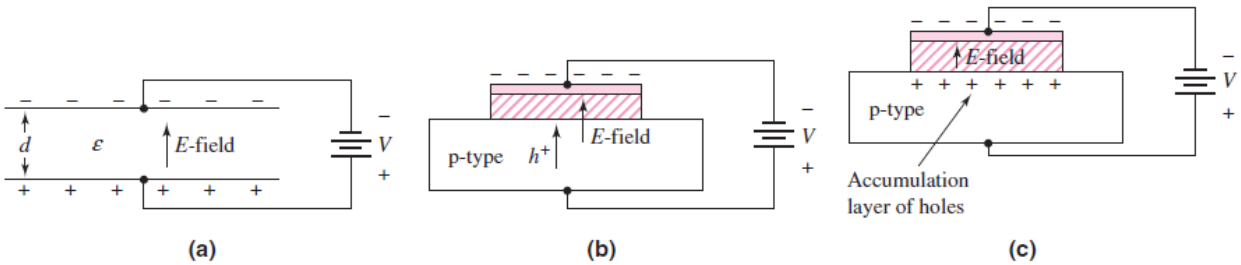

Figure 3.2 (a) A parallel-plate capacitor, showing the electric field and conductor charges, (b) a corresponding MOS capacitor with a negative gate bias, showing the electric field and charge flow, and (c) the MOS capacitor with an accumulation layer of holes

semiconductor, the holes in the p-type semiconductor will experience a force toward the oxide-semiconductor interface. The equilibrium distribution of charge in the MOS capacitor with this particular applied voltage is shown in Figure 3.2(c). An accumulation layer of positively charged holes at the oxide-semiconductor interface corresponds to the positive charge on the bottom "plate" of the MOS capacitor.

Figure 3.3(a) shows the same MOS capacitor, but with the polarity of the applied voltage reversed. A positive charge now exists on the top metal plate and the induced electric field is in the opposite direction, as shown. In this case, if the electric field penetrates the semiconductor, holes in the p-type material will experience a force away from the oxide-semiconductor interface. As the holes are pushed away from the interface, a negative space-charge region is created, because of the fixed acceptor impurity atoms. The negative charge in the induced depletion region corresponds to the negative charge on the bottom "plate" of the MOS capacitor. Figure 3.3(b) shows the equilibrium distribution of charge in the MOS capacitor with this applied voltage.

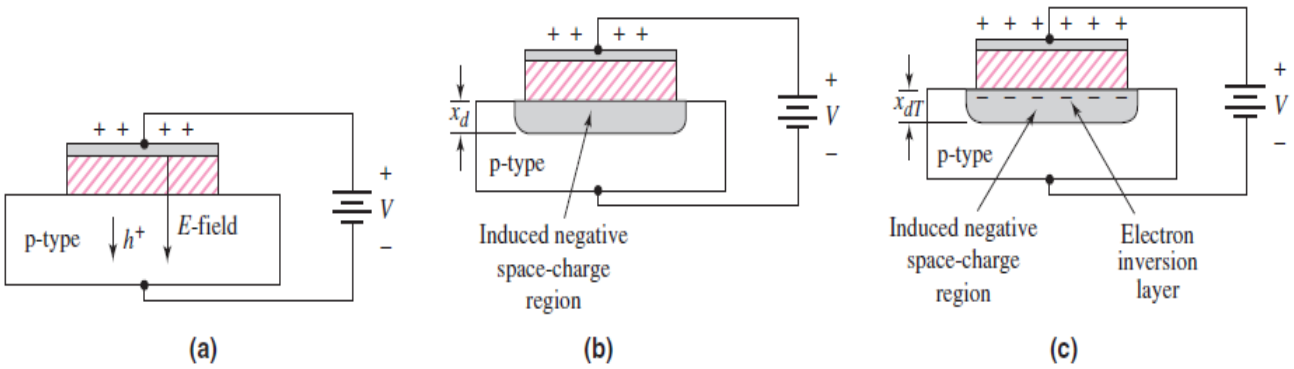

Figure 3.3 The MOS capacitor with p-type substrate: (a) effect of positive gate bias, showing the electric field and charge flow, (b) the MOS capacitor with an induced space-charge region due to a moderate positive gate bias, and (c) the MOS capacitor with an induced space-charge region and electron inversion layer due to a larger positive gate bias

When a larger positive voltage is applied to the gate, the magnitude of the induced electric field increases. Minority carrier electrons are attracted to the oxide-semiconductor interface, as shown in Figure 3.3(c). This region of minority carrier electrons is called an **electron inversion layer.** The magnitude of the charge in the inversion layer is a function of the applied gate voltage.

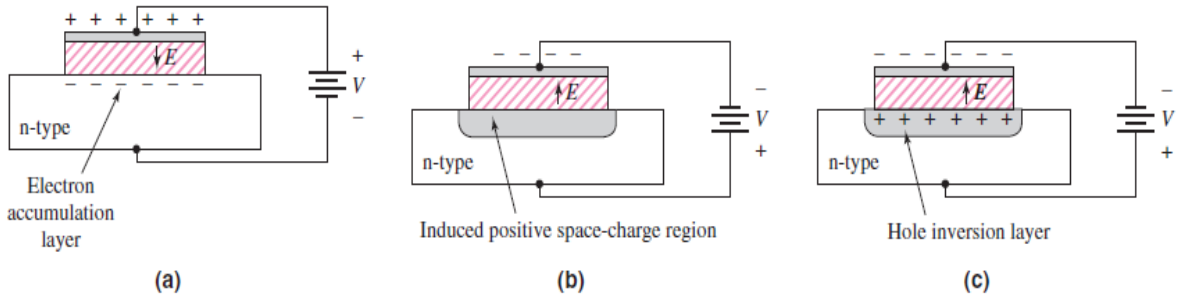

Figure 3.4 The MOS capacitor with n-type substrate: (a) effect of a positive gate bias and the formation of an electron accumulation layer, (b) the MOS capacitor with an induced space-charge region due to a moderate negative gate bias, and (c) the MOS capacitor with an induced space-charge region and hole inversion layer due to a larger negative gate bias

When a larger positive voltage is applied to the gate, the magnitude of the induced electric field increases. Minority carrier electrons are attracted to the oxide-semiconductor interface, as shown in Figure 3.3(c). This region of minority carrier electrons is called an **electron inversion layer.** The magnitude of the charge in the inversion layer is a function of the applied gate voltage.

The same basic charge distributions can be obtained in a MOS capacitor with an n-type semiconductor substrate. Figure 3.4(a) shows this MOS capacitor structure, with a positive voltage applied to the top gate terminal. A positive charge is created on the top gate and an electric field is induced in the direction shown. In this situation, an accumulation layer of electrons is induced in the n-type semiconductor.

Figure 3.4(b) shows the case when a negative voltage is applied to the gate terminal. A positive space-charge region is induced in the n-type substrate by the induced electric field. When a larger negative voltage is applied, a region of positive charge is created at the oxide-semiconductor interface, as shown in Figure 3.4(c). This region of minority carrier holes is called a **hole inversion layer.** The magnitude of the positive charge in the inversion layer is a function of the applied gate voltage.

For the MOS capacitor with a p-type substrate, a positive gate voltage must be applied to create the electron inversion layer; for the MOS capacitor with an n-type substrate, a negative gate voltage must be applied to create the hole inversion layer.

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MOSFET TOPIC BEGINS :

A metal oxide semiconductor field-effect transistor (MOSFET) is a unipolar device. The current flow in a MOSFET depends on one type of majority carrier (electrons or holes). The output current of MOSFETs is controlled by an electric field that depends on a gate control voltage. There are two types of MOSFETs: enhancement MOSFETs and depletion MOSFETs.

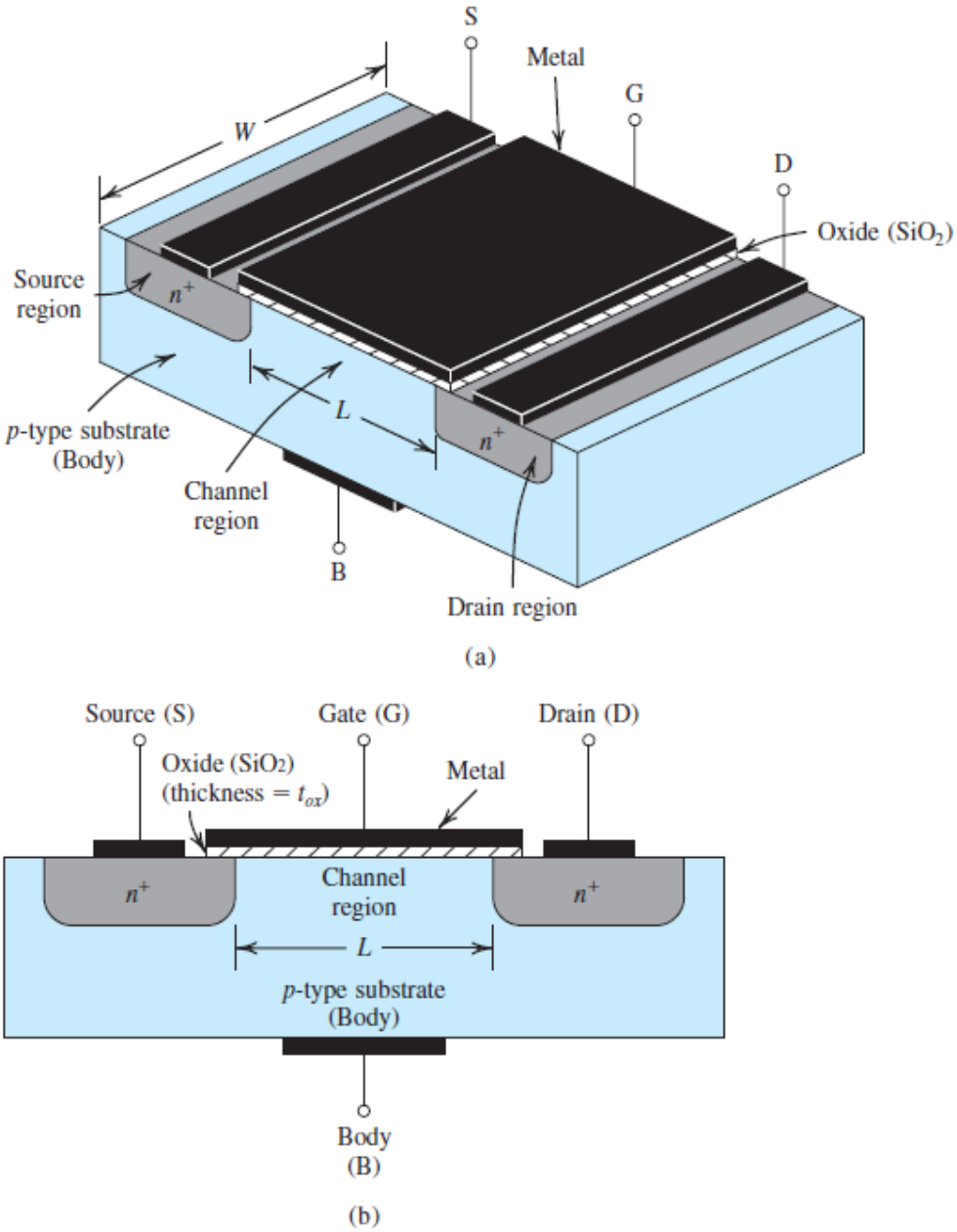

Figure 5.1 Physical structure of the enhancement-type NMOS transistor: **(a)** perspective view; **(b)** cross section.

5.1.1 Device Structure

Figure 5.1, shows the physical structure of the *n*-channel enhancement-type MOSFET. The meaning of the names "enhancement" and "*n*-channel" will become apparent shortly. The transistor is fabricated on a *p*-type substrate, which is a single-crystal silicon wafer that provides physical support for the device (and for the entire circuit in the case of an integrated circuit). Two heavily doped *n*-type regions, indicated in the figure as the n^+ **source**[1] and the n^+ **drain** regions, are created in the substrate. A thin layer of silicon dioxide (SiO_2) of thickness t_{ox} (typically 1 to 10 nm),[2] which is an excellent electrical insulator, is grown on the surface of the substrate, covering the area between the source and drain regions. Metal is deposited on top of the oxide layer to form the **gate electrode** of the device. Metal contacts are also made to the source region, the drain region, and the substrate, also known as the **body**.[3] Thus four terminals are brought out: the gate terminal (G), the source terminal (S), the drain terminal (D), and the substrate or body terminal (B).

Another name for the MOSFET is the **insulated-gate FET** or **IGFET**. This name also arises from the physical structure of the device, emphasizing the fact that the gate electrode is electrically insulated from the device body (by the oxide layer). It is this insulation that causes the current in the gate terminal to be extremely small (of the order of 10^{-15} A).

Observe that the substrate forms *pn* junctions with the source and drain regions. In normal operation these *pn* junctions are kept reverse-biased at all times. Since, as we shall see shortly, the drain will always be at a positive voltage relative to the source, the two *pn* junctions can be effectively cut off by simply connecting the substrate terminal to the source terminal. We shall assume this to be the case in the following description of MOSFET operation. Thus, here, the substrate will be considered as having no effect on device operation, and the MOSFET will be treated as a three-terminal device, with the terminals being the gate (G), the source (S), and the drain (D). It will be shown that a voltage applied to the gate controls current flow between source and drain. This current will flow in the longitudinal direction from drain to source in the region labeled "channel region." Note that this region has a length L and a width W, two important parameters of the MOSFET. Typically, L is in the range of 0.03 μm to 1 μm, and W is in the range of 0.1 μm to 100 μm. Finally, note that the MOSFET is a symmetrical device; thus its source and drain can be interchanged with no change in device characteristics.

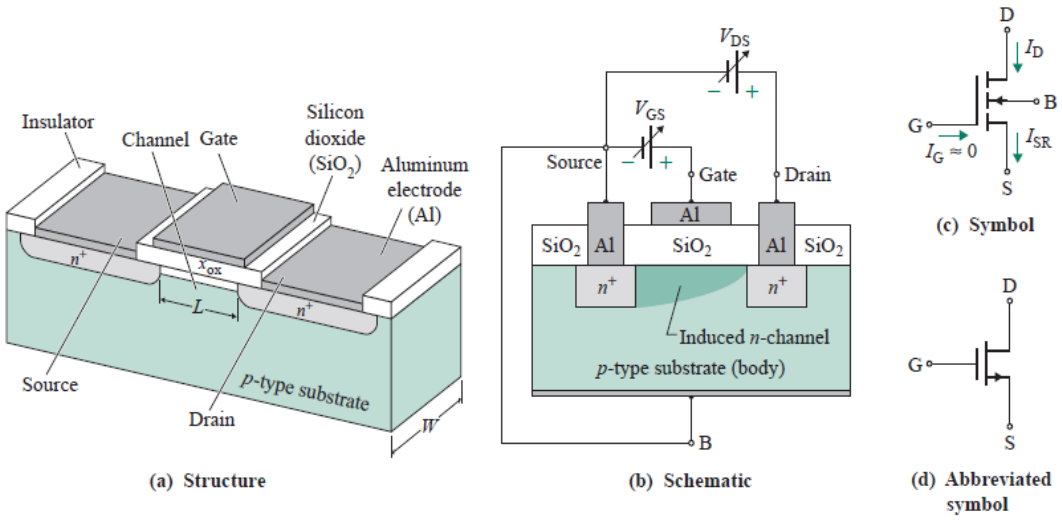

FIGURE Structure and symbols of an *n*-channel enhancement MOSFET

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Basic Transistor Operation

With zero bias applied to the gate, the source and drain terminals are separated by the p-region, as shown in Figure 3.6(a). This is equivalent to two back-to-back diodes, as shown in Figure 3.6(b). The current in this case is essentially zero. If a large enough positive gate voltage is applied, an electron inversion layer is created at the oxide–semiconductor interface and this layer "connects" the n-source to the n-drain,

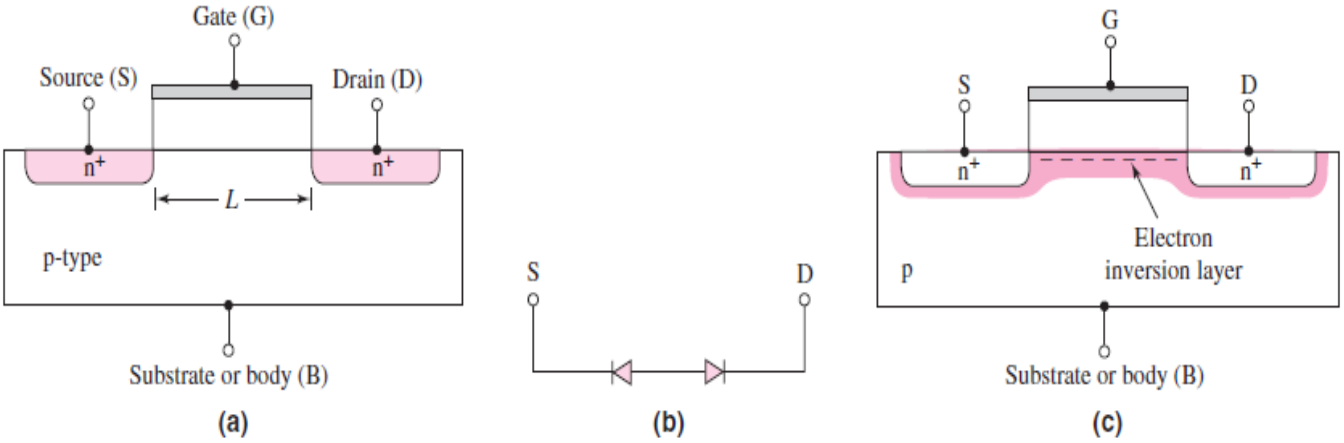

Figure 3.6 (a) Cross section of the n-channel MOSFET prior to the formation of an electron inversion layer, (b) equivalent back-to-back diodes between source and drain when the transistor is in cutoff, and (c) cross section after the formation of an electron inversion layer

as shown in Figure 3.6(c). A current can then be generated between the source and drain terminals. Since a voltage must be applied to the gate to create the inversion charge, this transistor is called an **enhancement-mode MOSFET.** Also, since the carriers in the inversion layer are electrons, this device is also called an **n-channel MOSFET (NMOS).**

The source terminal supplies carriers that flow through the channel, and the drain terminal allows the carriers to drain from the channel. For the n-channel MOSFET, electrons flow from the source to the drain with an applied drain-to-source voltage, which means the conventional current enters the drain and leaves the source. The magnitude of the current is a function of the amount of charge in the inversion layer, which in turn is a function of the applied gate voltage. Since the gate terminal is separated from the channel by an oxide or insulator, there is no gate current. Similarly, since the channel and substrate are separated by a space-charge region, there is essentially no current through the substrate.

N-channel MOSFET Enhancement type WORKING:

Operation

An NMOS is operated with positive gate and drain voltages relative to the source
Their substrates are connected to the source terminal.

An NMOS may be viewed as consisting of two diode junctions that are formed between the substrate and the source and between the substrate and the drain, as shown in Fig. 7.4(a). The hypothetical diodes are in series and back to back, as shown in Fig. 7.4(b).

The NMOS can operate in any of the four operating regions:

cutoff region, linear ohmic, nonlinear ohmic, and saturation.

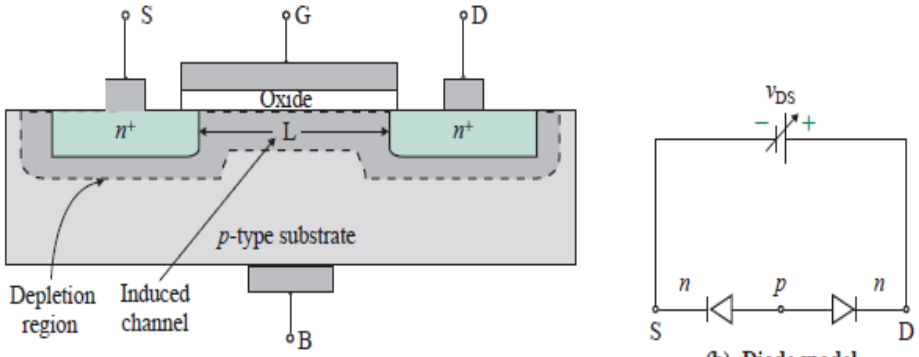

FIGURE 7.4 (a) NMOS schematic (b) Diode model

Operation with Zero Gate Voltage

With zero voltage applied to the gate, two back-to-back diodes exist in series between drain and source. One diode is formed by the *pn* junction between the n^+ drain region and the *p*-type substrate, and the other diode is formed by the *pn* junction between the *p*-type substrate and the n^+ source region. These back-to-back diodes prevent current conduction from drain to source when a voltage v_{DS} is applied. In fact, the path between drain and source has a very high resistance (of the order of 10^{12} Ω).

Creating a Channel for Current Flow

Consider next the situation depicted in Fig. 5.2. Here we have grounded the source and the drain and applied a positive voltage to the gate. Since the source is grounded, the gate voltage appears in effect between gate and source and thus is denoted v_{GS}. The positive voltage on the gate causes, in the first instance, the free holes (which are positively charged) to be repelled from the region of the substrate under the gate (the channel region). These holes are pushed downward into the substrate, leaving behind a carrier-depletion region. The depletion region is populated by the bound negative charge associated with the acceptor atoms. These charges are "uncovered" because the neutralizing holes have been pushed downward into the substrate.

As well, the positive gate voltage attracts electrons (i.e minority carriers) from the ptype substrate. When a sufficient number of electrons accumulate near the surface of the substrate under the gate, an *n* region is in effect created, connecting the source and drain regions, as indicated in Fig. 5.2. Now if a voltage is applied between drain and source, current flows through this induced *n* region, carried by the mobile electrons. The *induced n* region thus forms a **channel** for current flow from drain to source and *is aptly called so*. Correspondingly, the MOSFET of Fig. 5.2 is called an ***n*-channel MOSFET** or, alternatively, an **NMOS transistor**. Note that an *n*-channel MOSFET is

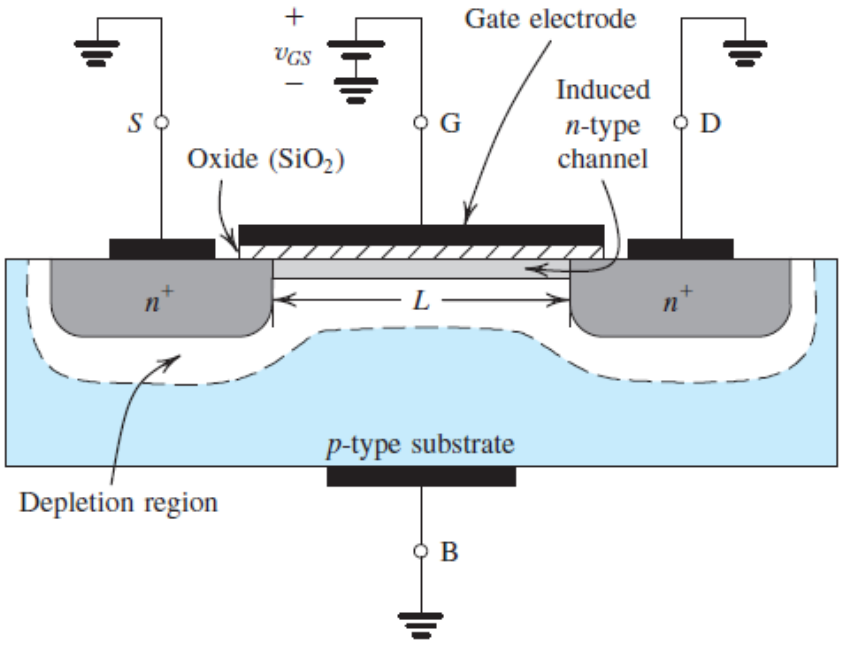

Figure 5.2 The enhancement-type NMOS transistor with a positive voltage applied to the gate. An *n* channel is induced at the top of the substrate beneath the gate.

formed in a *p*-type substrate: The channel is created by *inverting* the substrate surface from *p* type to *n* type. Hence the induced channel is also called an **inversion layer**.

Threshold voltage (Vt or Vtn or Vgs(th)) :

The **threshold voltage** of the n-channel MOSFET, denoted as V_{TN}, is defined[2] as the applied gate voltage needed to create an inversion charge in which the density is equal to the concentration of majority carriers in the semiconductor substrate. In simple terms, we can think of the threshold voltage as the gate voltage required to "turn on" the transistor.

The value of v_{GS} at which a sufficient number of mobile electrons accumulate in the channel region to form a conducting channel is called the **threshold voltage**

For the n-channel enhancement-mode MOSFET, the threshold voltage is positive because a positive gate voltage is required to create the inversion charge.

Why the name FET ?

The gate and the channel region of the MOSFET form a parallel-plate capacitor, with the oxide layer acting as the capacitor dielectric. The positive gate voltage causes positive charge to accumulate on the top plate of the capacitor (the gate electrode). The corresponding negative charge on the bottom plate is formed by the electrons in the induced channel. An electric field thus develops in the vertical direction. It is this field that controls the amount of charge in the channel, and thus it determines the channel conductivity and, in turn, the current that will flow through the channel when a voltage v_{DS} is applied. This is the origin of the name "field-effect transistor" (FET).

1. CUT – OFF Region

Cutoff Region :$0 \leq v_{GS} \leq V_t$.

The gate-to-source voltage v_{GS} is greater than zero but less than the threshold voltage V_t the drain current i_D will be approximately zero if the gate-to-source voltage v_{GS} is zero.

If the gate voltage Vgs is less than the threshold voltage, inversion layer is not formed and hence, the drain current in the device is essentially zero. Even when we apply a positive value of Vds, still device does not conduct and current remains zero.

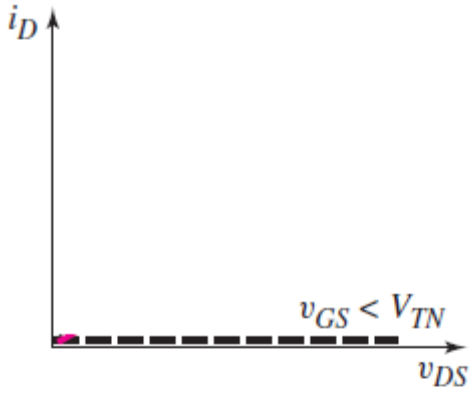

Figure 3.8 Plot of i_D versus v_{DS} characteristic for small values of v_{DS}

Overdrive voltage :

The voltage across this parallel-plate capacitor, that is, the voltage across the oxide, must exceed V_t for a channel to form. When $v_{DS} = 0$, as in Fig. 5.2, the voltage at every point along the channel is zero, and the voltage across the oxide (i.e., between the gate and the points along the channel) is uniform and equal to v_{GS}. The excess of v_{GS} over V_t is termed the **effective voltage** or the **overdrive voltage** and is the quantity that determines the charge in the channel. In this book, we shall denote $(v_{GS} - V_t)$ by v_{OV},

$$v_{GS} - V_t \equiv v_{OV} \tag{5.1}$$

We can express the magnitude of the electron charge in the channel by

$$|Q| = C_{ox}(WL)v_{OV} \tag{5.2}$$

where C_{ox}, called the **oxide capacitance**, is the capacitance of the parallel-plate capacitor per unit gate area (in units of F/m^2), W is the width of the channel, and L is the length of the channel. The oxide capacitance C_{ox} is given by

$$C_{ox} = \frac{\varepsilon_{ox}}{t_{ox}} \tag{5.3}$$

where ε_{ox} is the permittivity of the silicon dioxide,

$$\varepsilon_{ox} = 3.9\varepsilon_0 = 3.9 \times 8.854 \times 10^{-12} = 3.45 \times 10^{-11} \text{ F/m}$$

Finally, note from Eq. (5.2) that as v_{OV} is increased, the magnitude of the channel charge increases proportionately. Sometimes this is depicted as an increase in the depth of the channel; that is, the larger the overdrive voltage, the deeper the channel.

2. LINEAR OHMIC REGION:

Linear Ohmic Region $v_{GS} \geq V_t$ and $0 < v_{DS} << (v_{GS} - V_t)$

A positive value of v_{GS} will establish an electric field, which will attract negative carriers from the substrate and repel positive carriers. As a result, a layer of substrate near the oxide insulator becomes less *p*-type, and its conductivity is reduced. As v_{GS} increases, the surface near the insulator will attract more electrons than holes and will behave like an *n*-type channel. The minimum value of v_{GS} that is required to establish a channel is called the *threshold voltage* V_t. The drain current at $v_{GS} = V_t$ is very small. For $v_{GS} > V_t$, the drain current i_D increases almost linearly with v_{DS} for small values of v_{DS}

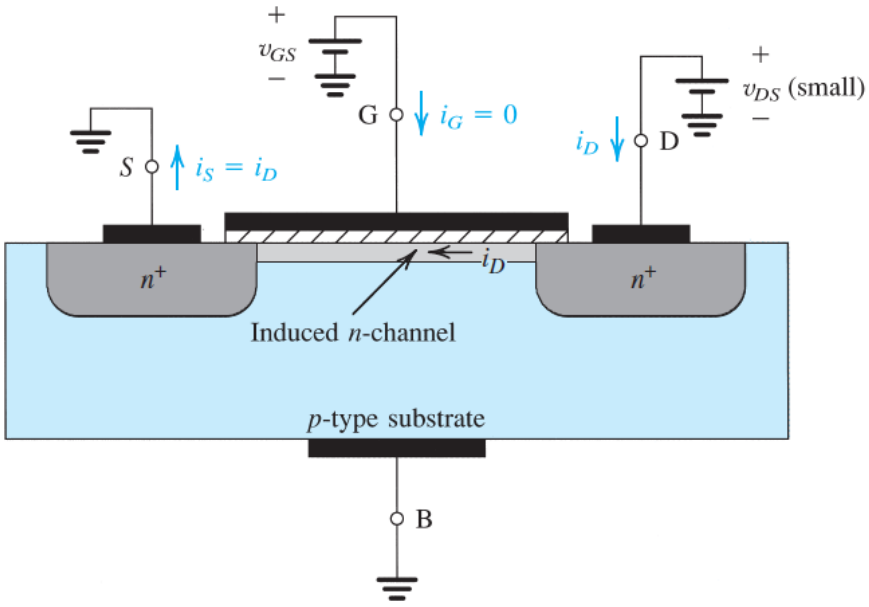

Figure 5.3 An NMOS transistor with $v_{GS} > V_t$ and with a small v_{DS} applied. The device acts as a resistance whose value is determined by v_{GS}. Specifically, the channel conductance is proportional to $v_{GS} - V_t$, and thus i_D is proportional to $(v_{GS} - V_t)v_{DS}$. Note that the depletion region is not shown (for simplicity).

Applying a Small v_{DS}

Having induced a channel, we now apply a positive voltage v_{DS} between drain and source, as shown in Fig. 5.3. We first consider the case where v_{DS} is small (i.e., 50 mV or so). The voltage v_{DS} causes a current i_D to flow through the induced *n* channel. Current is carried by free electrons traveling from source to drain (hence the names source and drain). By convention, the direction of current flow is opposite to that of the flow of negative charge. Thus the current in the channel, i_D, will be from drain to source, as indicated in Fig. 5.3.

Derivation of drain current Id in linear ohmic region:

We now wish to calculate the value of i_D. Toward that end, we first note that because v_{DS} is small, we can continue to assume that the voltage between the gate and various points along the channel remains approximately constant and equal to the value at the source end, v_{GS}. Thus, the effective voltage between the gate and the various points along the channel remains equal to v_{OV}, and the channel charge Q is still given by Eq. (5.2). Of particular interest in calculating the current i_D is the charge per unit channel length, which can be found from Eq. (5.2) as

$$\frac{|Q|}{\text{unit channel length}} = C_{ox} W v_{OV} \tag{5.4}$$

The voltage v_{DS} establishes an electric field E across the length of the channel,

$$|E| = \frac{v_{DS}}{L} \tag{5.5}$$

This electric field in turn causes the channel electrons to drift toward the drain with a velocity given by

$$\text{Electron drift velocity} = \mu_n |E| = \mu_n \frac{v_{DS}}{L} \tag{5.6}$$

where μ_n is the mobility of the electrons at the surface of the channel. It is a physical parameter whose value depends on the fabrication process technology. The value of i_D can now be found by multiplying the charge per unit channel length (Eq. 5.4) by the electron drift velocity (Eq. 5.6),

$$i_D = \left[(\mu_n C_{ox})\left(\frac{W}{L}\right) v_{OV}\right] v_{DS} \tag{5.7}$$

Thus, for small v_{DS}, the channel behaves as a linear resistance whose value is controlled by the overdrive voltage v_{OV}, which in turn is determined by v_{GS}:

$$i_D = \left[(\mu_n C_{ox})\left(\frac{W}{L}\right)(v_{GS} - V_t)\right] v_{DS} \tag{5.8}$$

The conductance g_{DS} of the channel can be found from Eq. (5.7) or (5.8) as

$$g_{DS} = (\mu_n C_{ox})\left(\frac{W}{L}\right) v_{OV} \tag{5.9}$$

or

$$g_{DS} = (\mu_n C_{ox})\left(\frac{W}{L}\right)(v_{GS} - V_t) \tag{5.10}$$

Observe that the conductance is determined by the product of three factors: $(\mu_n C_{ox})$, (W/L), and v_{OV} (or equivalently, $v_{GS} - V_t$).

We conclude this subsection by noting that with v_{DS} kept small, the MOSFET behaves as a linear resistance r_{DS} whose value is controlled by the gate voltage v_{GS}.

$$r_{DS} = \frac{1}{g_{DS}}$$

$$r_{DS} = \frac{1}{(\mu_n C_{ox})(W/L)v_{OV}} \tag{5.13a}$$

$$r_{DS} = \frac{1}{(\mu_n C_{ox})(W/L)(v_{GS} - V_t)} \tag{5.13b}$$

The operation of the MOSFET as a voltage-controlled resistance is further illustrated in Fig. 5.4, which is a sketch of i_D versus v_{DS} for various values of v_{GS}. Observe that the

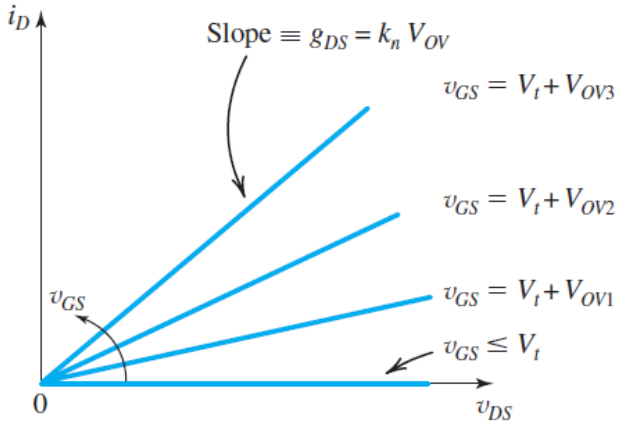

Figure 5.4 The i_D–v_{DS} characteristics of the MOSFET in Fig. 5.3 when the voltage applied between drain and source, v_{DS}, is kept small. The device operates as a linear resistance whose value is controlled by v_{GS}.

resistance is infinite for $v_{GS} \le V_t$ and decreases as v_{GS} is increased above V_t. It is interesting to note that although v_{GS} is used as the parameter for the set of graphs in Fig. 5.4, the graphs in fact depend only on v_{OV} (and, of course, k_n).

The description above indicates that for the MOSFET to conduct, a channel has to be induced. Then, increasing v_{GS} above the threshold voltage V_t enhances the channel, hence the names **enhancement-mode operation** and **enhancement-type MOSFET**. Finally, we note that the current that leaves the source terminal (i_S) is equal to the current that enters the drain terminal (i_D), and the gate current $i_G = 0$.

3. NON-LINEAR OHMIC REGION:

Nonlinear Ohmic Region $v_{GS} \geq V_t$ and $0 < v_{DS} < (v_{GS} - V_t)$.

Increasing v_{DS} does not change the depth of the channel at the source end. However, it increases the drain-to-gate voltage v_{DG} or decreases the gate-to-drain voltage v_{GD}, and the channel width decreases at the drain end. As a result, the channel becomes narrower at the drain end with a tapered shape, as shown in Figure. When v_{DS} becomes sufficiently large and v_{GD} is less than V_t [i.e., when $v_{GD} = (v_{GS} - v_{DS}) \leq V_t$], pinch-down occurs at the drain end of the channel. The i_D-v_{DS} characteristic will be nonlinear. Any further increase in v_{DS} does not cause a large increase in i_D

Lets see how happens ??

Operation as v_{DS} Is Increased

We next consider the situation as v_{DS} is increased. For this purpose, let v_{GS} be held constant at a value greater than V_t; that is, let the MOSFET be operated at a constant overdrive voltage V_{OV}. Refer to Fig. 5.5, and note that v_{DS} appears as a voltage drop across the length of the channel. That is, as we travel along the channel from source to drain, the voltage (measured relative to the source) increases from zero to v_{DS}. Thus the voltage between the gate and points along the channel decreases from $v_{GS} = V_t + V_{OV}$ at the source end to $v_{GD} = v_{GS} - v_{DS} = V_t + V_{OV} - v_{DS}$ at the drain end. Since the channel depth depends on this voltage, and specifically on the amount by which this voltage exceeds V_t, we find that the channel is no longer of uniform depth; rather, the channel will take the tapered shape shown in Fig. 5.5, being deepest at the source end (where the depth is proportional to V_{OV}) and shallowest at the drain end[6] (where the depth is proportional to $V_{OV} - v_{DS}$). This point is further illustrated in Fig. 5.6.

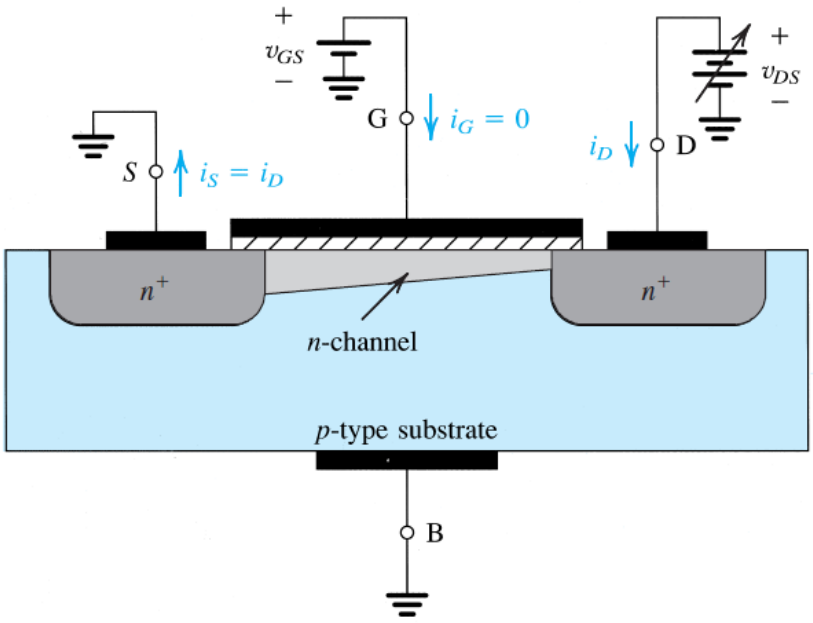

Figure 5.5 Operation of the enhancement NMOS transistor as v_{DS} is increased. The induced channel acquires a tapered shape, and its resistance increases as v_{DS} is increased. Here, v_{GS} is kept constant at a value $> V_t$; $v_{GS} = V_t + V_{OV}$.

4. SATURATION REGION :

Saturation Region $v_{GS} \geq V_t$ and $v_{DS} \geq (v_{GS} - V_t)$ or Operation for $v_{DS} \geq V_{OV}$

The above description of operation assumed that even though the channel became tapered, it still had a finite (nonzero) depth at the drain end. This in turn is achieved by keeping v_{DS} sufficiently small that the voltage between the gate and the drain, v_{GD}, exceeds V_t. This is indeed the situation shown in Fig. 5.6(a). Note that for this situation to obtain, v_{DS} must not exceed V_{OV}, for as $v_{DS} = V_{OV}$, $v_{GD} = V_t$, and the channel depth at the drain end reduces to zero.

Figure 5.8 shows v_{DS} reaching V_{OV} and v_{GD} correspondingly reaching V_t. The zero depth of the channel at the drain end gives rise to the term **channel pinch-off**. Increasing v_{DS} beyond this value (i.e., $v_{DS} > V_{OV}$) has no effect on the channel shape and charge, and the current through the channel remains constant at the value reached for $v_{DS} = V_{OV}$. The drain current thus **saturates** at the value found by substituting $v_{DS} = V_{OV}$ in Eq. (5.14),

$$i_D = \frac{1}{2}k'_n\left(\frac{W}{L}\right)V_{OV}^2 \tag{5.17}$$

The MOSFET is then said to have entered the **saturation region** (or, equivalently, the saturation mode of operation). The voltage v_{DS} at which saturation occurs is denoted V_{DSsat},

$$V_{DSsat} = V_{OV} = V_{GS} - V_t \tag{5.18}$$

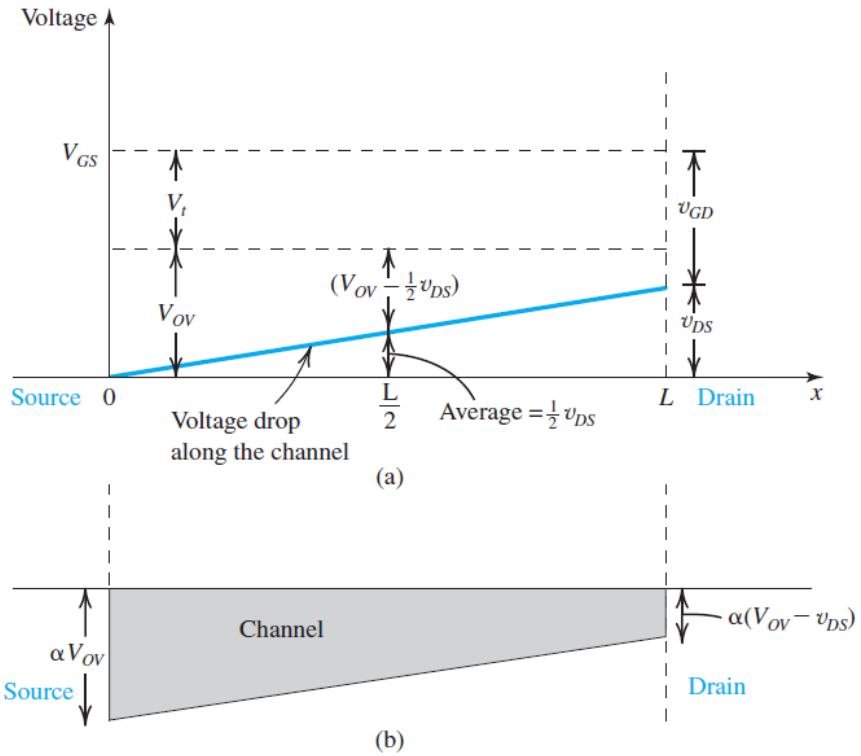

Figure 5.6 (**a**) For a MOSFET with $v_{GS} = V_t + V_{OV}$, application of v_{DS} causes the voltage drop along the channel to vary linearly, with an average value of $\frac{1}{2}v_{DS}$ at the midpoint. Since $v_{GD} > V_t$, the channel still exists at the drain end. (**b**) The channel shape corresponding to the situation in (a). While the depth of the channel at the source end is still proportional to V_{OV}, that at the drain end is proporational to $(V_{OV} - v_{DS})$.

How does current Id will behave, when the channel disappears from the drain end ??

It should be noted that channel pinch-off does *not* mean channel blockage: Current continues to flow through the pinched-off channel, and the electrons that reach the drain end of the channel are accelerated through the depletion region that exists there and into the drain terminal. Any increase in v_{DS} above V_{DSsat} appears as a voltage drop across the depletion region. Thus, both the current through the channel and the voltage drop across it remain constant in saturation.

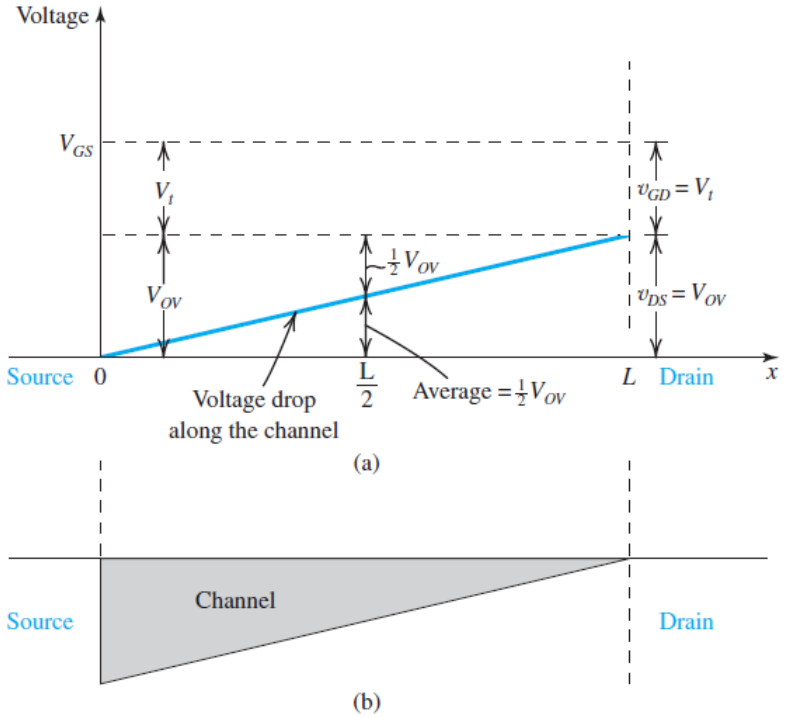

Figure 5.8 Operation of MOSFET with $v_{GS} = V_t + V_{OV}$, as v_{DS} is increased to V_{OV}. At the drain end, v_{GD} decreases to V_t and the channel depth at the drain end reduces to zero (pinch off). At this point, the MOSFET enters the saturation mode of operation. Further increasing v_{DS} (beyond $V_{Dsat} = V_{OV}$) has no effect on the channel shape and i_D remains constant.

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Shape of channel for MOSFET operating in different Operating Modes:

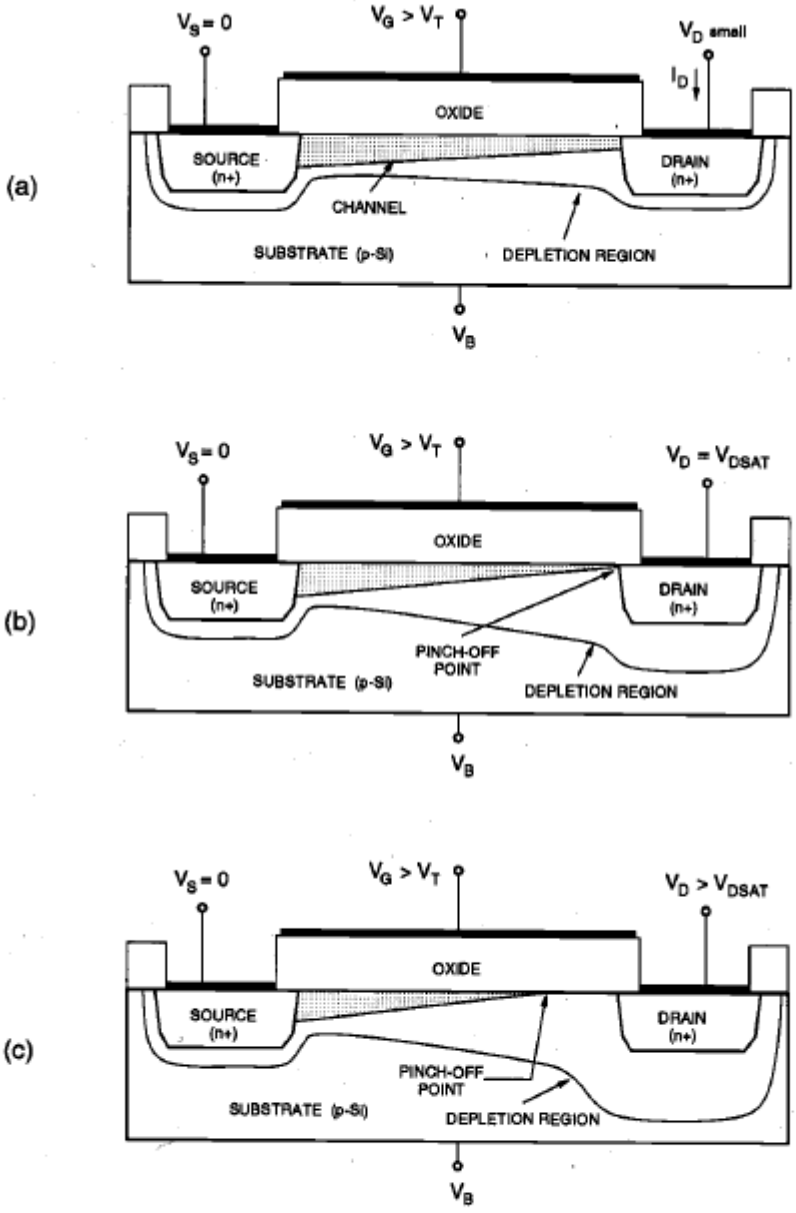

Figure 3.14. Cross-sectional view of an n-channel (nMOS) transistor, (a) operating in the linear region, (b) operating at the edge of saturation, and (c) operating beyond saturation.

Beyond Saturation region i.e $v_{DS} > v_{DS}(\text{sat})$ and $v_{DS}(\text{sat}) = v_{GS} - V_{TN}$

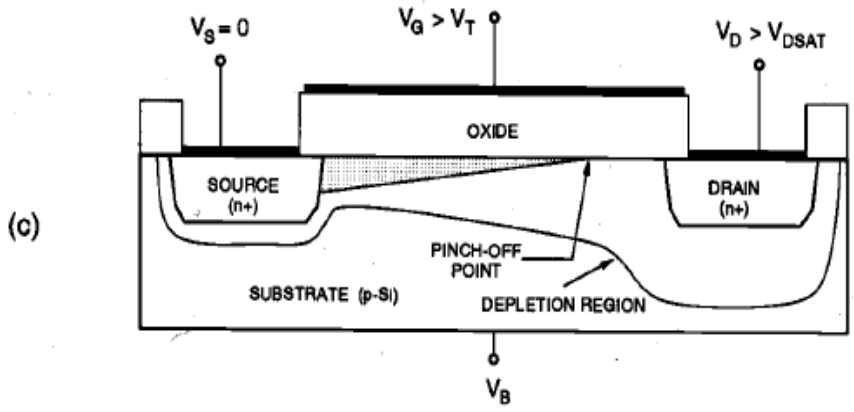

Figure 3.14. Cross-sectional view of an n-channel (nMOS) transistor, (c) operating beyond saturation.

Beyond the pinch-off point, i.e., for $V_{DS} > V_{DSAT}$, a depleted surface region forms adjacent to the drain, and this depletion region grows toward the source with increasing drain voltages. This operation mode of the MOSFET is called the *saturation mode* or the *saturation region*. For a MOSFET operating in the saturation region, the effective channel length is reduced as the inversion layer near the drain vanishes, while the channel-end voltage remains essentially constant and equal to V_{DSAT} (Fig. 3.14(c)). Note that the pinched-off (depleted) section of the channel absorbs most of the excess voltage drop ($V_{DS} - V_{DSAT}$) and a high-field region forms between the channel-end and the drain boundary. Electrons arriving from the source to the channel-end are injected into the drain-depletion region and are accelerated toward the drain in this high electric field, usually reaching the drift velocity limit. The pinch-off event, or the disruption of the continuous channel under high drain bias, characterizes the saturation mode operation of the MOSFET.

Channel Length Modulation (Id slightly increases beyond saturation region) :

once the channel is pinched off at the drain end, further increases in v_{DS} have no effect on the channel's shape. But, in practice, increasing v_{DS} beyond v_{OV} does affect the channel somewhat. Specifically, as v_{DS} is increased, the channel pinch-off point is moved slightly away from the drain, toward the source. This is illustrated in Fig. 5.16, from which we note that the voltage across the channel remains constant at v_{OV}, and the additional voltage applied to the drain appears as a voltage drop across the narrow depletion region between the end of the channel and the drain region. This voltage accelerates the electrons that reach the drain end of the channel and sweeps them across the depletion region into the drain. Note, however, that (with depletion-layer widening) the channel

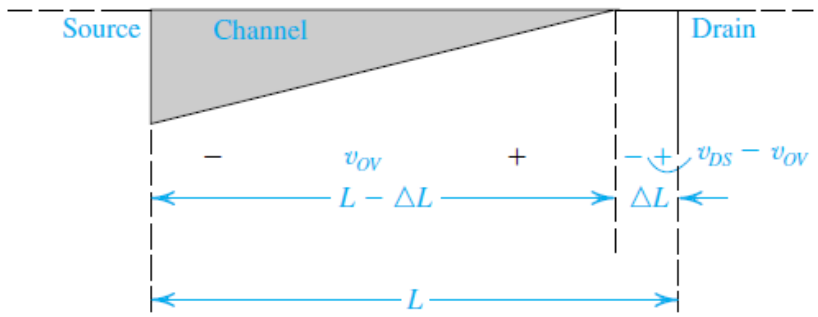

Figure 5.16 Increasing v_{DS} beyond v_{DSsat} causes the channel pinch-off point to move slightly away from the drain, thus reducing the effective channel length (by ΔL).

length is in effect reduced, from L to $L - \Delta L$, a phenomenon known as **channel-length modulation**.

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OUTPUT AND TRANSFER CHARACTERISTICS OF NMOS-E type:

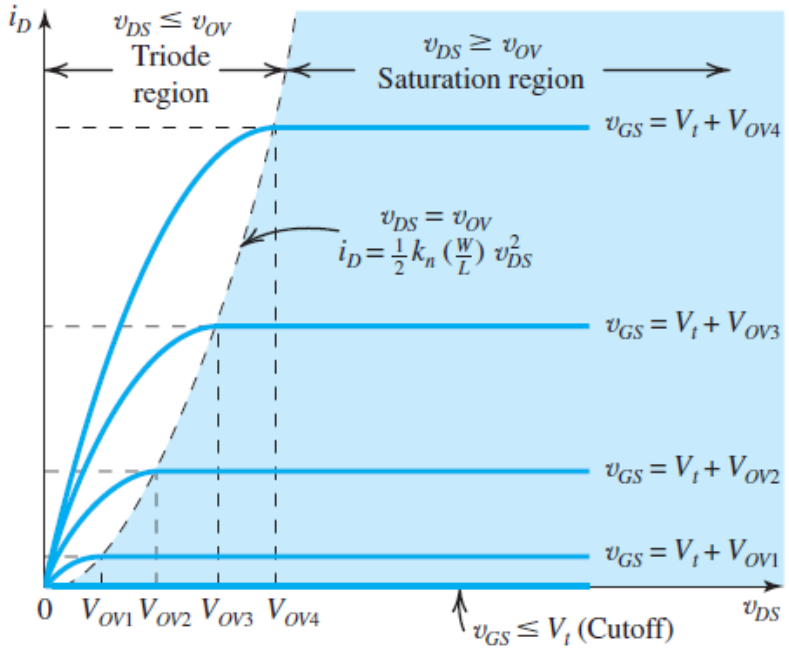

Figure 5.13 The i_D–v_{DS} characteristics for an enhancement-type NMOS transistor.

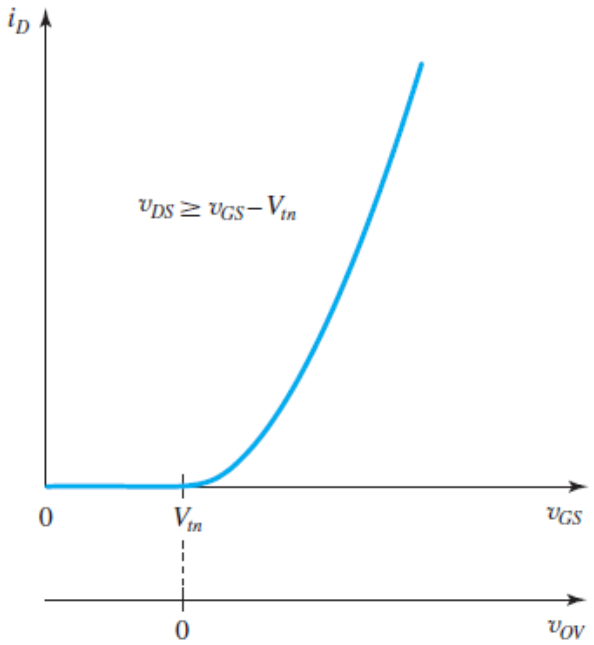

Figure 5.14 The i_D–v_{GS} characteristic of an NMOS transistor operating in the saturation region.

TRANSFER CHARACTERISTICS DERIVED FROM OUTPUT CURVE:

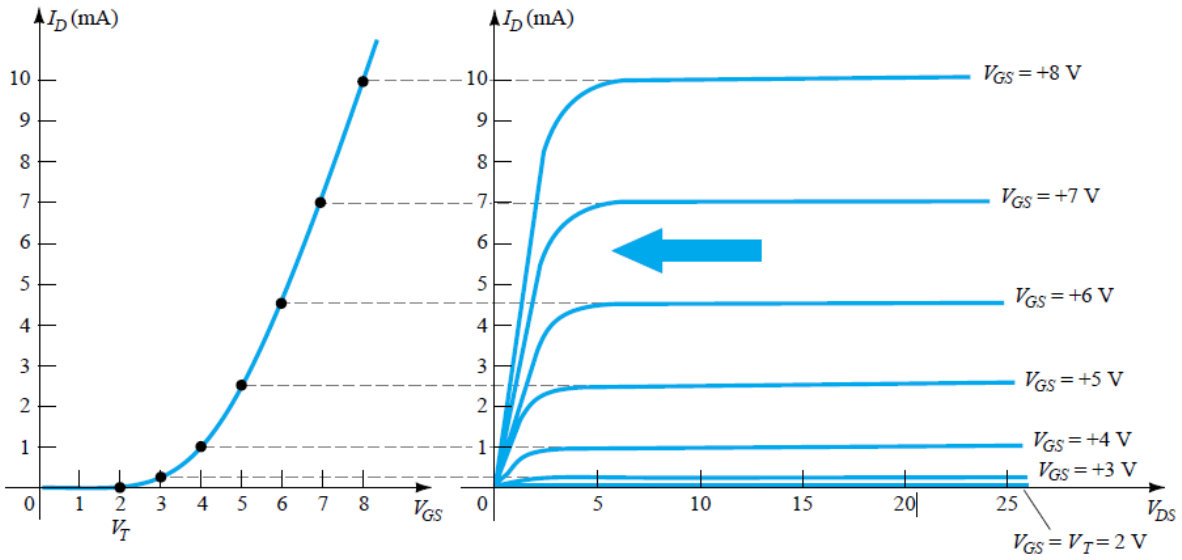

Figure 5.35 Sketching the transfer characteristics for an *n*-channel enhancement-type MOSFET from the drain characteristics.

For values of V_{GS} less than the threshold level, the drain current of an enhancement-type MOSFET is 0 mA.

For levels of $V_{GS} > V_T$, the drain current is related to the applied gate-to-source voltage by the following nonlinear relationship:

$$I_D = k(V_{GS} - V_T)^2$$

Again, it is the squared term that results in the nonlinear (curved) relationship between I_D and V_{GS}. The k term is a constant that is a function of the construction of the device. The value of k can be determined from the following equation [derived from Eq. (5.13)] where $I_{D(on)}$ and $V_{GS(on)}$ are the values for each at a particular point on the characteristics of the device.

$$k = \frac{I_{D(on)}}{(V_{GS(on)} - V_T)^2}$$

NOTE : k here is also denoted as k_n

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I-V equation relations for NMOS - E type :

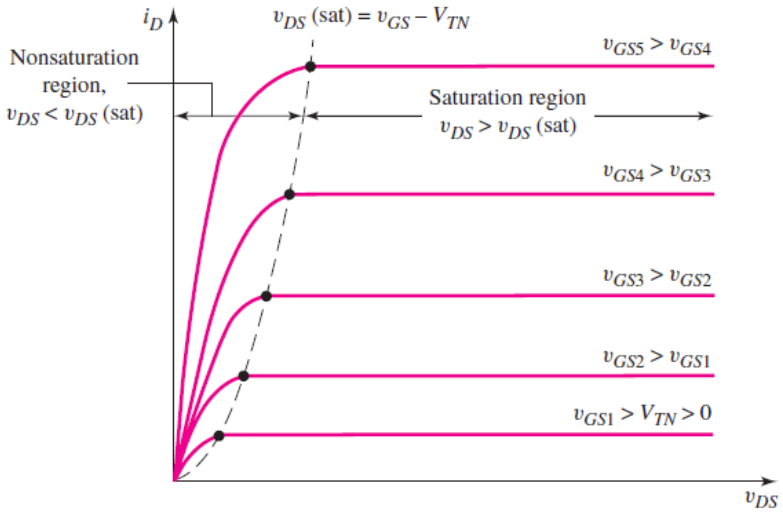

Figure 3.10 Family of i_D versus v_{DS} curves for an n-channel enhancement-mode MOSFET. Note that the v_{DS}(sat) voltage is a single point on each of the curves. This point denotes the transition between the nonsaturation region and the saturation region

The region for which $v_{DS} < v_{DS}$(sat) is known as the **nonsaturation** or **triode region.** The ideal current–voltage characteristics in this region are described by the equation

$$i_D = K_n\left[2(v_{GS} - V_{TN})v_{DS} - v_{DS}^2\right] \qquad \textbf{(3.2(a))}$$

In the saturation region, the ideal current–voltage characteristics for $v_{GS} > V_{TN}$ are described by the equation

$$i_D = K_n(v_{GS} - V_{TN})^2 \qquad \textbf{(3.2(b))}$$

The parameter K_n is sometimes called the transconduction parameter for the n-channel device.

for an n-channel device K_n is given by

$$K_n = \frac{W\mu_n C_{ox}}{2L} \qquad \textbf{(3.3(a))}$$

where C_{ox} is the oxide capacitance per unit area. The capacitance is given by

$$C_{ox} = \epsilon_{ox}/t_{ox}$$

where t_{ox} is the oxide thickness and ϵ_{ox} is the oxide permittivity. For silicon devices, $\epsilon_{ox} = (3.9)(8.85 \times 10^{-14})$ F/cm. The parameter μ_n is the mobility of the electrons in the inversion layer. The channel width W and channel length L

We can rewrite the conduction parameter in the form

$$K_n = \frac{k_n'}{2} \cdot \frac{W}{L} \qquad \textbf{(3.3(b))}$$

where $k_n' = \mu_n C_{ox}$ and is called the **process conduction parameter.** Normally, k_n' is considered to be a constant for a given fabrication technology, so Equation (3.3(b)) indicates that the width-to-length ratio W/L is the transistor design variable.