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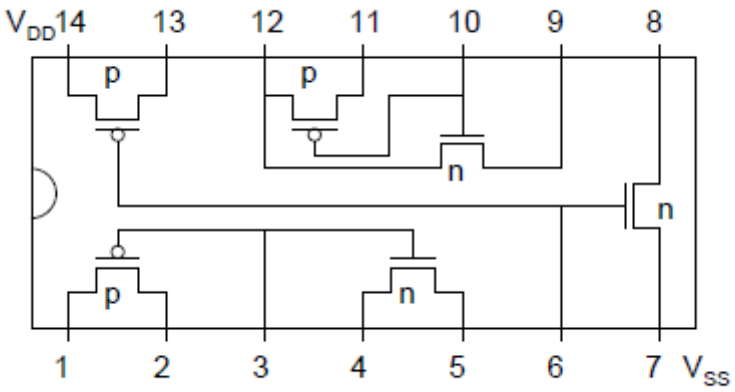
Department of Electronics Engineering

Experiment no: 01

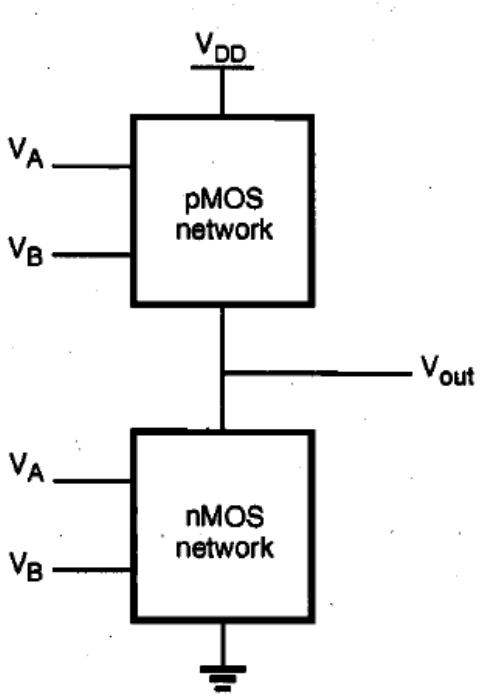
Aim: Implementation and Simulation of universal gates 2- input NAND and NOR using Static CMOS logic.

Apparatus: PC loaded with Microwind software, DSCH3 tool , IC CD 4007, breadboard, multimeter, resistors, LED, power supply (0 – 15 V) , connecting Wires.

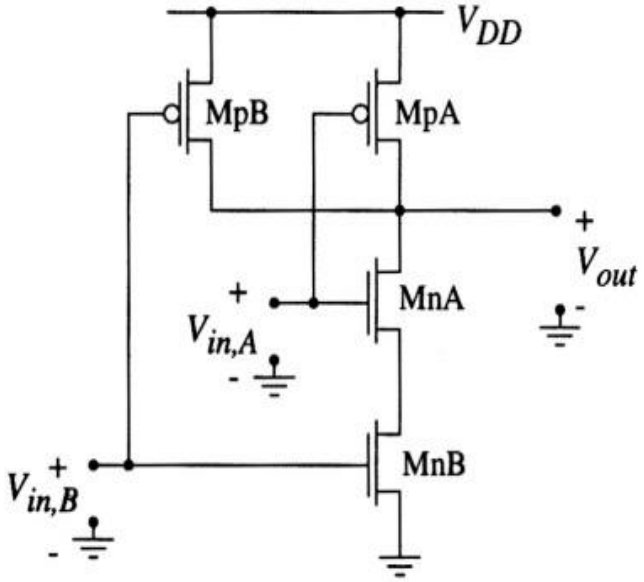
Circuit Diagram: **1) Pinout of IC CD4007**



2) **STATIC CMOS Structure:**



3) Circuit diagram for 2 I/P NAND gate

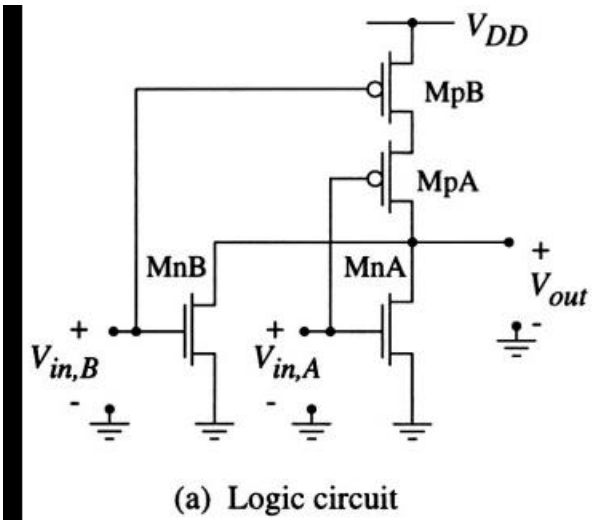


(a) Logic circuit

$V_{in,A}$	$V_{in,B}$	V_{out}
0v	0v	V_{DD}
0v	V_{DD}	V_{DD}
V_{DD}	0v	V_{DD}
V_{DD}	V_{DD}	0v

(b) Operation summary

4) Circuit diagram for 2 I/P NOR gate

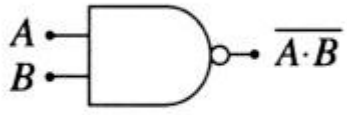


(a) Logic circuit

$V_{in,A}$	$V_{in,B}$	V_{out}
0v	0v	V_{DD}
0v	V_{DD}	0v
V_{DD}	0v	0v
V_{DD}	V_{DD}	0v

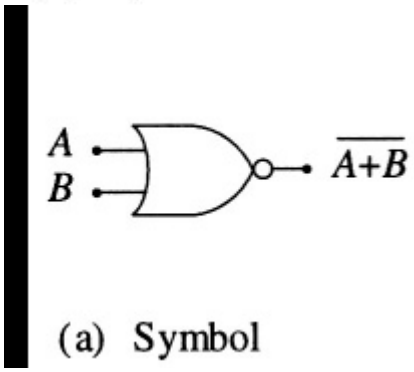
(b) Operation summary

4) Truth table for 2 I/P NAND and NOR gates



A	B	$\overline{A \cdot B}$
0	0	1
0	1	1
1	0	1
1	1	0

(a) Symbol (b) Truth table



A	B	$\overline{A+B}$
0	0	1
0	1	0
1	0	0
1	1	0

(a) Symbol (b) Truth table

Theory: CMOS provides an extremely powerful approach to building complicated digital logic networks in a very efficient manner.
The general structure of a complex logic gate can be created by the following steps.

- Provide a complementary pair (an nFET and a pFET with a common gate) for each input;
- Replace the single nFET with an **array** of nFETs that connects the output to ground;
- Replace the single pFET with an **array** of pFETs that connects the output to VDD.
- Design the nFET and pFET switching network so that only one network acts as a closed switch for any given input combination.

STATIC CMOS NAND Gate :

To construct a CMOS circuit that provides this function we will use two complementary pairs, one for each of the inputs *A* and *B,* and create the nFET and pFET arrays according to the needed outputs. First, note that there is only a single case where the output is a 0. This occurs when both inputs are at logic 1 values. Translating this observation into voltages then says that the output voltage Vout = 0V if and only if both of the two input voltages high, i.e. A = B = VDD, since the NMOS connect the output node to ground, this requires that the two nFETs be connected in series. If either input voltage is low, then Vout = VDD, indicating that the output node must be connected to the power supply. To accommodate these cases, we will wire the two pFETs in parallel. Combining the requirements for the FETs results in the circuit shown in Figure.

The logical operation of the circuit can be verified by working in reverse. Consider the seriesconnected nFETs MnA and MnB. If both A = B = VDD, then these transistors are active and

conduct current while both pFETs are in cutoff. This provides a strong conduction path to ground and gives an output voltage of Vout = 0V. However, if either *A* or *B* is low (either individually or at the same time) then there is no path to ground; in this case, at least one p-channel device is conducting to the power supply, giving a value of Vout = VDD.

STATIC CMOS NOR Gate :

A CMOS NOR2 gate can be built by using two complementary pairs as shown in Figure. Input *A* is connected to MnA and MpA, while *B* controls MnB and MpB. Note that the nFETs are connected in parallel, while the pFETs form a series chain. To understand the operation of the gate, we examine the conduction states of the transistors for different input voltages A & B. If A = VDD then MnA is ON and MpA is OFF; since MnA provides a conducting path from the ground to the output, Vout = 0V. Setting B = VDD, turns MnB ON and MpB OFF and also results in Vout = 0V. And, if both A and B are high, then both nFETs are ON and the output voltage is Vout = 0V. The only input combination that results in Vout = VDD, is when A = B = 0V, since both pFETs are ON while both nFETs are OFF.

Procedure: **Part A: Hardware Implementation**

1. Draw the circuit with pin number and variables.

2. Make the connections as per the circuit diagrams and wire them on Bread board.

3. Verify the truth table for 2 I/P NAND and NOR gates

Part B: Design Simulation

4. Draw the circuit using DSCH3 tool.

5. Apply clock signal for all combinations of inputs A and B.

6. Connect LED's at all observing nodes.

7. Run the simulation and observe the output waveforms.

Conclusion: