Dwarkadas. J. Sanghvi College of Engineering
Department of Electronics Engineering

Experiment no: 05

Aim: Simulation of single ended differential sense amplifier.

Apparatus: PC loaded with LT spice software.

Theory: A **differential amplifier** is a type of electronic amplifier that amplifies the difference between two voltages but does not amplify the particular voltages. The output of an ideal differential amplifier is given by:

$$V_{\text{out}} = A_{\text{d}}(V_{\text{in}}^{+} - V_{\text{in}}^{-})$$

Where V_{in}^{+} and V_{in}^{-} are the input voltages and A_{d} is the differential gain.

Differential amplifiers are often used to null out noise or bias-voltages that appear at both inputs. The signals common to both the inputs are suppressed at the o/p of amplifier by a ratio called as CMRR. Spikes on the power supply are suppressed by PSRR ratio. This differential approach is directly applicable to SRAM memories, as these are the only memory cells that offer a true differential output.

Figure (a) shows the most basic differential sense amplifier. It is a differential voltage amplifier with a current mirror load. The inputs are fed to the differential i/p terminals M1 & M2 and M3 & M4 acts as an active current mirror load.

There is a current sink ISS which is a constant current sink. The current through this would be always constant and hence the Sum of iD1 and iD2 would be always constant i.e. ISS = iD1 + iD2. To keep ISS constant in this circuit, if there is a decrease in one of the branch current the other branch current increases.

When a differential input is applied (bit and bit' lines), let's assume the higher voltage is applied to the transistor M1 gate and the compliment is on the M2 gate. In this case the current through M1, that is iD1 increases and the current iD2 decreases. Since iD1=iD3 the current mirror draws the same current as iD1, which results in a mirrored current iD4 = iD3 = iD1.

Also notice that ISS needs to be constant and hence whenever iD1 decreases iD2 will increase. Thus the voltage difference is transferred in to a current difference and this current is amplified at the output and again this is converted as a voltage at the output. The ISS keeps the current always constant and because of this it brings one of the transistors to higher saturation by drawing more current through that branch when the other branch supplies reduced current.

As shown in fig. (b) When the inputs are same on bit and bit' lines, iD1 = iD2 & differential i/p is zero. For positive diff. i/p iD1 > iD2 & for negative diff. i/p iD2 > iD1.

Circuit Diagram:

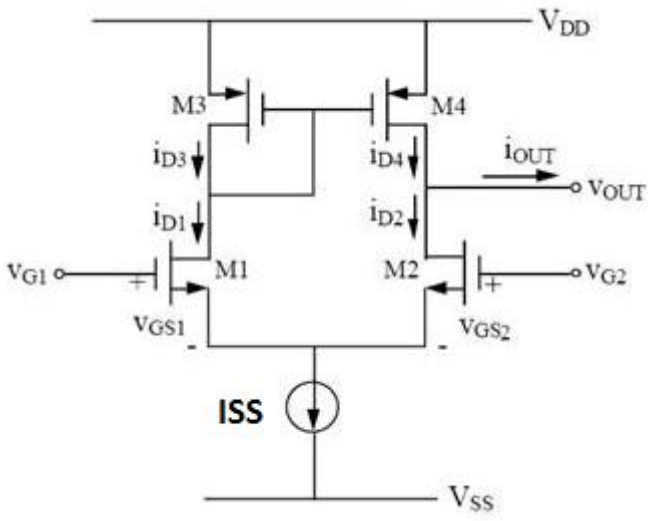

Fig a : single ended differential sense amplifier

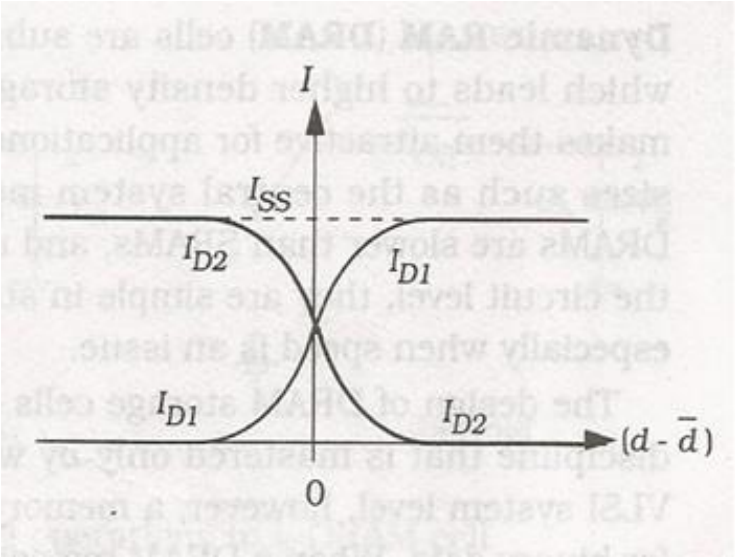

Fig b : Current waveforms

Procedure: **Design Simulation**

1. Draw the circuit using LT spice software.
2. Apply VDD = 12V, ISS = 5mA dc and Vg1 = 1V peak-to-peak / 1KHz and Vg2 = 0V.
3. Run the simulation and observe the output waveforms.

Conclusion:

Attach the printouts of circuit diagram and waveform.