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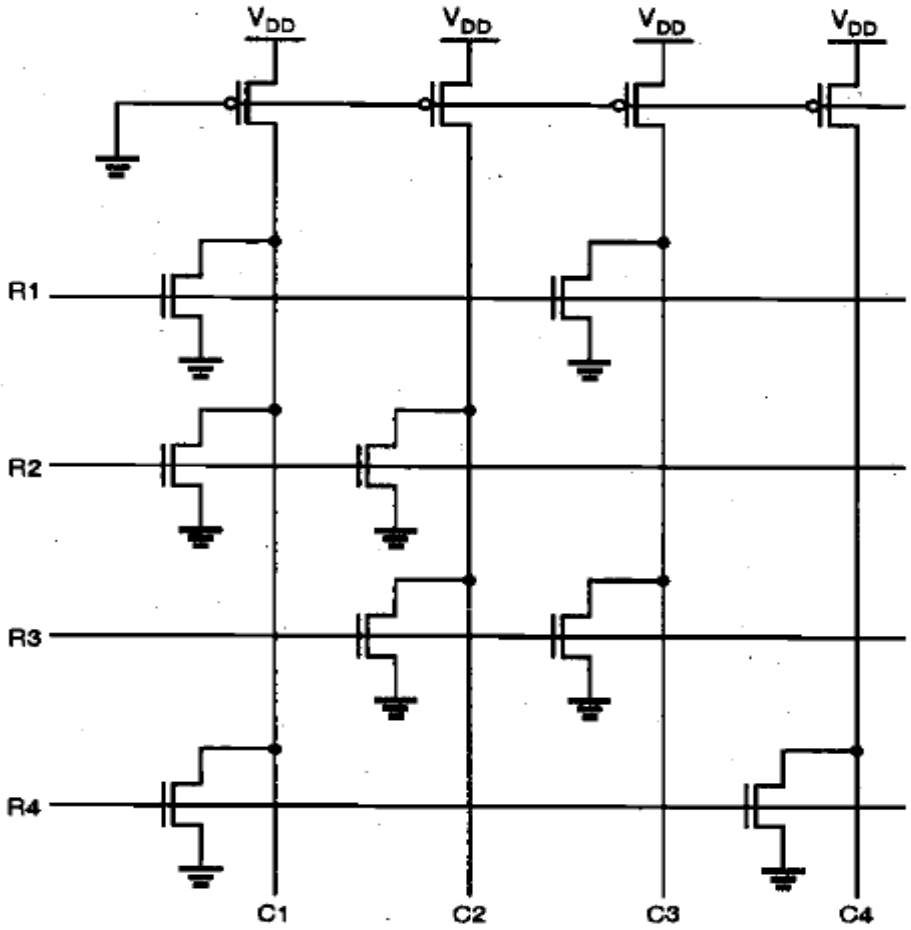
Experiment no: 06

Aim: Simulation of 4x4 NAND ROM and NOR ROM array for given data.

Apparatus: PC loaded with Microwind software, DSCH3 tool.

Circuit Diagram:

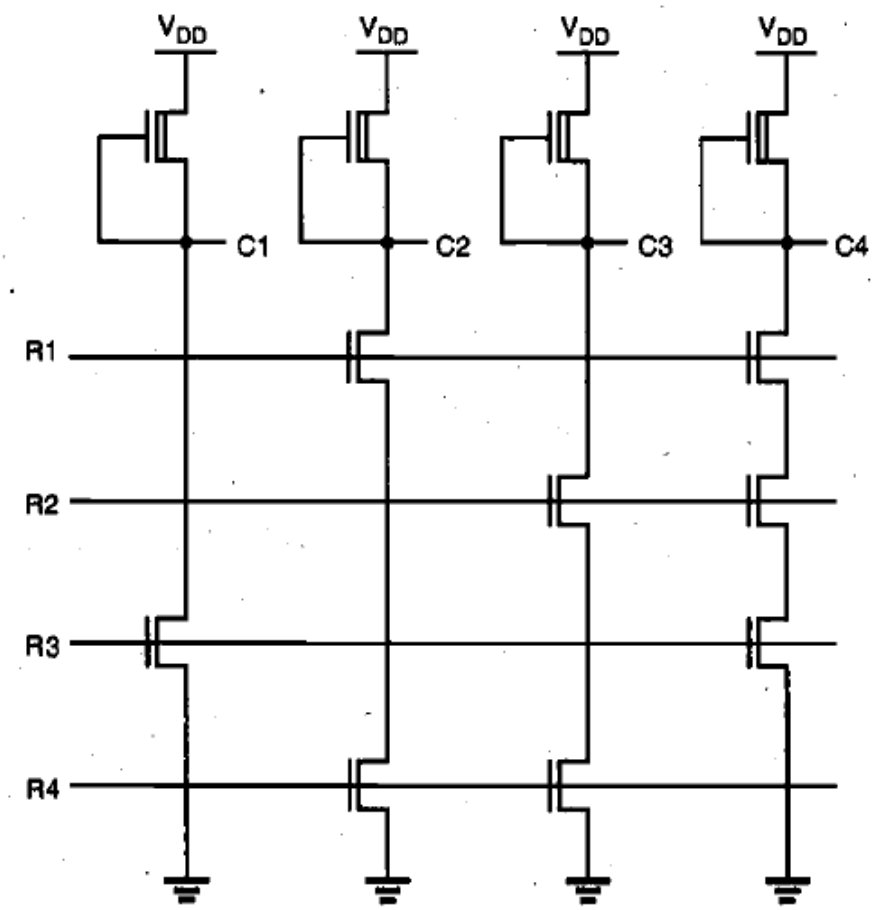
1) Figure (a) 4 X 4 NOR based ROM array :



2) Truth table for NOR based ROM array

R1	R2	R3	R4	C1	C2	C3	C4
1	0	0	0	0	1	0	1
0	1	0	0	0	0	1	1
0	0	1	0	1	0	0	1
0	0	0	1	0	1	1	0

3) Figure (b) 4 X 4 NAND based ROM array



4) Truth table for NAND based ROM array

R1	R2	R3	R4	C1	C2	C3	C4
0	1	1	1	0	1	0	1
1	0	1	1	0	0	1	1
1	1	0	1	1	0	0	1
1	1	1	0	0	1	1	0

Theory:

Read-Only Memory (ROM) Circuits : The read-only memory array can also be seen as a simple combinational Boolean network which produces a specified output value for each input combination, i.e., for each address. Thus, storing binary information at a particular address location can be achieved by the presence or absence of a data path from the selected row (word line) to the selected column (bit line), which is equivalent to the presence or absence of a device at that particular location. In the following, we will examine two different implementations for MOS ROM arrays.

4-bit x 4-bit NOR ROM array : Consider first the 4-bit x4-bit memory array shown in Fig (a), each column consists of a pseudo-nMOS NOR gate driven by some of the row signals, i.e., the word lines.

Here only one word line is activated (selected) at a time by raising its voltage to *VDD,* while all other rows are held at a low voltage level. If an active transistor exists at the cross point of a column and the selected row, the column voltage is pulled down to the logic low level by that transistor. If no active transistor exists at the cross point, the column voltage is pulled high by the pMOS load device. Thus, a logic " 1 "-bit is stored as the absence of an active transistor, while a logic ""-bit is stored as the presence of an active transistor at the crosspoint. To reduce static power consumption, the pMOS load transistors in the ROM array shown in Fig. (a) can also be driven by a periodic precharge signal, resulting in a *dynamic* ROM.

4-bit x 4-bit NAND ROM array : Next, we will examine a significantly different ROM array design, which is also called a NAND ROM (Fig. b). Here, each bit line consists of a depletion-load NAND gate, driven by some of the row signals, i.e., the word lines. In normal operation, all word lines are held at the logic-high voltage level except for the selected line, which is pulled *down* to logic-low level. If a transistor exists at the crosspoint of a column and the selected row, that transistor is turned off and the column voltage is pulled high by the load device. On the other hand, if no transistor exists (shorted) at that particular crosspoint, the column voltage is pulled low by the other nMOS transistors in the multi-input NAND structure. Thus, a logic "1 "-bit is stored by the presence of a transistor that can be deactivated, while a logic "0"-bit is stored by a shorted or normally on transistor at the crosspoint.

Procedure: **Design Simulation**

1. Draw the circuit using DSCH3 tool.
2. Apply clock signal for all combinations of inputs R1, R2, R3 and R4.
3. Connect LED's at all observing nodes and verify the outpu.
4. Run the simulation and observe the output waveforms.

Conclusion: