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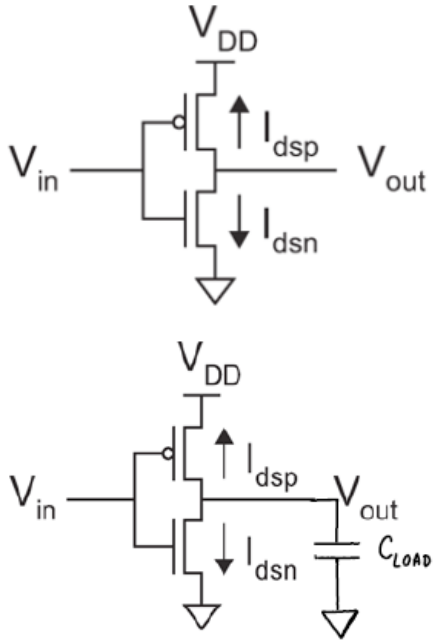
Department of Electronics Engineering

Experiment no: 08

Aim: Simulation and analysis of power dissipation in CMOS circuits.

Apparatus: PC loaded with LTspice software.

Circuit Diagram:



Circuit 1 : CMOS inverter with and without C_{load}

Theory: Static CMOS gates in older technologies were very power-efficient. In newer technologies, power is a primary design constraint. Power dissipation has skyrocketed due to transistor scaling, chip transistor counts and clock frequencies.

Static CMOS gates are very power-efficient because they dissipate nearly zero power while idle.

Instantaneous Power : The instantaneous power P(t) drawn from the power supply is proportional to the supply current $i_{DD}(t)$ and the supply voltage V_{DD}.

Energy consumed :
The energy consumed over the time interval T is the integral of P(t)

Average Power :
The average power over this interval P_{avg}

Instantaneous power: $P = i_{DD}(t) \cdot V_{DD}$

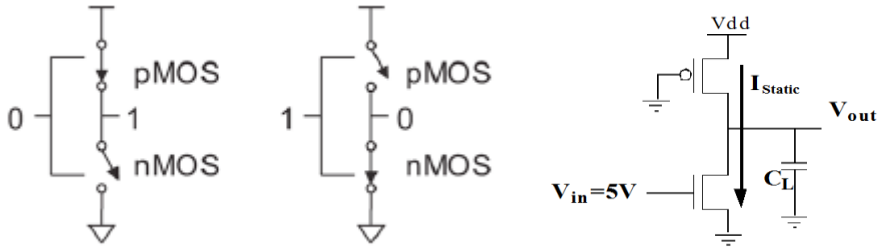
Energy consumed: $E = \int_0^T i_{DD} \cdot V_{DD} dt$

Average power: $P_{avg} = \frac{1}{T}\int_0^T i_{DD} \cdot V_{DD} dt$

Power dissipation in CMOS circuits comes from two components:

1) **Static power dissipation due to**
   a) Subtreshold conduction through OFF transistors.
   b) Tunneling current through gate oxide.
   c) Leakage through reverse biased diodes (in the parasitic diodes)

$P_{static} = V_{DD}I_{Ieakge}$



Here , OFF transistors still conduct a small amount of leakage current (I_{Ieakge})

2) **Dynamic power dissipation due to**
   a) Charging and discharging (switching) of the load capacitance (C_{load}) .
   b) "Short-Circuit" current while both pMOS and nMOS networks are partially ON.

This leads to :
i) Capacitance Switching Current: This flows to charge and discharge capacitance loads during logic changes.
ii) Short-Circuit Current: This is the current due to the DC path between the supply and ground during output transition.

Primary source of dynamic dissipation is charging of the load capacitance. Suppose load C_{load} is switched between V_{DD} and GND at average frequency f_{clock}. Over time T, load is charged and discharged $T.f_{clock}$ times.

In one complete charge/discharge cycle, a total charge of $Q=CV_{DD}$ is transferred between V_{DD} and GND.The average dynamic power dissipation is

$$P_{dynamic} = P_{sw} + P_{sc} = \frac{1}{T}\int_0^T i_{DD}(t) \cdot V_{DD} dt = \frac{V_{DD}}{T}\int_0^T i_{DD}(t) dt$$

Assuming a logic gate goes through one complete charge/discharge cycle every clock cycle and thus taking the integral of current over the interval T as the total charge delivered during time T

$$P_{sw} = C \cdot V_{DD}^2 \cdot f_{clock}$$

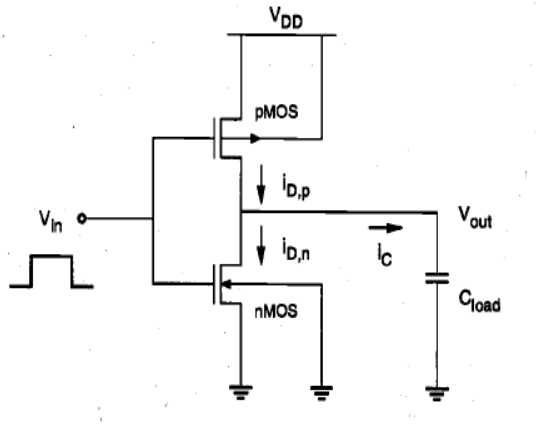
Because most gates do not switch every clock cycle, we introduce a corrective activity factor α :

$$P_{sw} = \alpha \cdot C \cdot V_{DD}^2 \cdot f_{clock}$$

As not all gates switch every clock cycle the above quantity is multiplied by α. A clock has α =1 because it rises and fall every cycle, but most data have a maximum activity factor α =0.5 because they transition only once every cycle empirically static CMOS has α=0.1

Now because, input rise/fall time is greater than zero, both nMOS and pMOS will be ON for a short period of time (while the input is between V_{tn} and V_{DD}-$|V_{tp}|$).
1) This results in a "short-circuit" current pulse from V_{DD} to GND
2) Typically this increases power dissipation by about 10%

Switching / Dynamic Power dissipation :
During switching events where the output load capacitance is alternatingly charged up and charged down, on the other hand, the CMOS inverter inevitably dissipates power.



. CMOS inverter used in the dynamic power-dissipation analysis.

When the input voltage switches from low to high, the pMOS transistor in the circuit is turned off, and the nMOS transistor starts conducting. During this phase, the output load capacitance Cad is being discharged through the nMOS transistor. Thus, the capacitor current equals the instantaneous drain current of the nMOS transistor. When the input voltage switches from high to low, the nMOS transistor in the circuit is turned off, and the pMOS transistor starts conducting. During this phase, the output load capacitance C_{load} is being charged up through the pMOS transistor; therefore, the capacitor current equals the instantaneous drain current of the pMOS transistor.

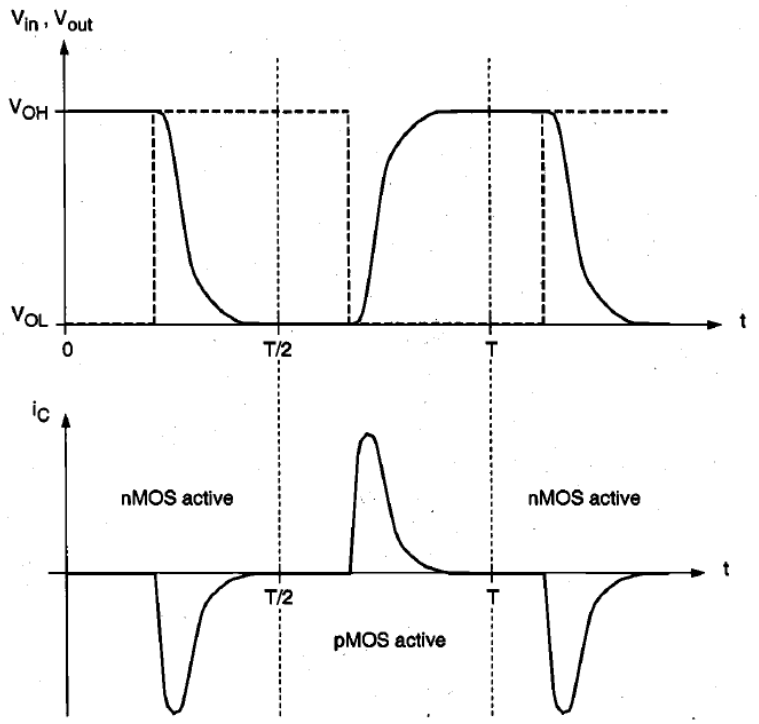


Figure : Typical input and output voltage waveforms and the capacitor current waveform during switching of the CMOS inverter.

$$P_{sw} = C \cdot V_{DD}^2 \cdot f_{clock}$$

It is clear from above formula that the average power dissipation of the CMOS inverter is proportional to the switching frequency f_{clock} .Therefore, the low-power advantage of CMOS circuits becomes less prominent in high-speed operation, where the switching frequency is high. Also note that the average power dissipation is independent of all transistor characteristics and transistor sizes.

Note that under realistic conditions, when the input voltage waveform deviates from ideal step input and has nonzero rise and fall times, for example, both the nMOS and the pMOS transistor will simultaneously conduct a certain amount of current during the switching event. This is called the short-circuit current, since in this case, the two transistors temporarily form a conducting path between the V_{DD} and the ground.

Procedure: **Design Simulation**

1. Draw the circuit 1 in the schematic of LTspice.

2. Apply V_{DD} and clock signal Vin to the inverter.

3. Run the simulation and observe the drain current waveforms for driver transistor for CMOS inverter.

4. Repeat Steps 2 to 3 for C_{Load} = 0.05pf and 0.2pf .

Conclusion: