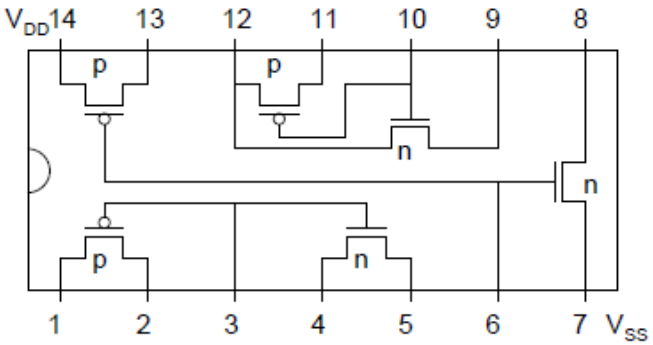
Dwarkadas. J. Sanghvi College of Engineering
Department of Electronics Engineering

Experiment no: 03

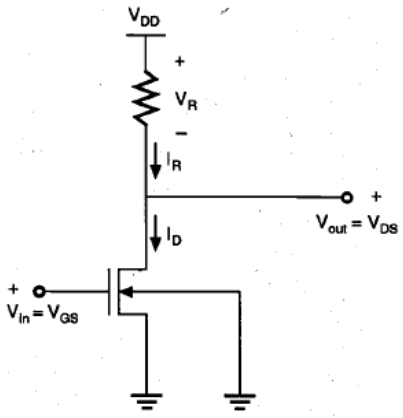
Aim: Estimation of Noise Margin Levels for
a) NMOS Inverter with resistive load
b) CMOS Inverter

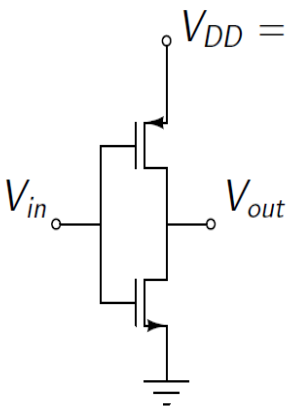
Apparatus: CD 4007, breadboard, multimeter, resistors, LED, power supply (0 – 15 V) , connecting wires.

Circuit Diagram: **1) Pinout of IC CD4007**



2) Circuit diagram for Resistive load and CMOS Inverter





Truth Table

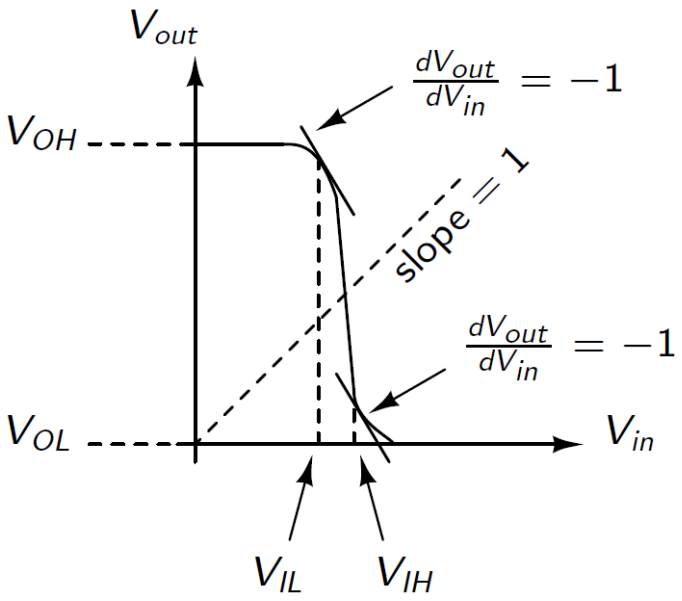
V_{in}	V_{out}
0 V	5 V
5 V	0 V

3) Observation Tables for both the circuits

Theory: Noise margin indicates the maximum amount of noise voltage that can be tolerated so that the logic levels are interpreted correctly. Inverter switching threshold (the value of V_{in} at the point where the slope = -1 line cuts the plot)

V_{OH}, V_{OL}, V_{IH}, V_{IL} determine the noise margin of the inverter.
V_{OL} = max output voltage for a valid "0"

V_{OH} = min output voltage for a valid "1"
V_{IL} = max input voltage for a valid "0"
V_{IH} = min input voltage for a valid "1"



Procedure: **Part A: Hardware Implementation**

1. Draw the circuit with pin number and variables.

2. Make the connections as per the circuit diagrams and wire them on breadboard .

3.Test both the inverter's functionality by applying an input of 5V and 0V and verify the inverter output.

4.Vary input voltage V_{in} from 0 to 5 volts in small steps and note the corresponding output voltage V_{out}.

5. From the data obtained in step 4, plot V_{out} v/s V_{in} on a linear graph. From the graph, try to estimate noise margin for low and high signal levels.

6. From the plot, try to identify the regions in which each transistor is in cutoff, linear or saturation region.

.
Conclusion:

Plot VTC curves on graph paper.