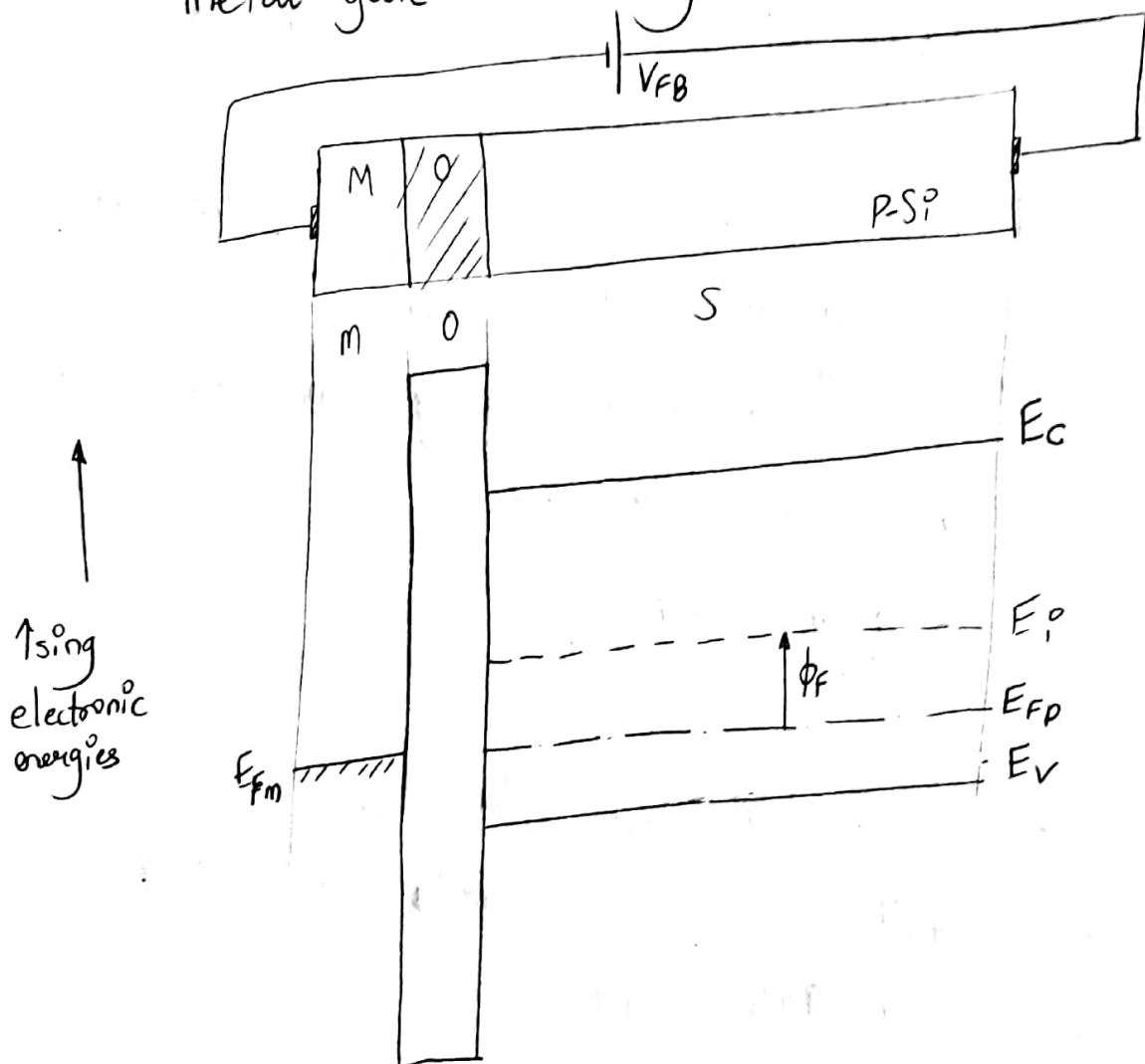
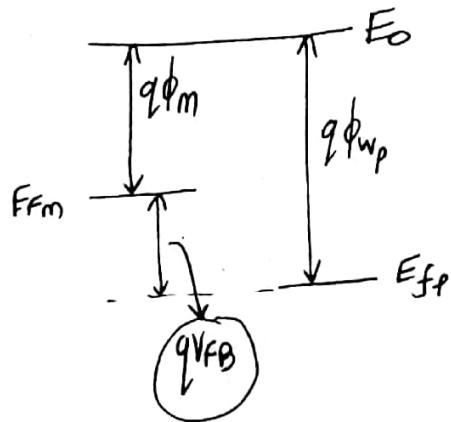


→ Flat-band condition in MOS capacitor :-

- To achieve flat-band condition in a MOS capacitor, we have to remove negative charge in P-Si substrate under equilibrium. So, we apply negative voltage to metal gate w.r.t body.



Note :- a) When a fermi-level moves up, it means you are applying a negative voltage.
 b) Flat band means zero-charge condition in semiconductor



$$V_{FB} = \phi_{ms} - \frac{\phi_{ox}}{C_ox}$$

contact

- As evident from EBD of isolated MOSCAP, a potential exist due to difference betn work function of metal & semiconductor.
- When a external voltage $-V_{FB} = -(\phi_{wp} - \phi_m)$ is applied to MOSCAP, it is in Flat-band condition
- Under flat-band condition, all the energy bands are flat
- From above EBD, it is clear that

$$qV_{FB} = -q(\phi_m - \phi_{wp})$$

It means that Flat-band voltage equal to difference betn ϕ_m & ϕ_{wp} should be applied externally to a MOS capacitor.

- In flat-band condition, the bands in the silicon (and oxide) are flat. As a consequences, there is no net charge in the semiconductor or on the metal and the electric field is zero everywhere.

→ Band bending in the MOS Capacitor :

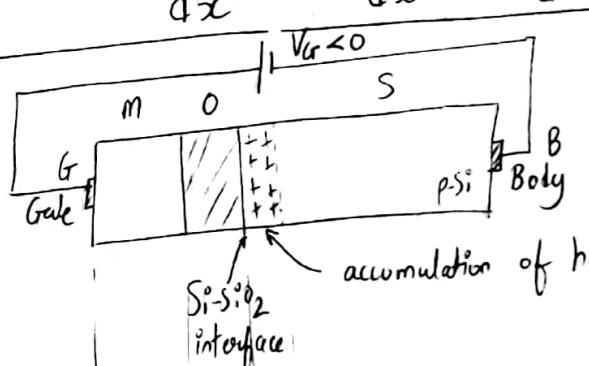
- This section explores what happens when a voltage is applied to the gate of the MOS capacitor, and the different band bendings that result at the semiconductor surface.

Note:- Recall from semiconduct theory → Presence of an electric field E causes a bending of the bands, given by

$$qE = \frac{dE_C}{dx} = \frac{dE_i}{dx} = \frac{dE_v}{dx}$$

1. Accumulation :-

means pile up of majority carriers at the Si-SiO_2 interface



accumulation of holes near Si-SiO_2 interface.

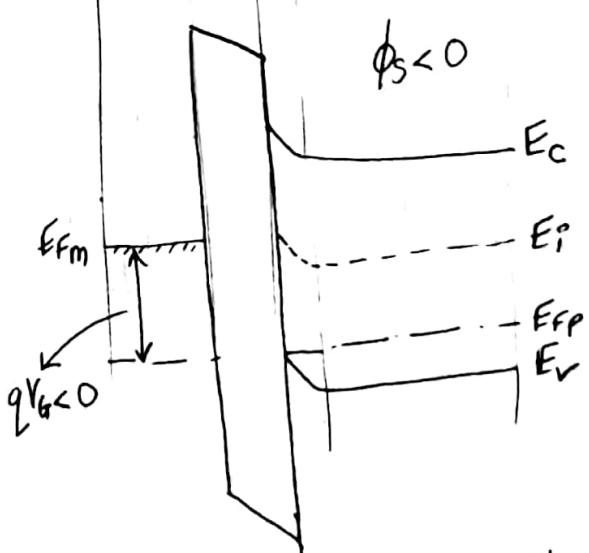
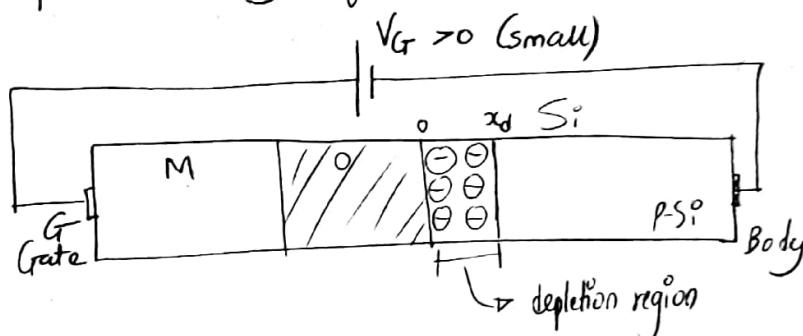


fig (a) EBD of MOS capacitor in Accumulation ($V_{G>0}$) condition

- When the gate voltage applied is negative ($V_G < 0V$), majority carriers (holes) are attracted to the surface of the semiconductor from the bulk.
 - The excess carriers produce a positively charged layer at the surface, which is matched by negative charge at the metal-oxide interface.
 - There is an electric field in the oxide which penetrates slightly into the semiconductor, producing band-bending, as shown in fig(a).
 - Note that the fermi-levels in the semiconductor and metal are separated by qV_G .
 - This condition is called "accumulation", since it results in an accumulation of majority carriers at the Si-SiO₂ interface.
- We now define the surface potential (ϕ_S) or (ψ_S) This is the total amount of band bending at the surface of the semiconductor measured w.r.t bulk.
- The band bending can be measured on E_i, E_c or E_v.

- In this case, the bands bend upwards and ϕ_s (by definition) will be considered to be negative.
- For typical applied voltages in accumulation, ϕ_s is limited to -0.1 to -0.2 V.

2. Depletion: When the gate voltage applied is positive and not too large ($V_G > 0V$), the majority carriers are repelled away from the surface of p-Si producing a depletion region.



(fig b)

means removal
of majority
carriers at
the Si-SiO₂
interface -

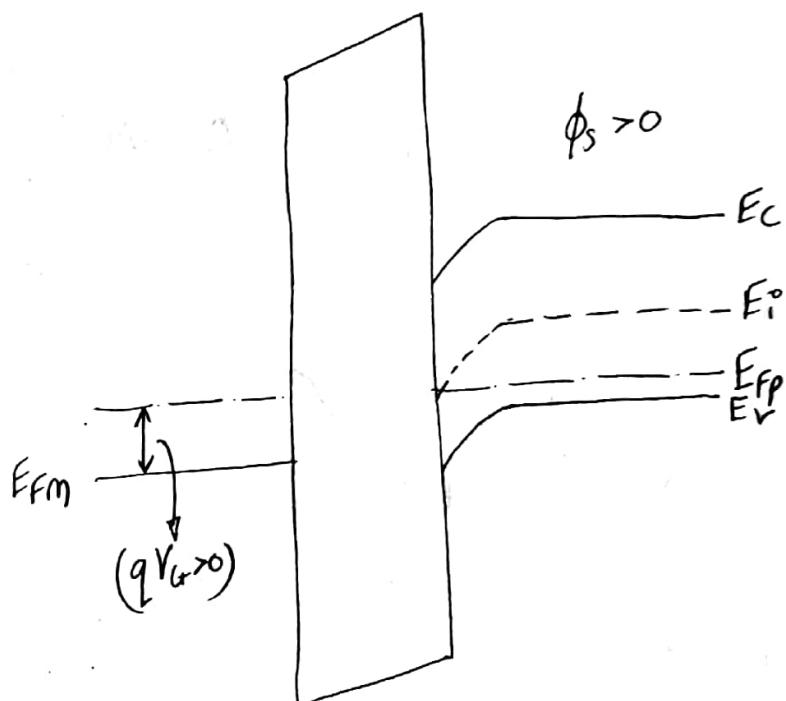
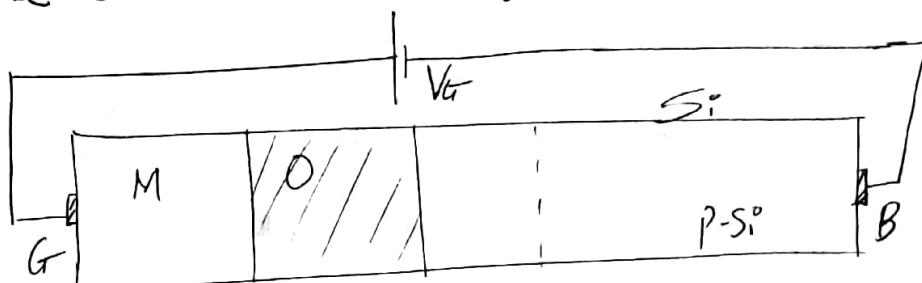


fig b: EBD of MOS Capacitor in depletion ($V_G > 0$ small)

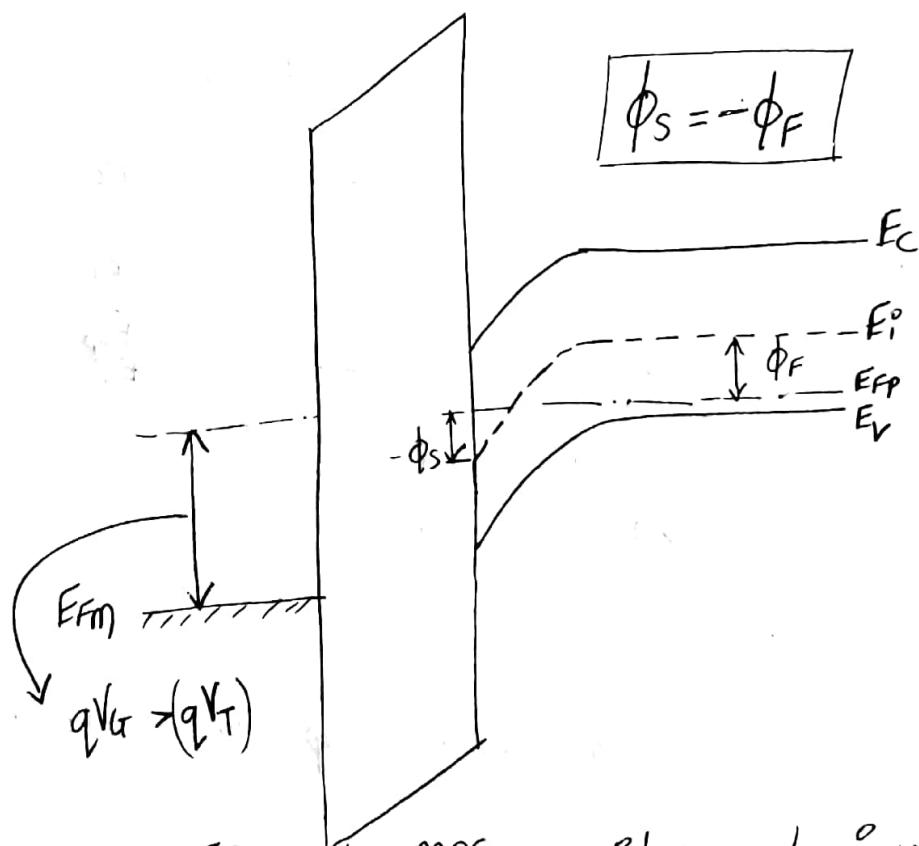
- The depletion region contains a negative charge corresponding to the ionized immobile acceptors.
- The bands now bend downwards and ϕ_s is positive as evident in fig b.
- This condition is known as "Depletion".

3. Inversion :- Finally, when the gate voltage applied is positive and sufficiently large, the bands in the semiconductor bands as shown in fig c.



means pile-up
of minority
carriers

so that they
dominate the
"bulk" majority
carriers at
the interface



figc. EBD of MOS capacitor under inversion

- In this case, the energy bands in the semiconductor bend enough that the conduction band comes close to the fermi level.
 - This means that the surface of the semiconductor layer has effectively become n-type, and there are mobile minority carriers (electrons) present at the surface.
 - This condition is known as "inversion", because the surface has been effectively inverted from p-type to n-type.
- [It is the carriers in the inversion layer which contributes to conduction in a MOS transistor.]
- A common definition of the onset of inversion is that the p-Si surface is as n-type as the bulk is p-type. ($n_s = P_B$)
 ↑
 no of holes in bulk
 ↓
 no of e's at surface
 - At inversion, $\phi_s = -\phi_F$ bulk & surface fermi potential are equal in magnitude but opposite in sign.
 - In inversion, the negative charge in the inversion layer adds to the negative charge in the depletion region.