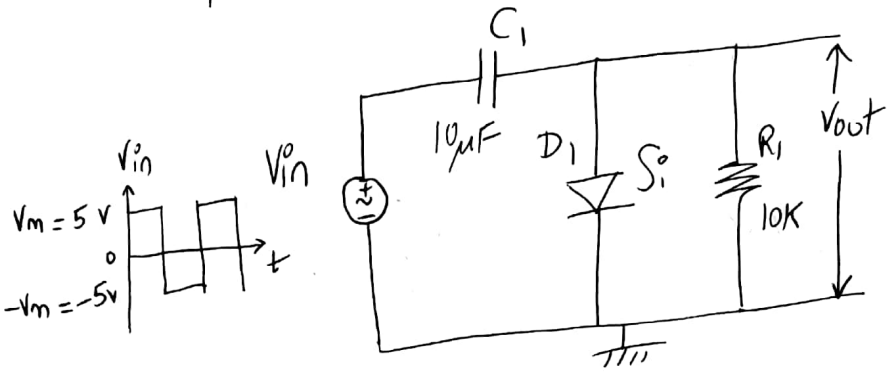
Clamper circuits

25/11/19

Numerical 01:-

Identify the circuit below and draw output waveform with proper voltage levels. Write the output expression



Solution:-

→ Since given diode is Si, we will prefer constant voltage model (ie $V_{D_{ON}} = 0.7V$)

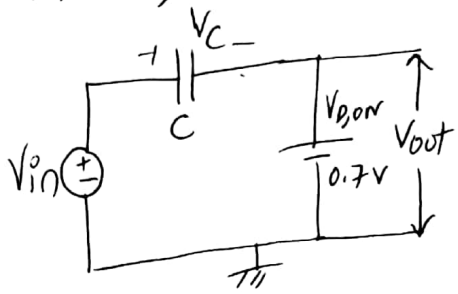
→ Given $V_{in} = 10V_{p-p}$ ie $V_m = 5V$

→ Assumption:-

RC time constant is large enough (than time period of i/p sig) to ensure that voltage across capacitor does not discharge significantly during the period the diode is OFF.

Operation:

a) During positive half cycle, Diode D_1 is ON when $V_{in} > V_{D,on}$ ie the circuit becomes:



ie $\boxed{V_{out} = V_{D,on} = 0.7V}$ ---during +ve half cycle of AC I/P

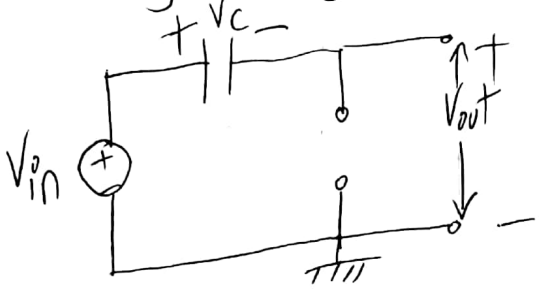
→ At the same time, C_1 charges and voltage across capacitor V_C reaches upto V_m.

KVL gives us: $V_{in} - V_C - V_{D,on} = 0$

$V_C = V_{in} - V_{D,on} = V_m - V_{D,on} = 5 - 0.7$

$\boxed{V_C = 4.3}$ ----voltage across capacitor during positive half cycle

b) During negative half cycle, Diode D_1 is OFF for entire negative cycle, ie the circuit becomes



Note: During -ve half cycle, capacitor holds the charges $V_C = 4.3V$ and act as a battery

KVL gives us:

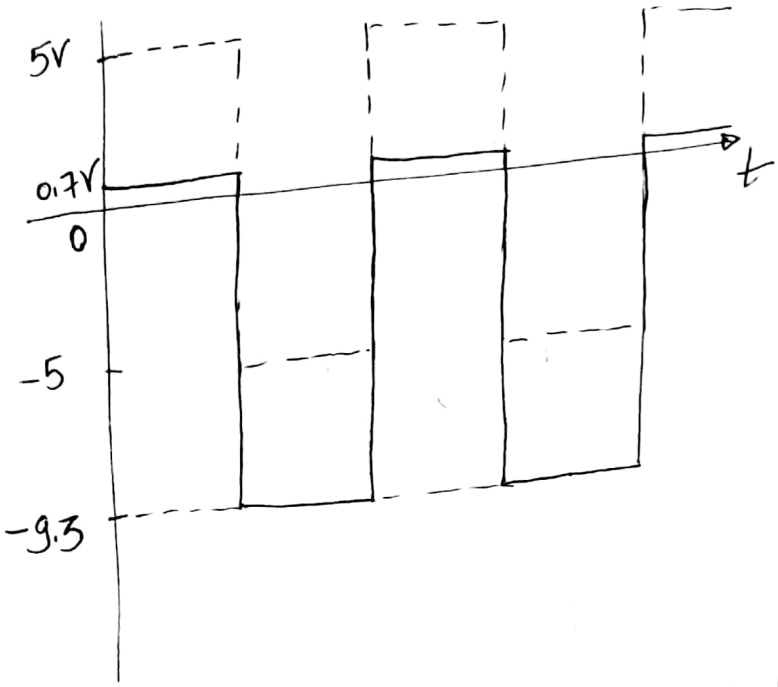
$$-V_{in} - V_c - V_{out} = 0$$

$$V_{out} = -V_{in} - V_c = -V_m - V_c$$

$$V_{out} = -5 - 4.3 = -9.3V$$

ie $\boxed{V_{out} = -9.3V}$ --- during -ve half cycle

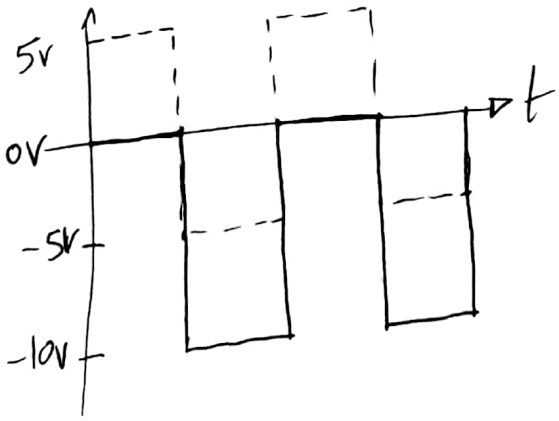
I/p and o/p waveforms:-



$V_{0,ON} = 0.7V$

→ Since, the o/p waveform is shifted down of x-axis, the given circuit is a Negative clamper

→ If $V_{0,ON} = 0$ ie given diode was an ideal diode, then the above waveforms would have looked like.



$V_{0,ON} = 0V$

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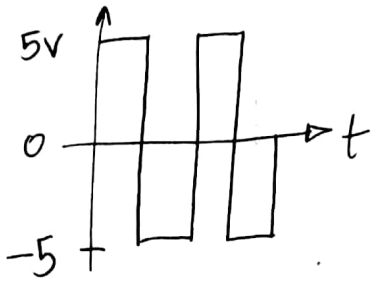
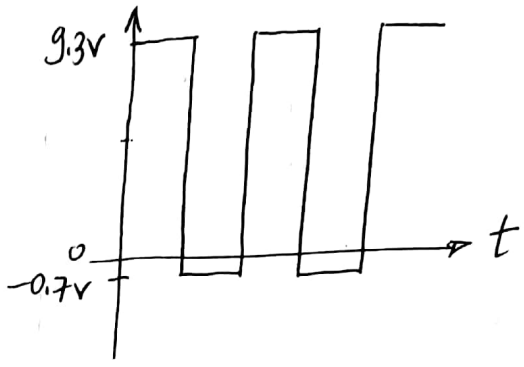
Design 01:-

Design a diode clamper to generate a steady state output Vout from the i/p Vin shown in the figure below :-



Vin(t)



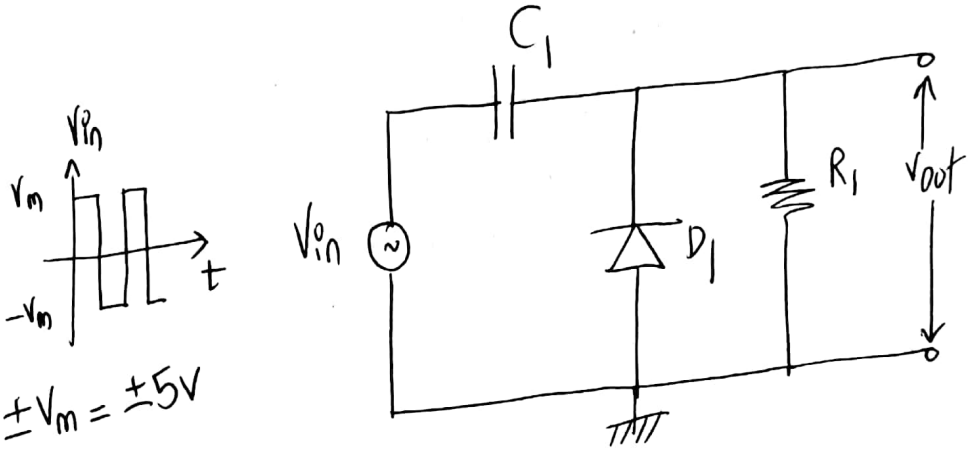
Vout(t)

Soln:- 1) Inspecting the above waveforms, we have to shift the waveform above x-axis by some amount Hence, it's a Positive clamper.

2) From Vout(t), it is clear that we can use constant voltage model with $V_{\gamma,on} = 0.7V$

3) Also, from o/p waveforms, we deduce that during -ve half cycle of I/P, $V_{out} = -0.7V$ and during +ve half cycle of I/P, o/p is $V_{out} = 9.3V$

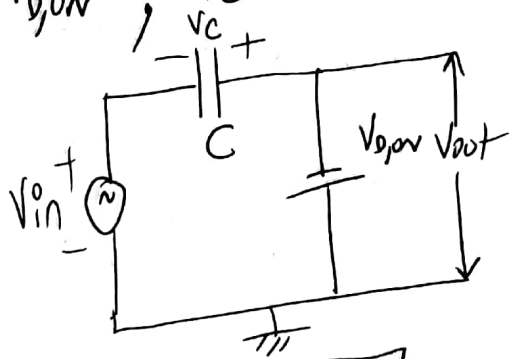
4) The diode clamper circuit which does this is shown below:



let's see how the above designed diode clamper gives the desired o/p.

Operation:-

a) During negative half cycle, D_1 is ON when $V_{in} < -V_{D,ON}$, ie the circuit becomes



ie $\boxed{V_{out} = -V_{D,ON} = -0.7V}$ --- during negative half cycle of I/P

This is consistent with our design

b) At the same time, C_1 charges and voltage across C_1 charges up to $-V_m$.

KVL gives us:

$$V_{in} + V_C + V_{D,on} = 0$$

$$V_C = -V_{in} - V_{D,on}$$

$$= -(-V_m) - V_{D,on}$$

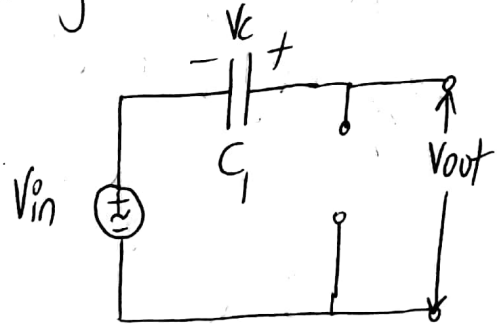
$$= -(-5) - 0.7$$

$$\boxed{V_C = 4.3V}$$

In negative half cycle $V_{in} = -V_m$

c) During the positive half cycle, Diode is OFF for entire positive cycle ie the circuit becomes,

Note:- During +ve half cycle, capacitor C_1 holds the charge $V_C = 4.3V$ & act as a batter



KVL gives,

$$V_{in} + V_C - V_{out} = 0$$

$$V_{out} = V_{in} + V_C$$

$$= V_m + V_C$$

$$= 5 + 4.3$$

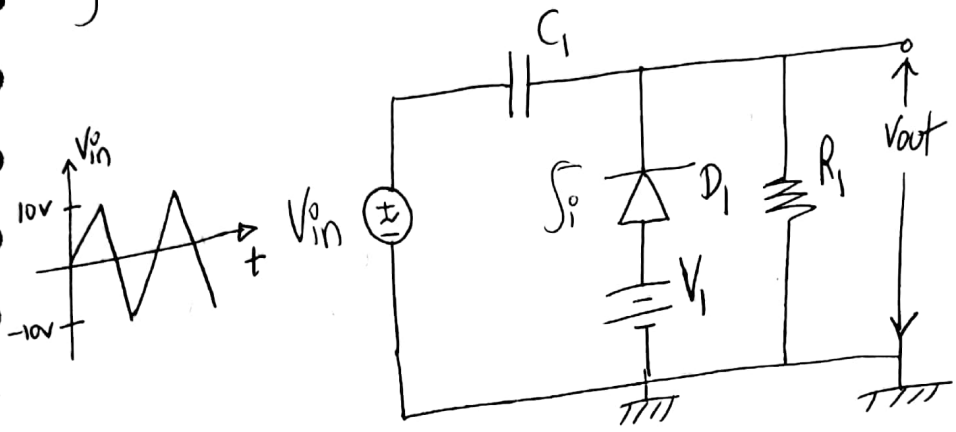
$$\boxed{V_{out} = 9.3V}$$

This value of o/p is in consistent with our design.

Numerical 02:-

Draw o/p waveforms with proper voltage levels for the circuit shown below:-

$V_1 = 2.7V$

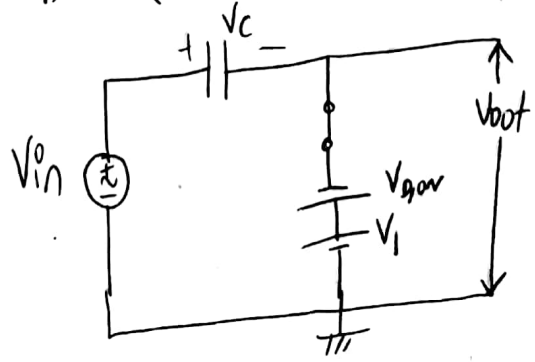


Soln:- 1) Since given diode D_1 is Si diode, we will use constant voltage model ie $\boxed{V_{\gamma on} = 0.7V}$

Given:- $V_{in} = 10V_{peak}$ ie $\pm V_m = \pm 10V$

Operation:-

a) During negative half cycle, D_1 is ON when $V_{in} < (-V_{\gamma on} + V_1)$, ⇒ ckt reduces to



ie $V_{out} = -V_{\gamma on} + V_1$

$= -0.7 + 2.7V$

$\boxed{V_{out} = 2V}$

ie $\boxed{V_{out} = 2V}$ --- during negative half cycle

b) At the same time, voltage across capacitor V_C charges upto $-V_m$

KVL gives us: $V_{in} + V_C + V_{D,on} - V_1 = 0$

$$V_C = -V_{in} - V_{D,on} + V_1$$

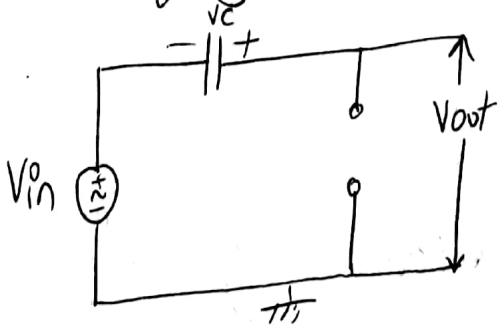
$$= -(-V_m) - 0.7 + 2.7$$

$$= 10 - 0.7 + 2.7$$

$\boxed{V_C = 12V}$ --- voltage across capacitor C_1 during +ve half cycle

-ve h.c $V_{in} = -V_m$

c) During positive half cycle, Diode D_1 is OFF for entire positive half cycle ie the circuit becomes



Note: During positive half cycle, capacitor C_1 holds the charge $V_C = 12V$ and act as a battery

KVL gives us :-

$$V_{in} + V_C - V_{out} = 0$$

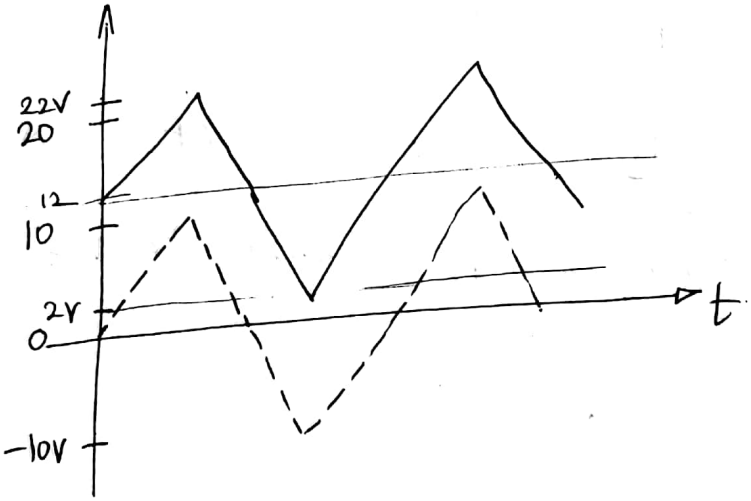
$$V_{out} = V_{in} + V_C$$

$$= V_m + V_C$$

$$= 10 + 12$$

$$\boxed{V_{out} = 22V}$$ --- during +ve half cycle

Input and Output waveforms :-

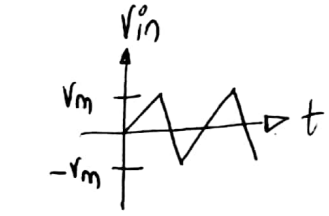


Note : The o/p waveform only shifts up and down the x-axis, without distorting the o/p at all.

→ Since, the o/p waveform is shifted above x-axis, the circuit is a Biased Positive clamper.

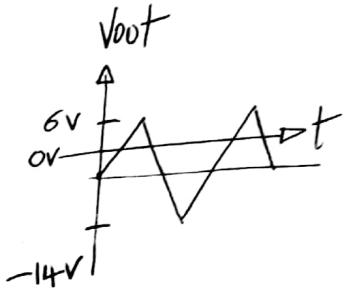
Design 02:

Design a circuit which does the following



$\pm V_m = \pm 10V$

Circuit

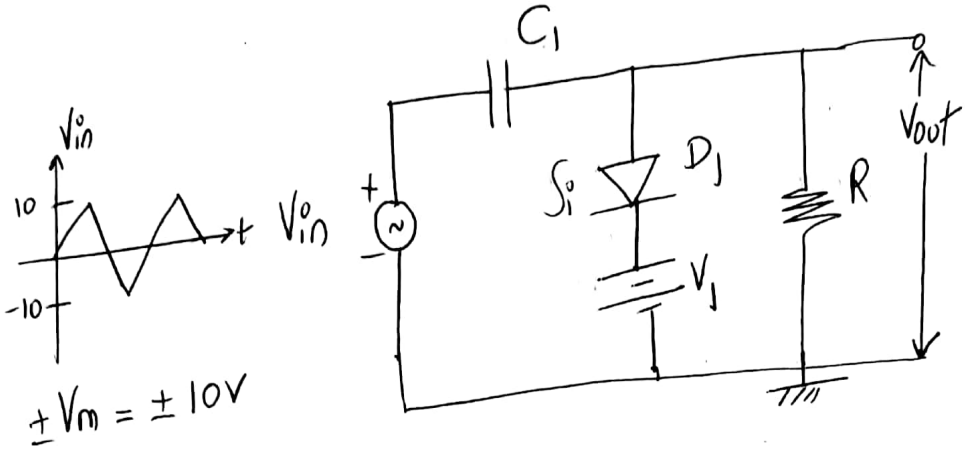


Soln:- 1) Inspecting the above waveforms, we have to shift the waveform below x-axis by some amount & also some +ve portion of o/p also remains above x-axis.
Hence, it must a Biased Negative clamper

2) From Vout (t), it is clear that we can either choose $V_{D,ON} = 0.7$ or $V_{D,ON} = 0V$
We will go with constant voltage model with $V_{D,ON} = 0.7V$.

3) Also, from o/p waveforms, we deduce that during +ve half cycle of I/P, Vout = +6V and during -ve half cycle of I/P, o/p is Vout = -14V

4) The diode clamper circuit which can produce such an o/p is:



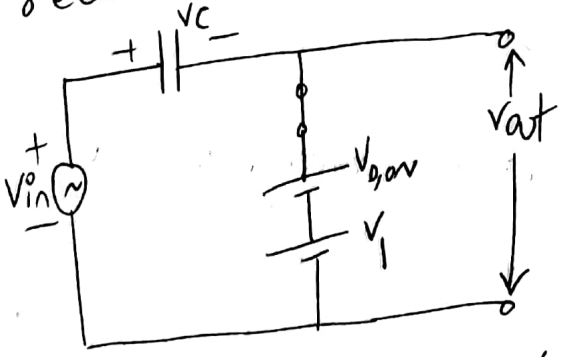
Consider D_1 as a Si diode

let's see how the above designed diode clamper gives the desired o/p

Operation:-

a) We want Vout = +6V during +ve half cycle ie during +ve half cycle, Diode D_1 should be ON when $V_{in} > V_{D,on} + V_1$

ie circuit reduces to



$V_{out} = V_{D,on} + V_1$

We know $V_{D,on} = 0.7V$

So, V_1 has to be 5.3

ie $\boxed{V_{out} = 0.7 + 5.3 = 6V}$ --- during +ve half cycle of I/P as desired

This is now consistent with our design

b) At the same time, voltage across C_1 charges up to V_m.

KVL gives us: $V_{in} - V_C - V_{D,ON} - V_1 = 0$

$V_C = V_{in} - V_{D,ON} - V_1$

$V_C = V_m - V_{D,ON} - V_1$

$V_C = 10 - 0.7 - 5.3$

$\boxed{V_C = 4V}$

It indicates the voltage across C_1 during positive half cycle.

c) During the negative half cycle, capacitor C_1 holds the charges $V_C = 4V$ and acts as a battery

Also, during -ve half cycle, Diode D_1 is OFF ie the circuit becomes

KVL gives us:- $V_{in} - V_C - V_{out} = 0$

$$V_{out} = V_{in} - V_C$$
$$= -V_m - V_C$$
$$= -10 - 4$$

$$\boxed{V_{out} = -14V}$$ --- during -ve half cycle as desired

During -ve half cycle, $V_{in} = -V_m$

Hence, the circuit which produce o/p as is given below