Design Rules for CMOS

- Design Rules
- Stick Diagrams
- Layout Diagram
- Examples

Design Rules: Introduction

- Design rules are a set of geometrical specifications that dictate the design of the layout
- **Layout is top view of a chip.**
- Design process are aided by stick diagram and layout
- Stick diagram gives the placement of different components and their connection details
- But the dimensions of devices are not mentioned
- Circuit design with all dimensions is Layout

Design Rules: Introduction

- Fabrication process needs different masks, these masks are prepared from layout
- Layout is an Interface between circuit designer and fabrication engineer
- Layout is made using a set of design rules.
- Design rules allow translation of circuit (usually in stick diagram or symbolic form) into actual geometry in silicon wafer
- These rules usually specify the minimum allowable line widths for physical objects on-chip
- Example: metal, polysilicon, interconnects, diffusion areas, minimum feature dimensions, and minimum allowable separations between two such features.

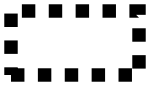
NEED FOR DESIGN RULES

- Better area efficiency
- Better yield
- Better reliability
- Increase the probability of fabricating a successful product on Si wafer

If design rules are not followed:

- Functional or non-functional circuit.
- Design consuming larger Si area.
- The device can fail during or after simulation.

Colour Codes :

Layer	Color	Representation
N+ Active	Green	
P+ Active	Yellow/Brown	
PolySi	Red	
Metal 1	Blue	
Metal 2	Magenta	
Contact	Black	X
Buried contact	Brown	X
Via	Black	X
Implant	Dotted yellow	
N-Well	Dotted Green/Black	

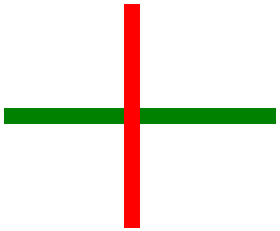
Stick Diagrams :

- A stick diagram is a symbolic representation of a layout.
- In stick diagram, each conductive layer is represented by a line of distinct color.
- Width of line is not important, as stick diagrams just give only wiring and routing information.
- Does show all components/vias, relative placement.
- Does not show exact placement, transistor sizes, wire lengths, wire widths, tub boundaries.

Stick Diagrams: Basic Rules

- Poly crosses diffusion forms transistor
- Red (poly) over Green(Active), gives a FET.

L:W



nFET/
nMOS

- Aspect Ratio

L:W

pFET/pMOS

Stick Diagrams (CMOS): Basic Steps

- Normally, the first step is to draw two parallel metal (blue) V_{DD} and GND rails.
- There should be enough space between them for other circuit elements.
- Draw Demarcation line (Brown) at center of V_{DD} and GND rails.
- This line represents the well (n/p-well).
- Next, Active (Green/yellow) paths must be drawn for required PU & PD transistors above & below DL.
- Draw vertical poly crossing both diffusions (Green & yellow)
- Remember, Poly (Red) crosses Active (Green/yellow), where transistor is required.

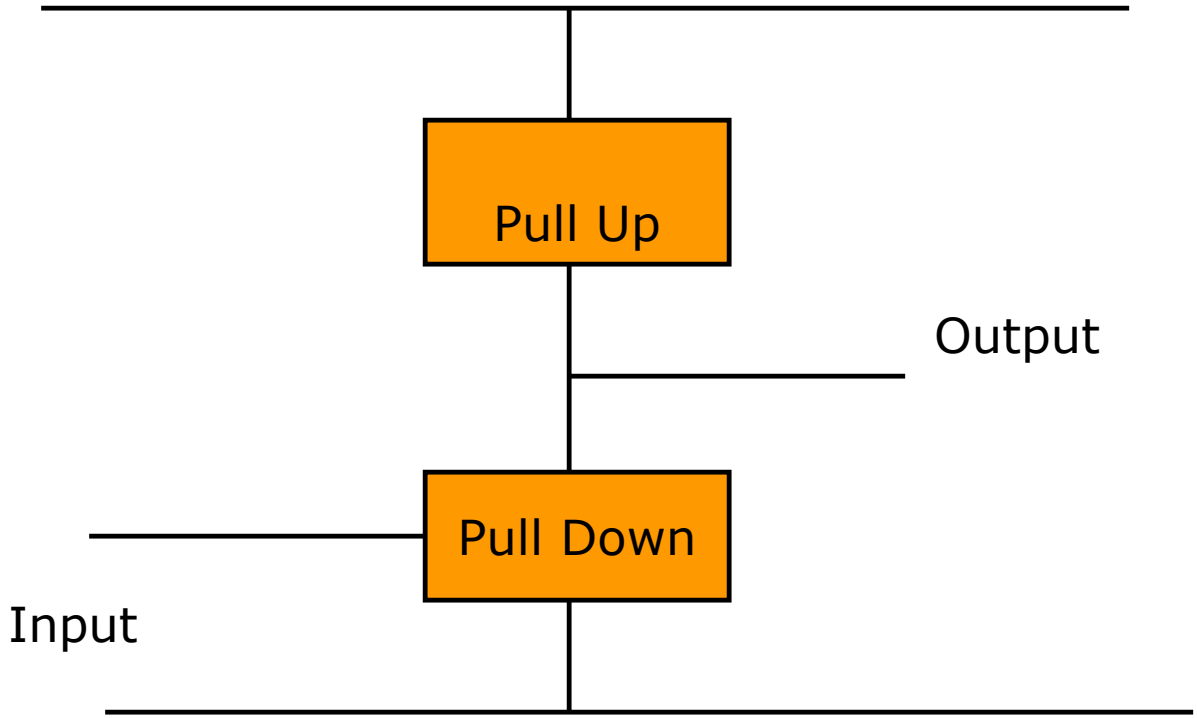
Stick Diagram (CMOS): Basic Steps

- No Diffusion can cross demarcation line.
- Only poly and metal can cross demarcation line
- N-diffusion and p-diffusion are joined using a metal wire.
- Place all PMOS above and NMOS below demarcation line.
- Connect them using wires (metal).
- Blue may cross over red or green, without connection.
- Connection between layers is specified with **X**.
- Metal lines on different layer can cross one another, connections are done using via.

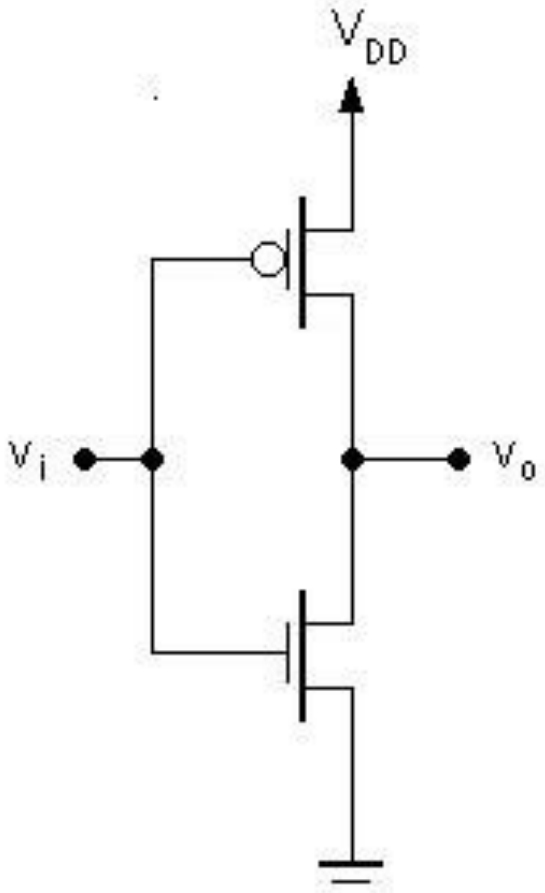
Inverter Using MOSFET

- Enhancement-Mode MOSFETs act as switches.
- They are switched OFF, when the input to gate is low.
- So, they can be used to pull the output down.
- Now, for pull-up, we can use a resistor.
- But resistors consume larger area.
- Another alternative is using MOSFET as pull-up.
- PU's can be NMOS or PMOS.

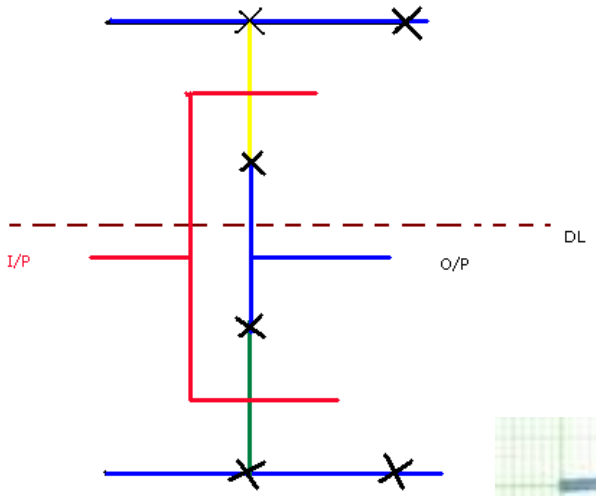
Inverter Using MOSFET

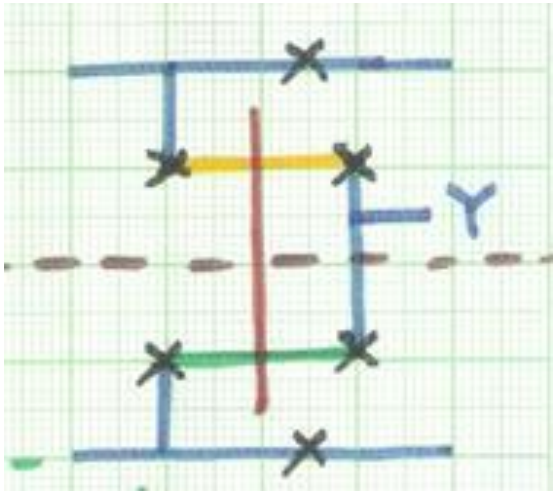


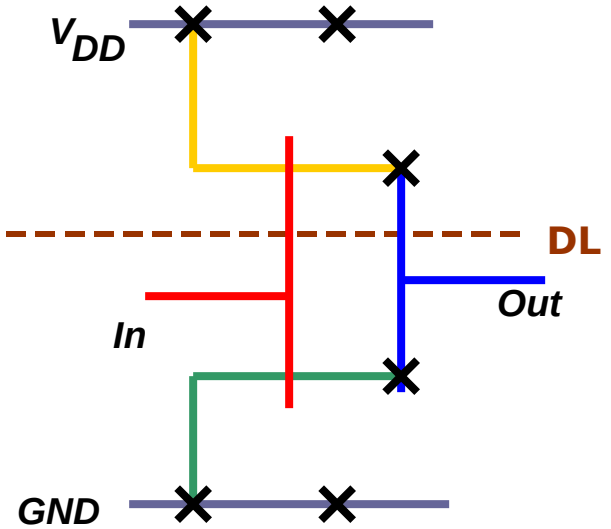
CMOS Invertor (Cicuit Diagram)



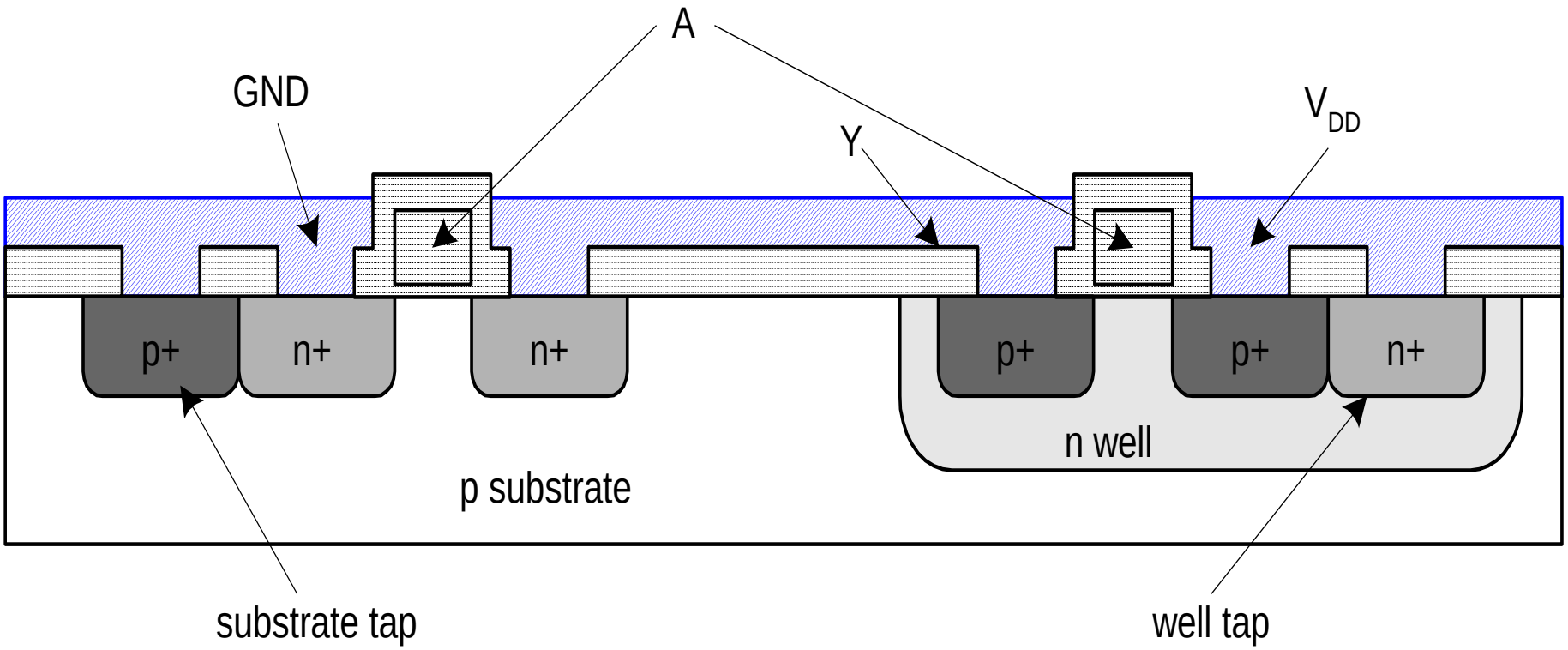
CMOS Invertor (Stick Diagram)







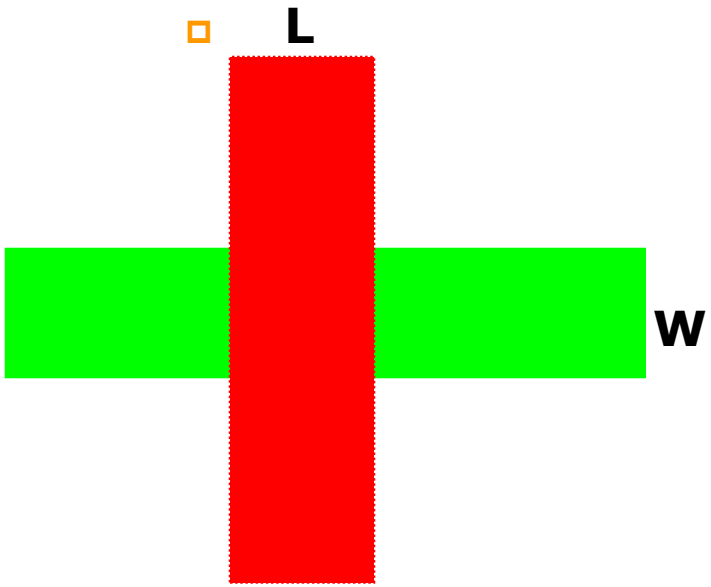
CMOS INVERTER :

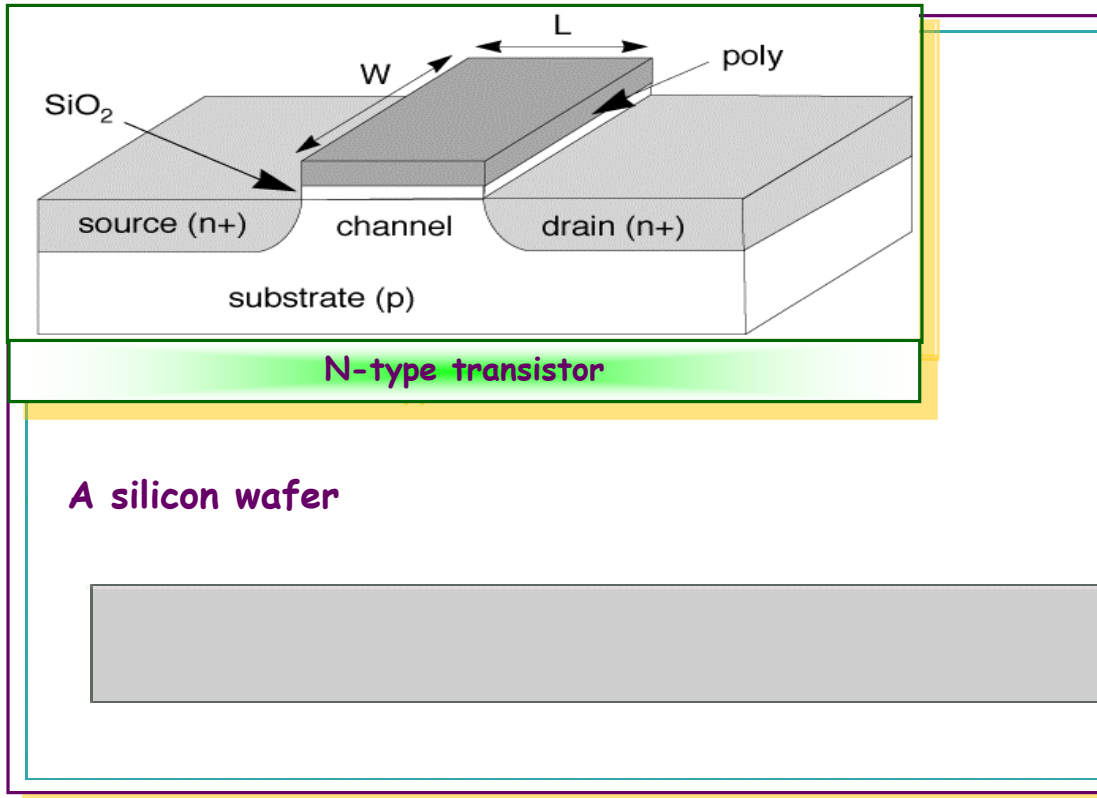


Well Biasing :

- The various N and P diffusions must be reverse biased to ensure that those wells are insulated from each other.
- This requires that the N- wells are connected to the most positive voltage, VDD.
- The P- substrate must be connected to the most negative voltage, ground.
- This assumes that all other nets are at a voltage between 0V and VDD.

MOSFET


L
W


L
W
poly
SiO_2
source (n+)
channel
drain (n+)
substrate (p)
N-type transistor
A silicon wafer

Types of Layout Design Rules

- Industry Standard: Micron Rule
- λ Based Design Rules

Types of Design Rules (Contd…)

- Industry Standard: Micron Rule
  - All device dimensions are expressed in terms of absolute dimension(μm/nm)
  - These rules will not support proportional scaling

Types of Design Rules (Contd…)

- λ Based Design Rules :
  - Developed by Mead and Conway.
  - All device dimensions are expresses in terms of a scalable parameter λ.
  - λ = L/2; L = The minimum feature size of transistor
  - L = 2 λ
  - These rules support proportional scaling.
  - They should be applied carefully in sub-micron CMOS process.

Design Rules

- Minimum length or width of a feature on a layer is **2λ**
  - To allow for shape contraction
- Minimum separation of features on a layer is 2λ
  - To ensure adequate continuity of the intervening materials.

Design Rules :

- Two Features on different mask layers can be misaligned by a maximum of 2λ on the wafer.
- If the overlap of these two different mask layers can be catastrophic to the design, they must be separated by at least 2λ
- If the overlap is just undesirable, they must be separated by at least λ

Design Rules: CMOS

- Line size and spacing:
  - **metal1:**
    - Minimum width=3λ, Minimum Spacing=3λ
  - **metal2:**
    - Minimum width=3λ, Minimum Spacing=4λ
  - **poly:**
    - Minimum width= 2λ, Minimum Spacing=2λ
  - **ndiff/pdiff:**
    - Minimum width= 3λ, Minimum Spacing=3λ,
  - **wells:**
    - minimum width=6λ,
      minimum n-well/p-well space = 6λ(They are at same potential)
      = 9λ (They are at different potential)

Design Rules: CMOS

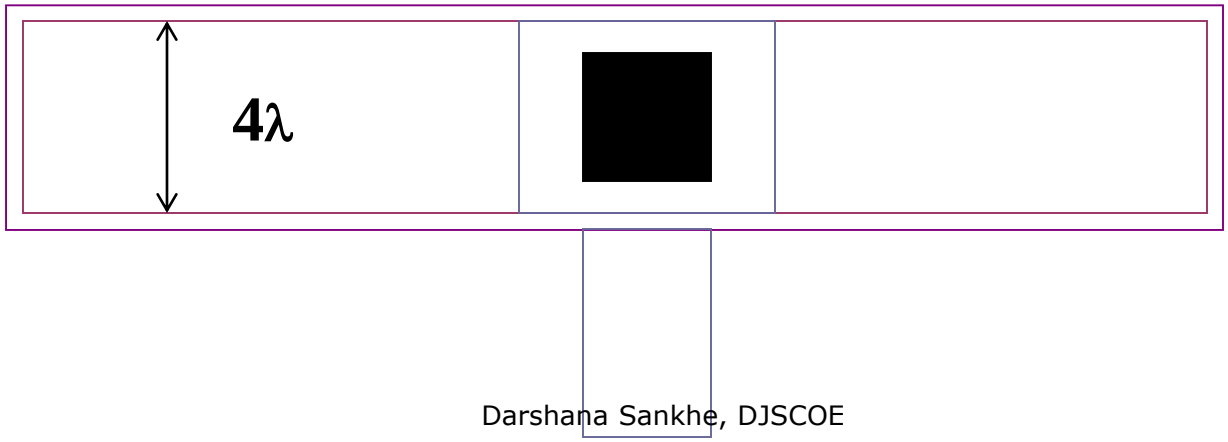
- Transistors:
  - Min width=3λ
  - Min length=2λ
  - Min poly overhang=2λ

- Contacts (Vias)
  - Cut size: exactly 2λ X 2λ
  - Cut separation: minimum 2λ
  - Overlap: min 1λ in all directions

Contact Cut :

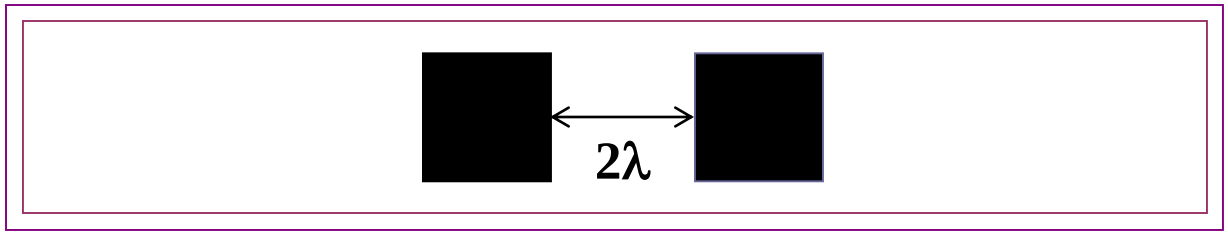
- **Metal connects to polySi/diffusion by contact cut.**
- **Contact area: 2λ*2λ**

- **Metal and polySi or diffusion must overlap this contact area by λ so that the two desired conductors encompass the contact area despite any mis-alignment between conducting layers and the contact hole**



Contact Cut

- **Contact cut – contact cut: 2λ apart**
- **Why? To prevent holes from merging.**



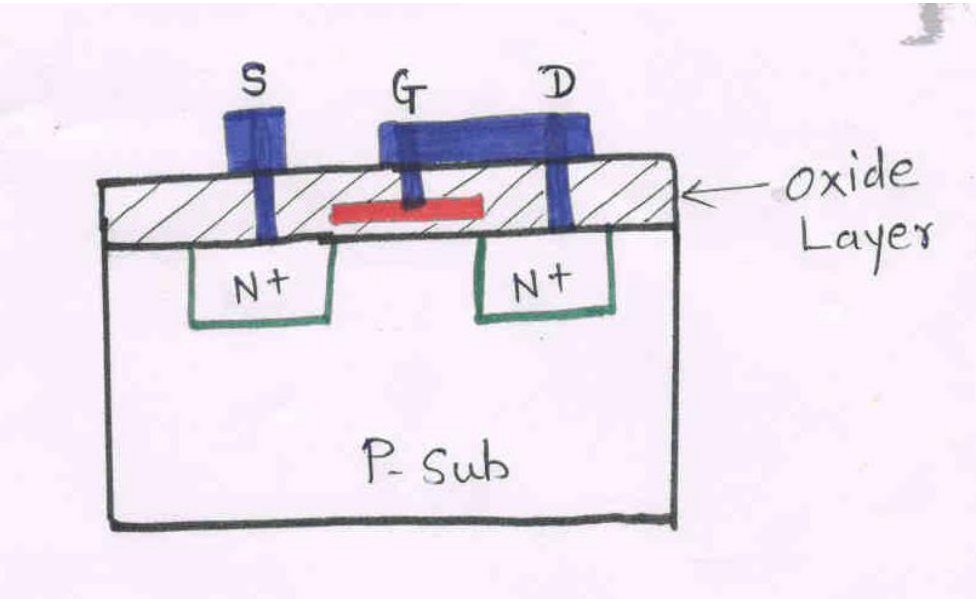
Interlayer Contacts :

- Interconnection between poly and diffusion is done by contacts.

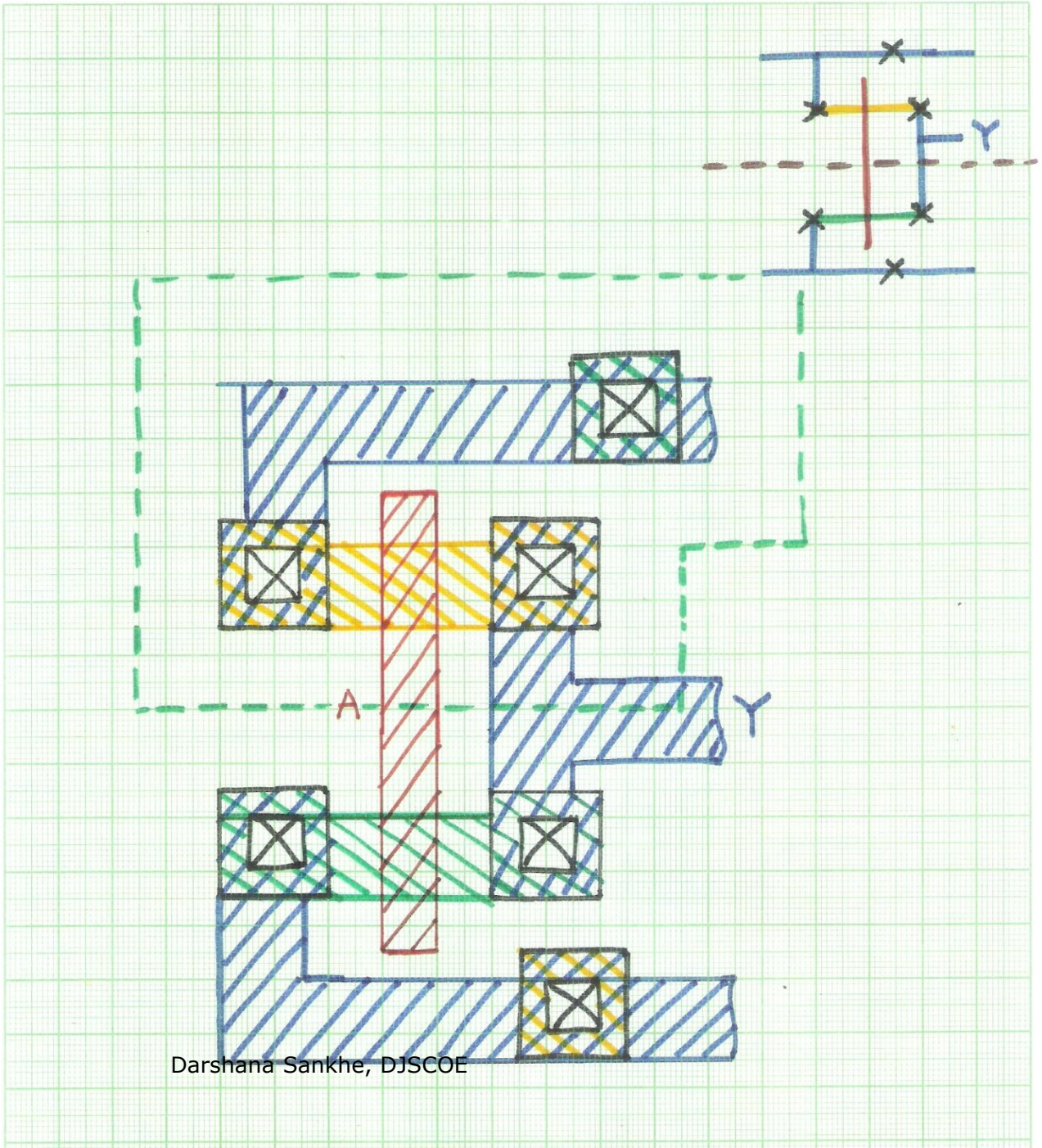
- Metal contact
- Butting contact
- Buried contact

Metal contact :

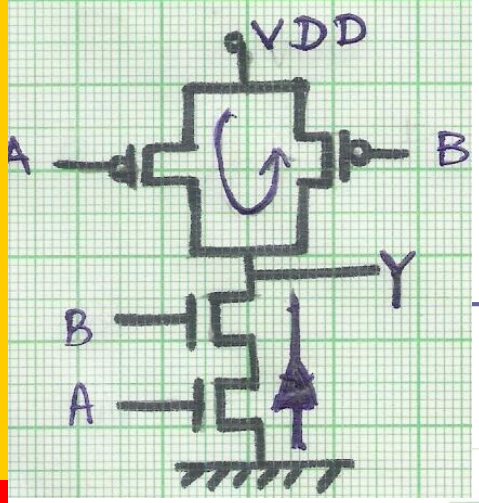
- Contact cut of 2λ * 2λ in oxide layer above poly and diffusion
- Metal used for interconnection
- Individual contact size becomes 4λ * 4λ

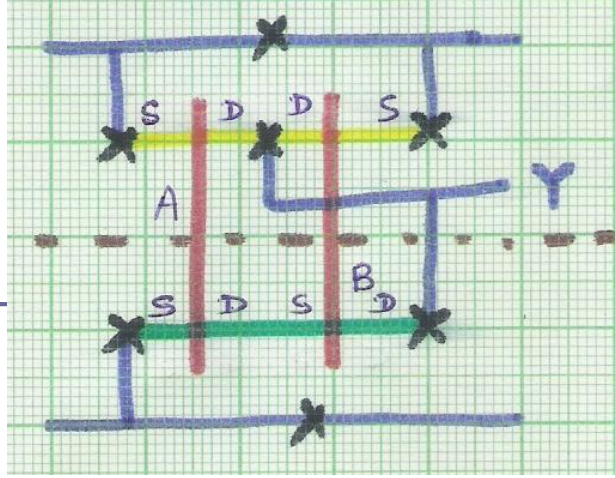


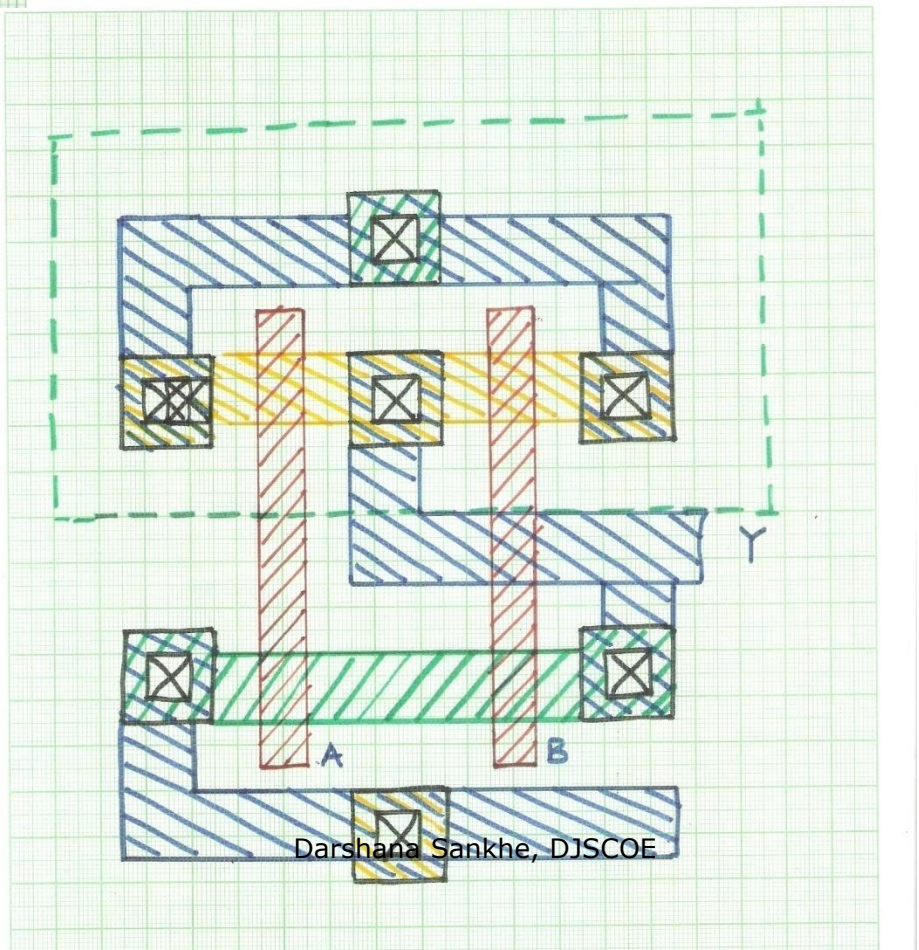
CMOS Inverter:



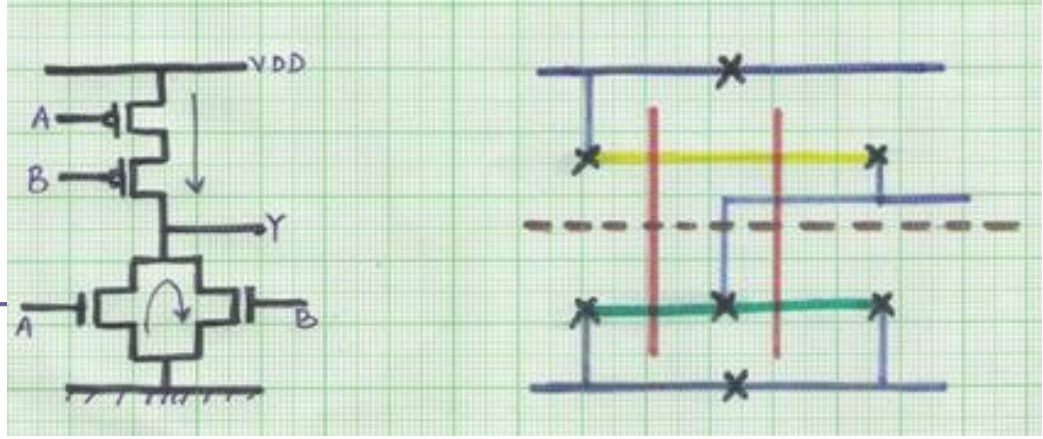
CMOS NAND

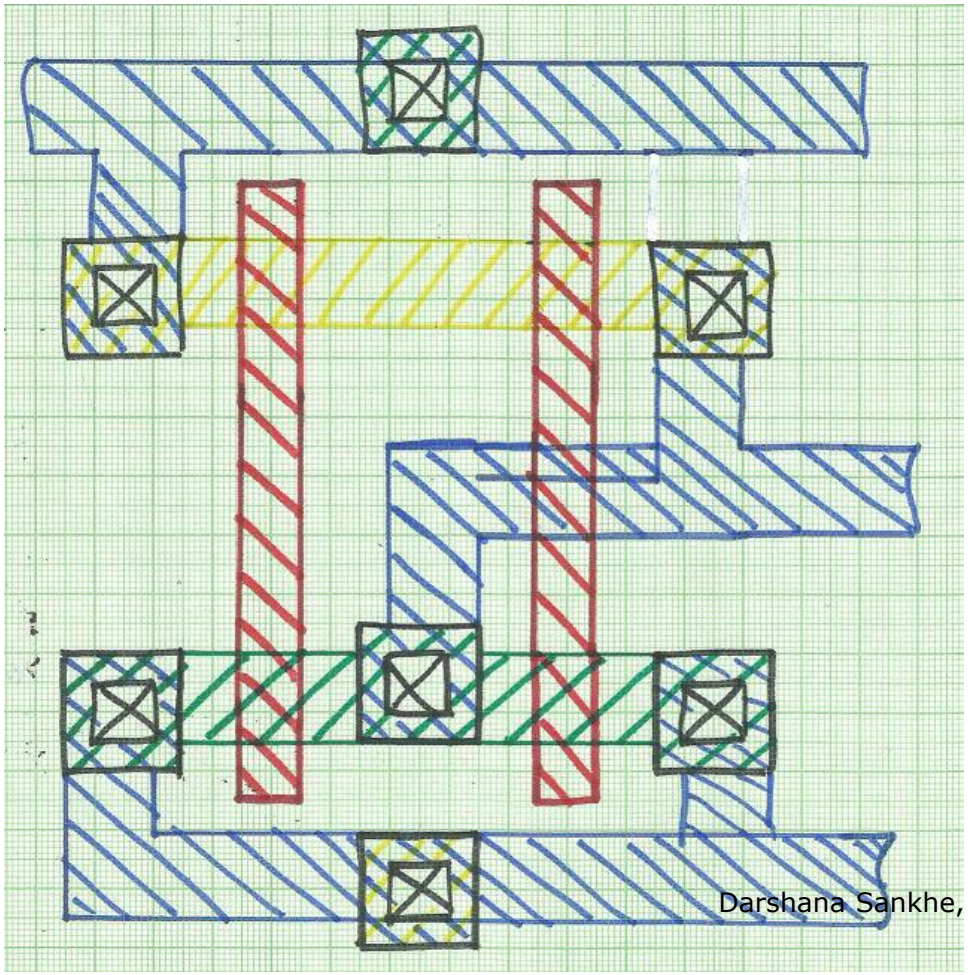






CMOS NOR:





Design of NMOS/CMOS Circuits:

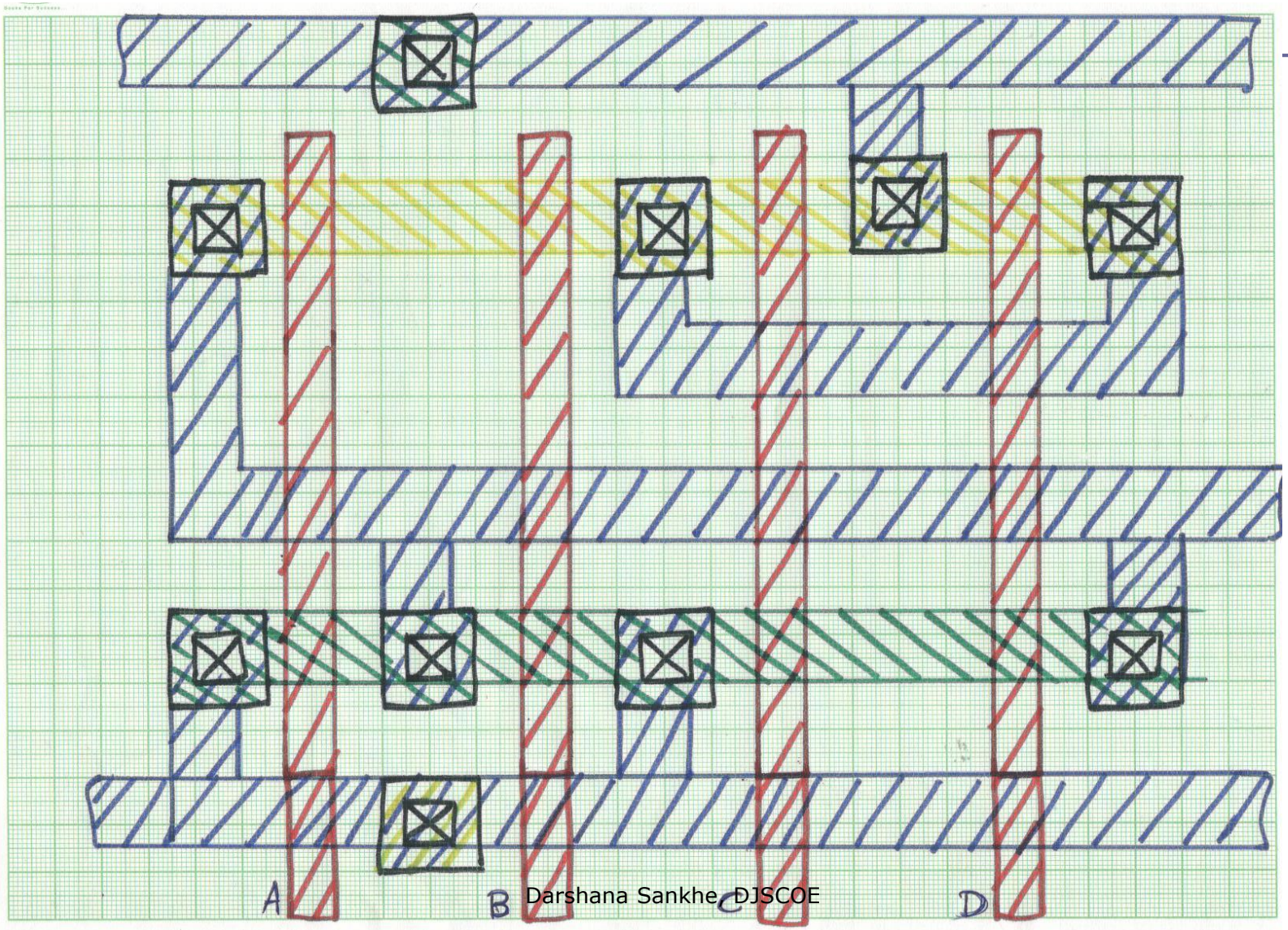
- PDN – The Function to be implemented, must be expressed in a inverted form.

- $F = \overline{(A + BC)\, D}$

- $F = (AB + C)(D + E)$

- $\overline{F} = A + B + CD$

F’ = A + B + CD



Thank you