

Fabrication of carbon nanotube field-effect transistors with semiconductors as source and drain contact materials

Z. Xiao

Department of Electrical Engineering, Alabama A&M University, Normal, AL 35726
F. E. Camino

Center for Functional Nanomaterials, Brookhaven National Laboratory, Upton, NY 11973

Proposal Title

Fabrication of single-walled carbon nanotube field-effect transistors.

Research Achievement

Common problems in the fabrication of carbon nanotube field effect transistors (CNTFETs) include the positioning of tubes across electrodes and poor device electrical performance due to the presence of metallic nanotubes intermixed with semiconducting ones. To circumvent these problems, in this work dielectrophoresis has been used for tube alignment, while semiconducting electrodes have been employed to selectively turn off metallic nanotubes resulting in improved device electrical characteristics.

Research on how to achieve higher drain-source current (I_{DS}) on/off ratio and better I_{DS} saturation properties in CNTFETs is interesting due to the good prospect of these devices for nanoelectronic applications [1, 2]. However, the yield for good device performance is low because currently there is no effective way to separate metallic carbon nanotubes, which shunt FET characteristics, from semiconducting tubes, which are the active elements of the device. To solve this issue, semiconducting electrodes (Sb_2Te_3 or Bi_2Te_2Se) were used instead of metal electrodes in CNTFETs. This substitution allows to selectively isolate metallic nanotubes due to the current-blocking action produced by the back-to-back metal–semiconductor junctions formed at the interfaces between semiconducting electrodes and metallic nanotubes. Measurements indicate that this electrode material substitution results in improved device performance.

In this research, ultra-purified SWCNTs from Carbon Nanotechnologies, Inc. were used for the fabrication of CNTFETs, and N-Methyl Pyrrolidone was used as the solvent for the dispersion of SWCNTs in solutions. Fig. 1 shows a flow diagram of the fabrication process of CNTFETs with Sb_2Te_3 –SWCNT or Bi_2Te_2Se –SWCNT source/drain contacts.

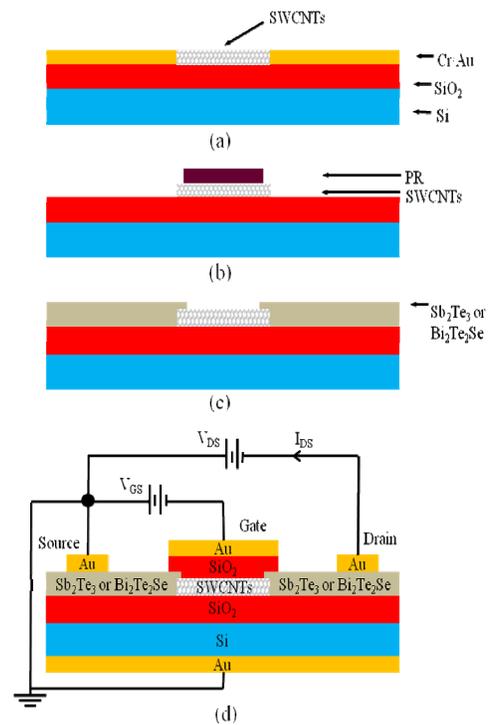


Fig. 1. Flow diagram of the main steps in the device fabrication process. (a) Alignment of SWCNTs to a pair of gold electrodes via dielectrophoresis. (b) Etching away of gold electrodes with the interelectrode region protected by photoresist (PR). (c) Deposition of Sb_2Te_3 or Bi_2Te_2Se layer followed by PR lift-off to define semiconducting contacts to SWCNTs. (d) Final device after the deposition of gate oxide and the formation of metal contacts.

Fig. 2 shows a scanning electron micrograph (SEM) of SWCNTs aligned onto a pair of gold electrodes using the dielectrophoresis process. Figs. 3 and 4 shows I_{DS} - V_{DS} curves at several gate voltages (V_{GS}) for a CNTFET fabricated using Sb_2Te_3 and Bi_2Te_2Se as source and drain contact material, respectively. CNTFETs have PMOS-like electrical properties. The CNTFET with Sb_2Te_3 -SWCNT contacts has an I_{DS} ratio of about 5000 at $V_{DS} = -3V$. The CNTFET with Bi_2Te_2Se -SWCNT contacts has an I_{DS} ratio of about 2000 at $V_{DS} = -1V$. Both CNTFETs have higher V_{DS} starting the deviation from their switch-off status compared to CNTFETs fabricated with metal-SWCNT source/drain contacts [1]. The CNTFET with Sb_2Te_3 -SWCNT source/drain contacts (Fig. 3) also shows a good saturation I_{DS} with increasing V_{DS} . The fabrication processes developed in this research can be applied to other semiconductor electrode materials and could be employed in future wafer-scale CNTFET-based nanoelectronic circuits.

Future Work

As a continuation of this work, we plan to define submicron gates within the interelectrode region using the ion beam assisted deposition capability of the dual electron/ion beam system at the Center for Functional Nanomaterials. We also plan to use this tool for the fabrication of single-tube CNTFETs. In addition, wafer-scale fabrication of CNTFET-based nanoelectronic circuits with semiconductor contact materials using the dielectrophoresis technique will be explored.

References

- [1] Kang S J, Kocabas C, Ozel T, Shimi M, Pimparkar N, Alam M, Rotkin S and Rodger J A , **Nature** 2, 230 (2007).
- [2] LeMieux M C, Roberts M, Barman S, Jin Y W, Kim J M and Bao Z, **Science** 321, 101 (2008).

Publications

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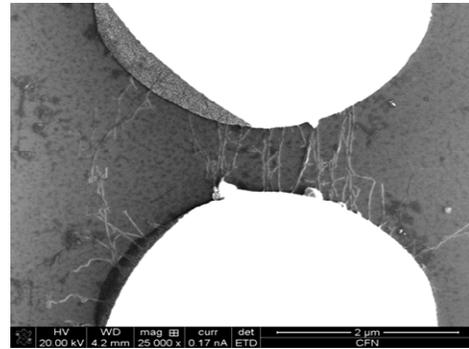


Fig. 2. SEM of SWCNTs aligned onto a pair of gold electrodes via dielectrophoresis.

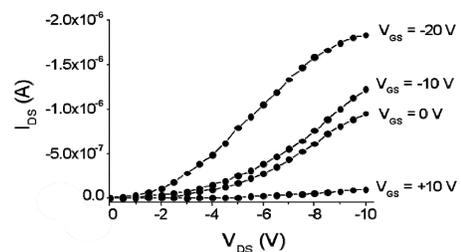


Fig. 3. Drain-source current (I_{DS}) versus drain-source voltage (V_{DS}) and gate voltage (V_{GS}) for the CNTFET fabricated with Sb_2Te_3 -SWCNT source/drain contacts.

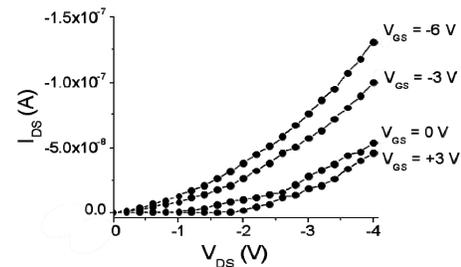


Fig. 4. Drain-source current (I_{DS}) versus drain-source voltage (V_{DS}) and gate voltage (V_{GS}) for the CNTFET fabricated with Bi_2Te_2Se -SWCNT source/drain contacts.