

# Fabrication Processes :

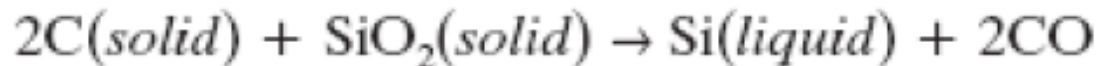
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- Refining of Si
- Crystal growth and wafer preparation
- Epitaxy
- Deposition
- Oxidation
- Diffusion
- Ion Implantation
- Lithography
- Etching
- Metallization

# Refining of Si :

## Raw Material and Purification

- Raw Material – Quartzite  $\text{SiO}_2$
- Convert Quartzite into metallurgical grade silicon or (MGS)
  - Furnace with quartzite and carbon (coal or coke) @ 2000 °C
  - ~ 98% pure



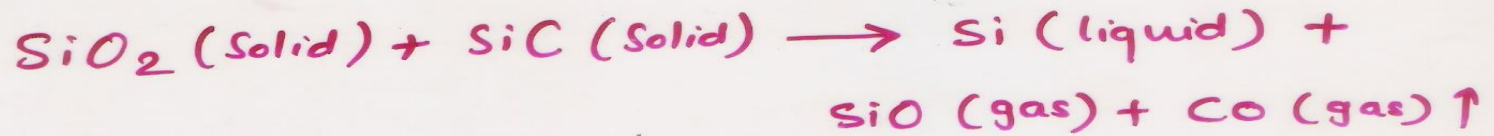
- MFGS converted to electronics grade silicon (EGS)
  - MGS powder combined with gaseous HCl
  - Produce  $\text{SiH}_4$  (silane),  $\text{SiH}_3\text{Cl}$  (chlorosilane),  $\text{SiH}_2\text{Cl}_2$  (dichlorosilane),  $\text{SiHCl}_3$  (trichlorosilane), or  $\text{SiCl}_4$  (silicon tetrachloride)

# Raw Material and Purification (2)

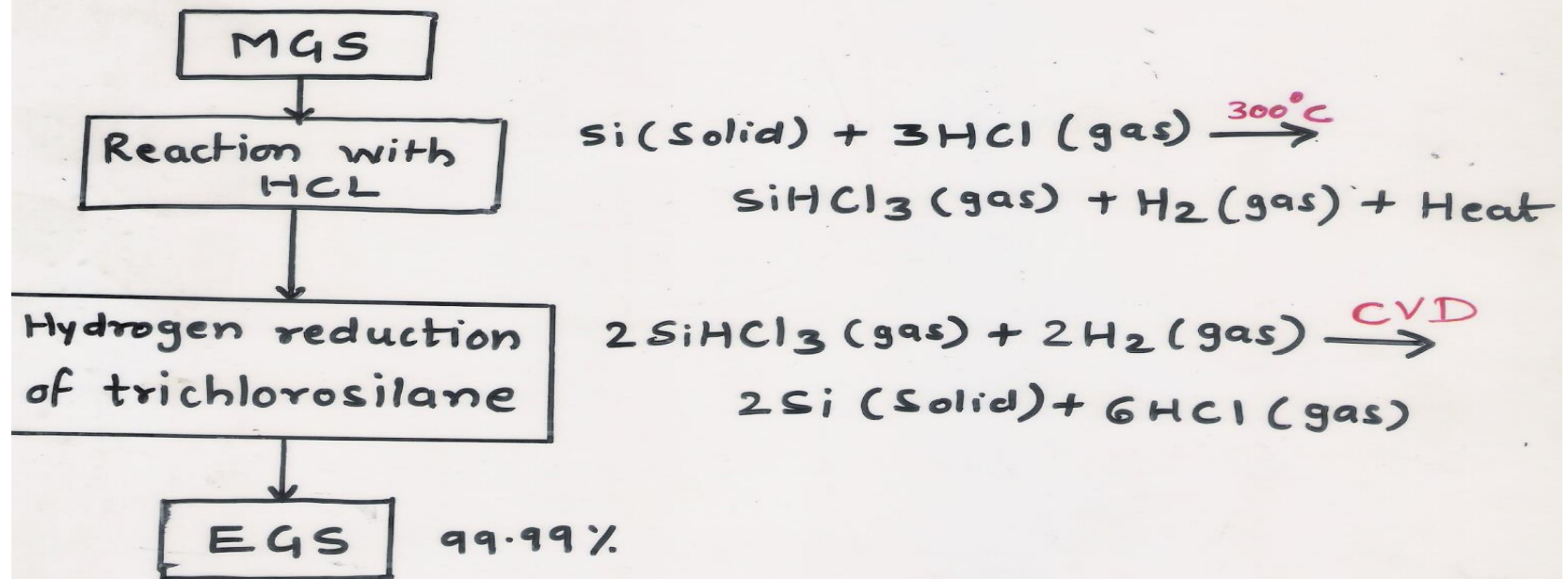
- $\text{SiHCl}_3$  (trichlorosilane) processing
  - Room temperature liquid that can be purified using fractional distillation. Boiled and condensed back into a liquid.
- Chemical vapor deposition
  - $\text{SiHCl}_3$  (gas) and hydrogen (gas) with Si rod
$$2\text{SiHCl}_3(\text{gas}) + 2\text{H}_2(\text{gas}) \rightarrow 2\text{Si}(\text{solid}) + 6\text{HCl}(\text{gas})$$
  - Deposition of polysilicon (parts per billion purity)  
 $10^{13}$  to  $10^{14}$   $\text{cm}^{-3}$  impurities
- **Polycrystalline silicon is used for Crystal Growth**

Refining of Silicon : silica and silicate

Natural source of Si — Sand or quartz.



MGS — Metallurgical Grade Si ; 98% pure.



Consumption of EGS —  $5 \times 10^6$  kg. per year.

# Crystal growth :

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- Growing of single crystal Si from fine granules of Si (EGS) under controlled doping of impurities at a temperature  $\geq 1000^{\circ}\text{C}$
- Impurities added to Si are
  - P type Si – Boron ( $\text{B}_2\text{H}_6$  i.e. diborane )
  - N type Si – phosphorous ( $\text{PH}_3$  i.e. phosphene)
  - Doping concentration –  $10^{15}$  to  $10^{16}$  / $\text{cm}^3$

# Crystal growth Techniques:

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- Czochralski Growth (CZ Growth)
- Float Zone Growth (FZ Growth)
- Bridgman Growth for GaAs

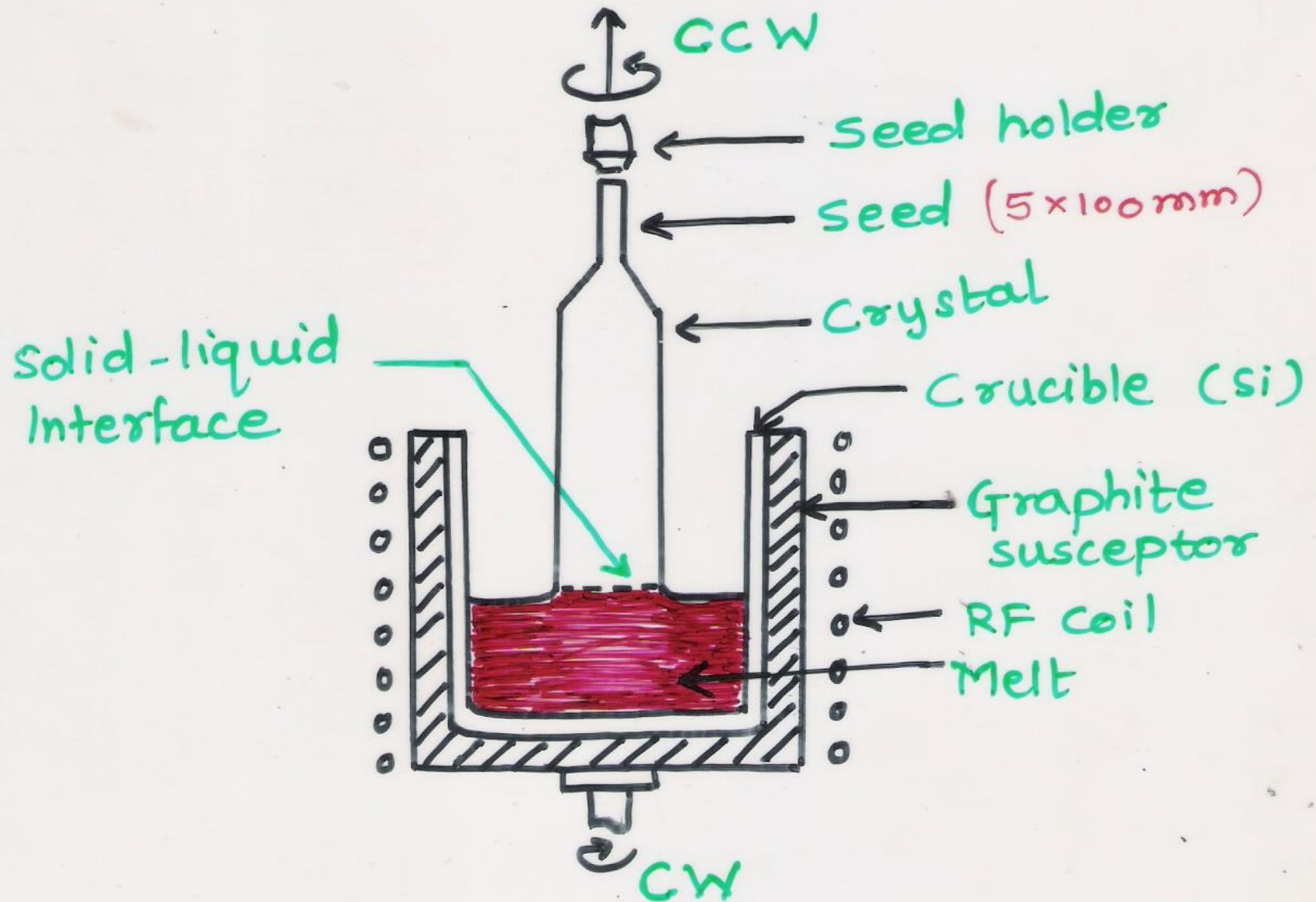
# Czochralski Growth (CZ Growth)

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- CZ Process – Subsystems
  - Furnace
  - Crystal pulling system
  - $\mu\text{p}$  based Control system
    - Temperature, speed of rotation, pull rate, flow rate, crystal dimensions, gas source and exhaust system....

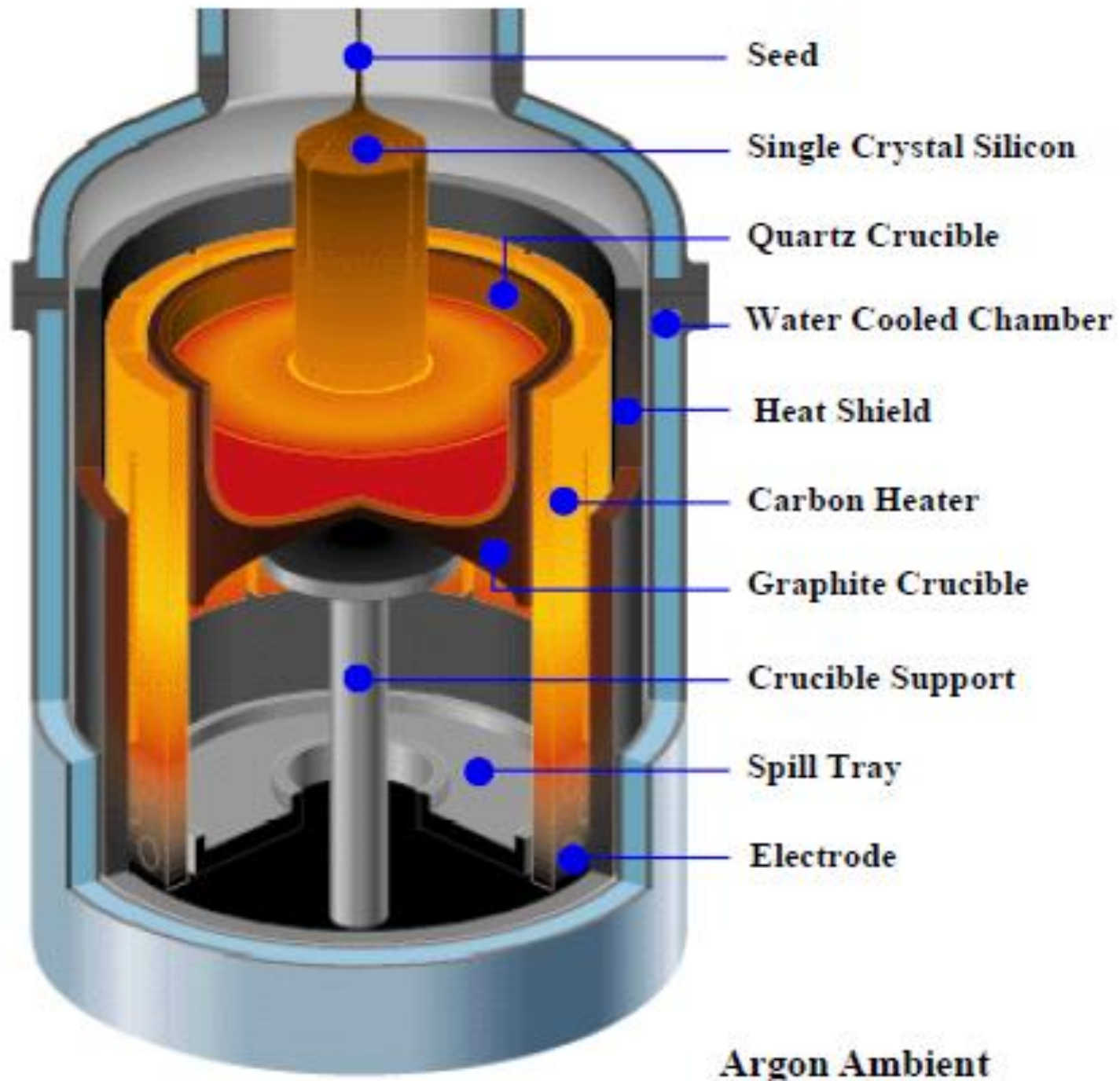
**Essentially all Si wafers used for ICs today come from Czochralski (cho-HRAL-skee) grown crystals.**

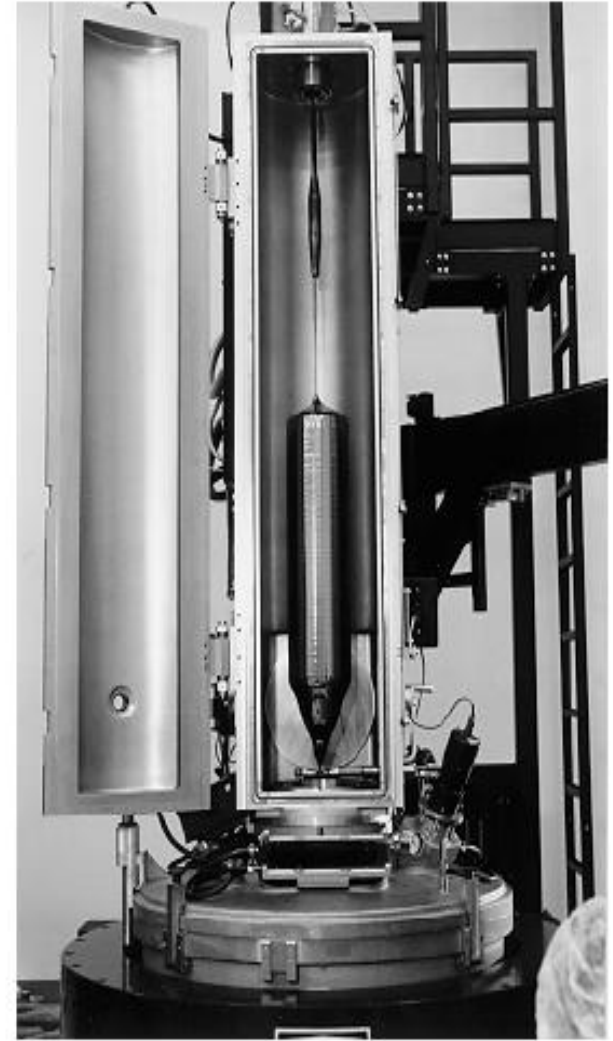
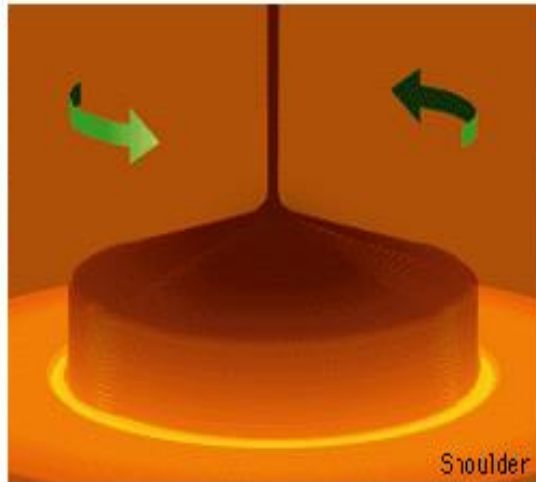
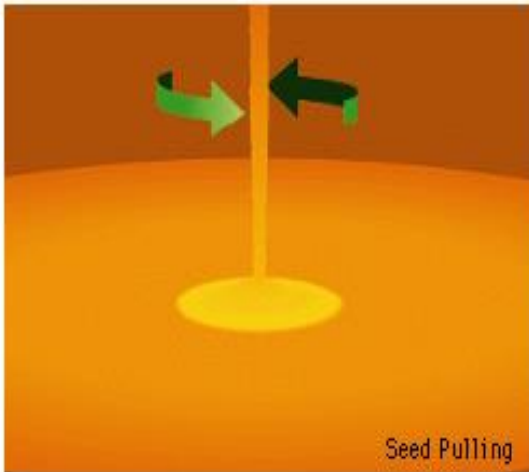
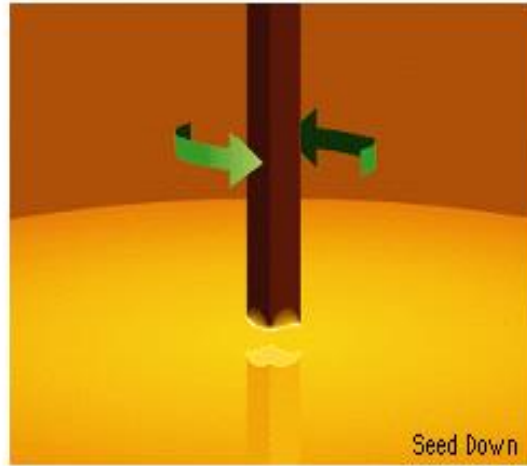
# CZ Process (Czochralski)







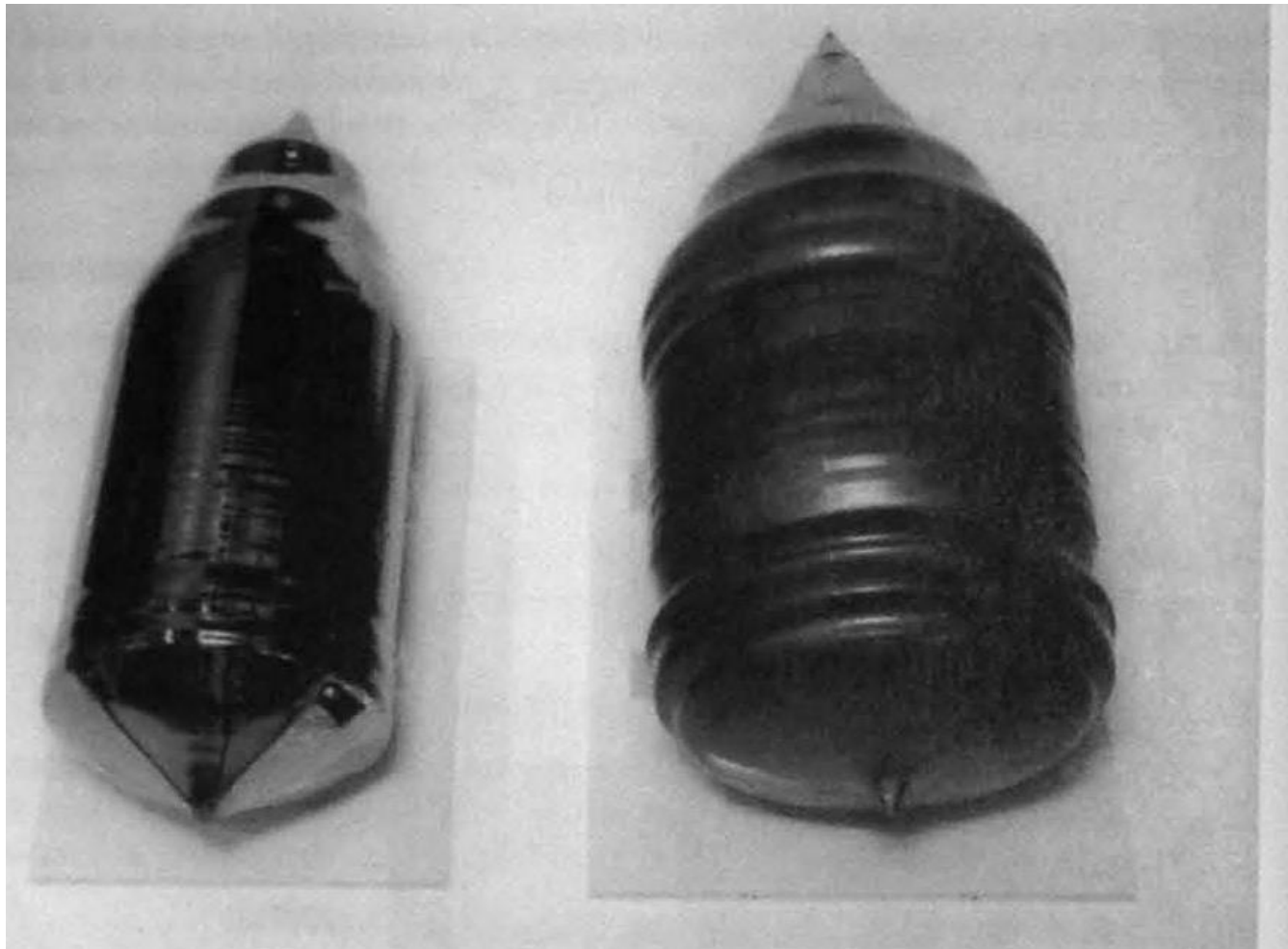




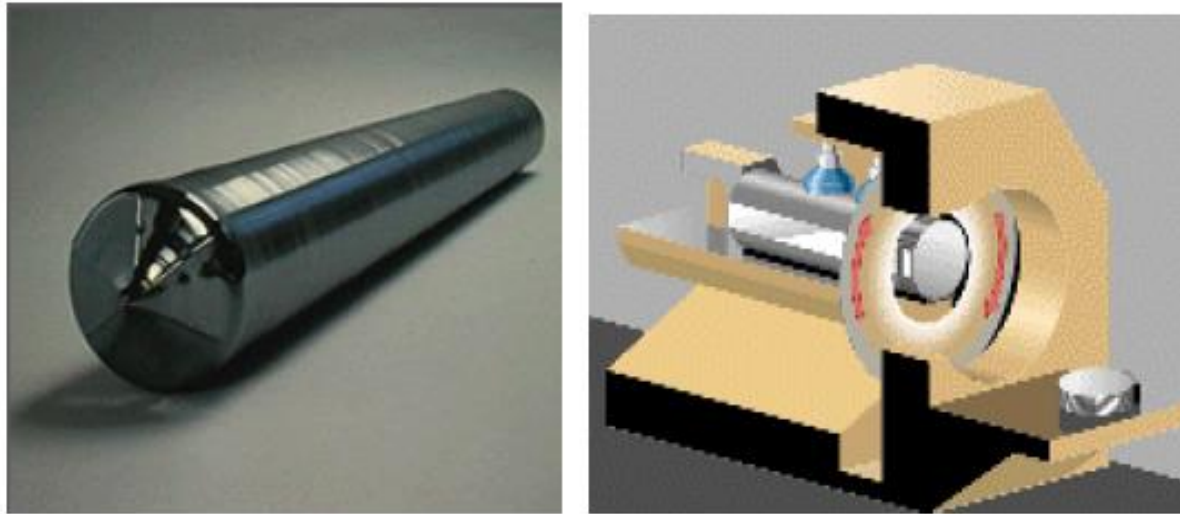
(More information on crystal growth at <http://www.memc.com>)

# CZ Grown Si Ingot :

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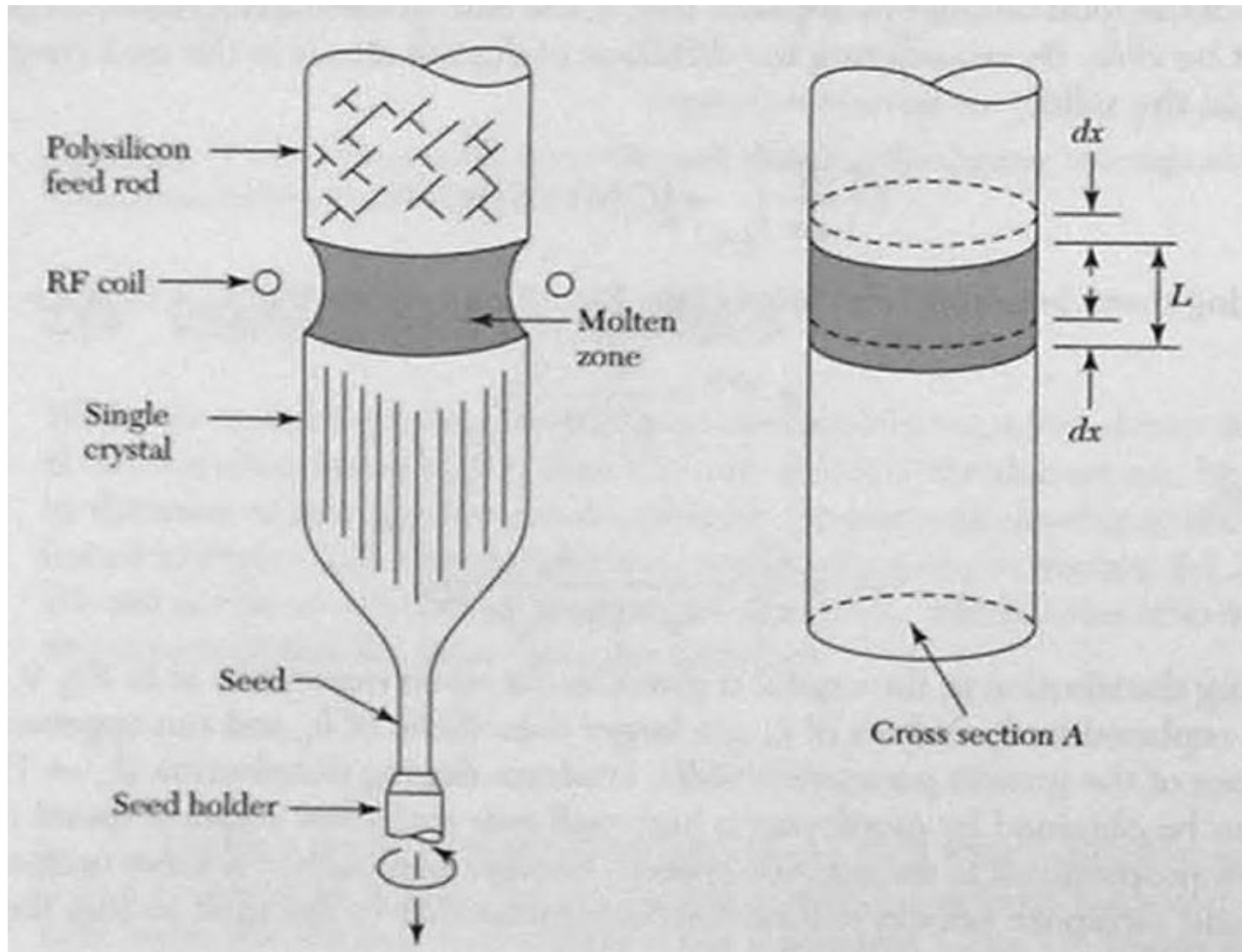


# Ingots Cutting into Wafers

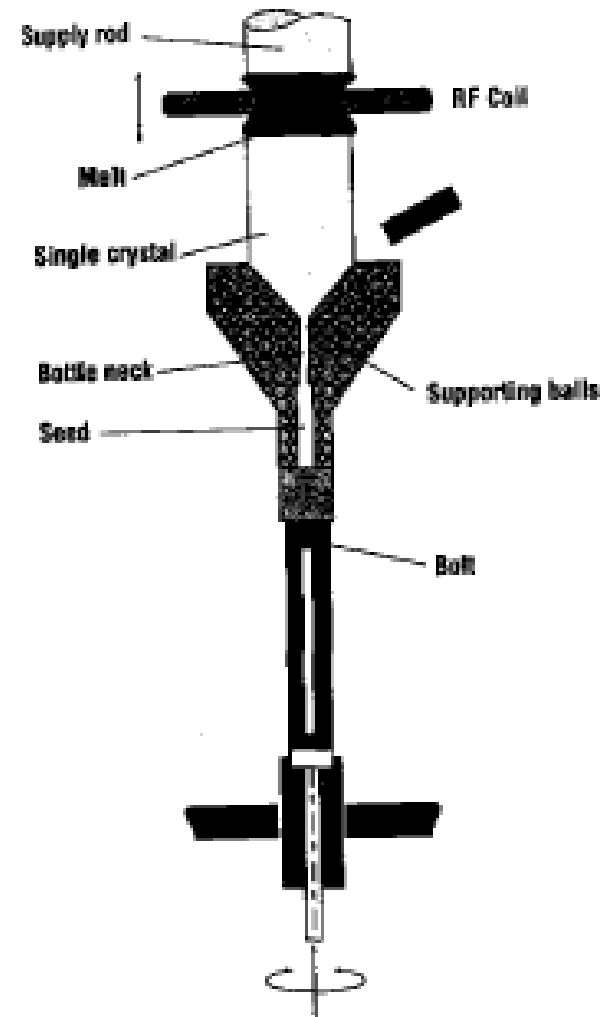
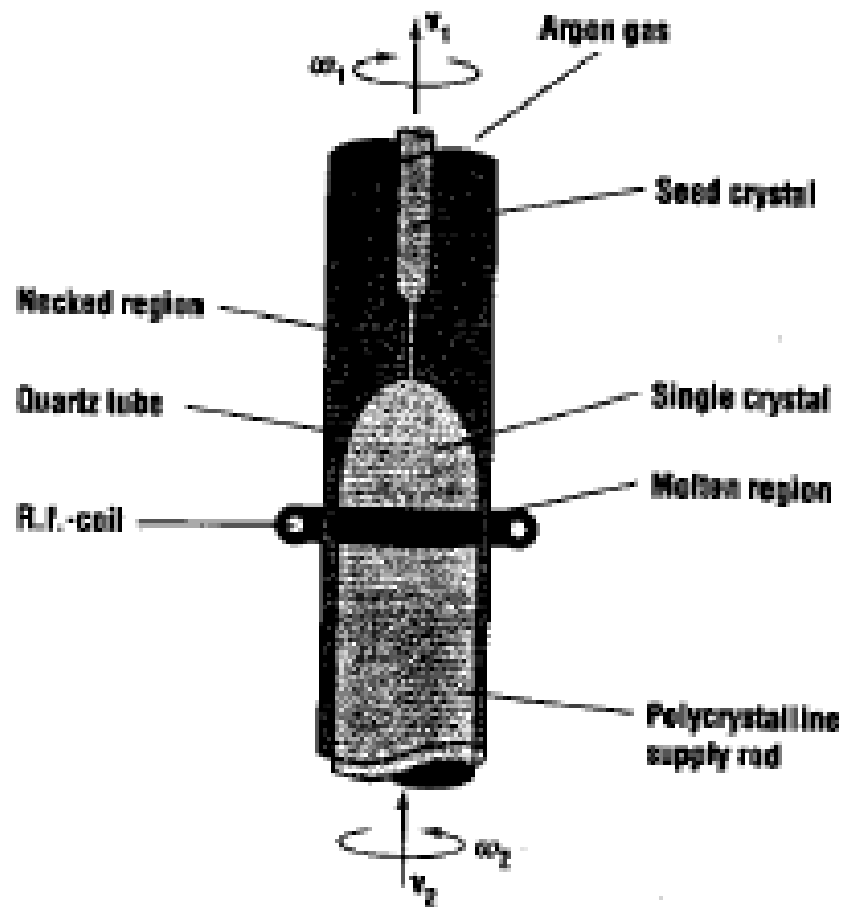


**After crystal pulling, the boule is shaped and cut into wafers which are then polished on one side.**

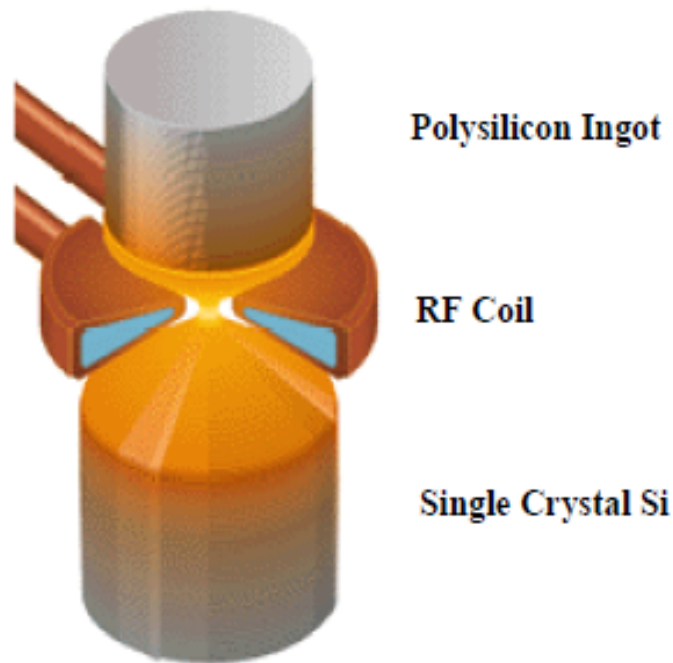
# Float Zone Growth (FZ Growth)



# Float Zone Growth (FZ Growth)



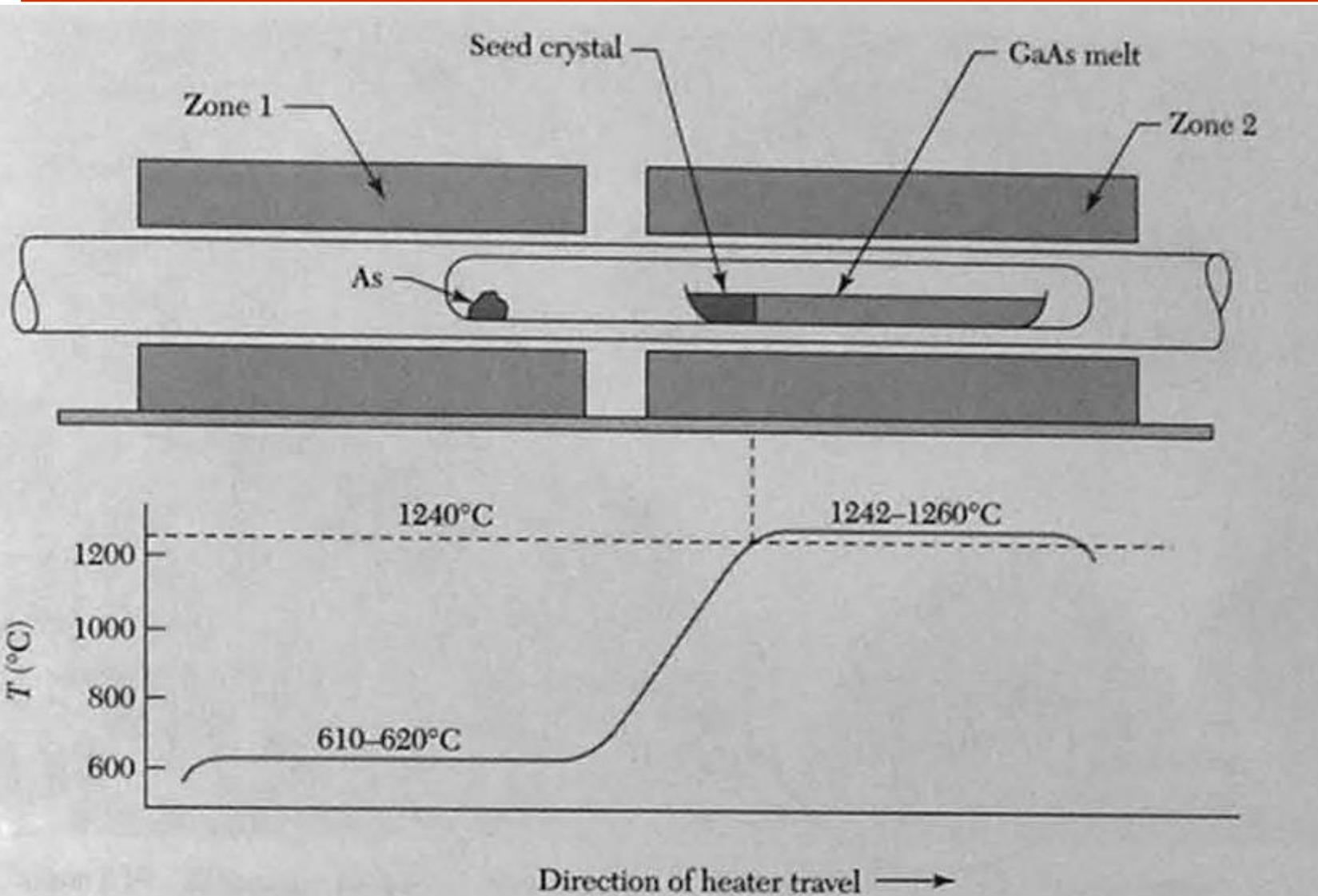
# Float Zone Crystal Growth



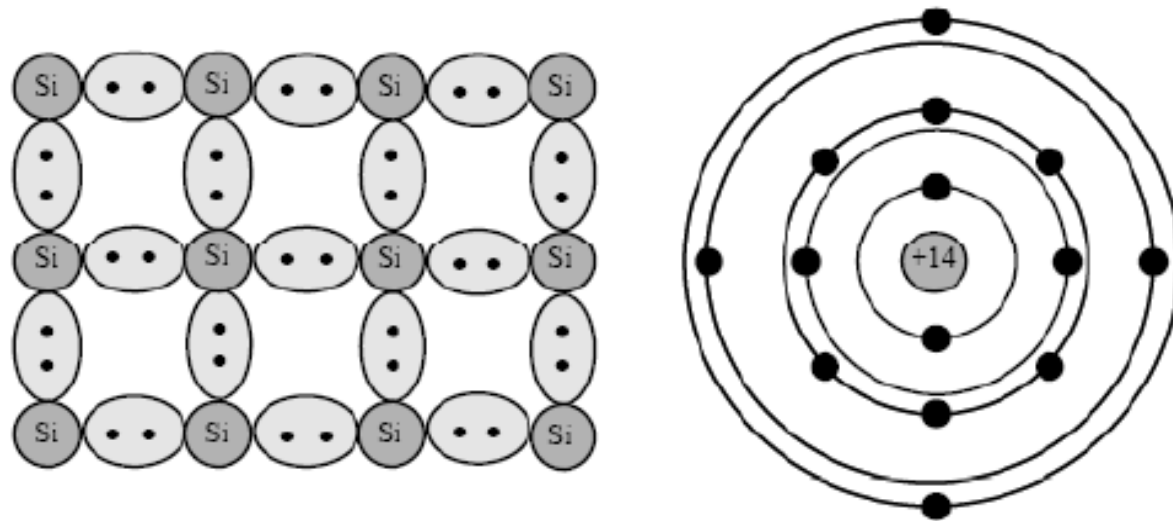
- An alternative process is the float zone process which can be used for refining or single crystal growth.
- Localized  $I^2R$  heating via RF Coil
  - Nitrogen or dopant ambient
- Wafers < 150 mm
  - Detectors and power
  - Doping is a challenge
  - Reduced C and O impurities
- Bottom in contact with single crystal seed



# Bridgman Growth for GaAs :



# Silicon as a Material



**Figure 1-13** Simple representation of silicon atoms bonded in a crystal (left). The dotted areas are covalent or shared electron bonds. The electronic structure of a single Si atom is shown conceptually on the right. The four outermost electrons are the valence electrons that participate in the covalent bonds.

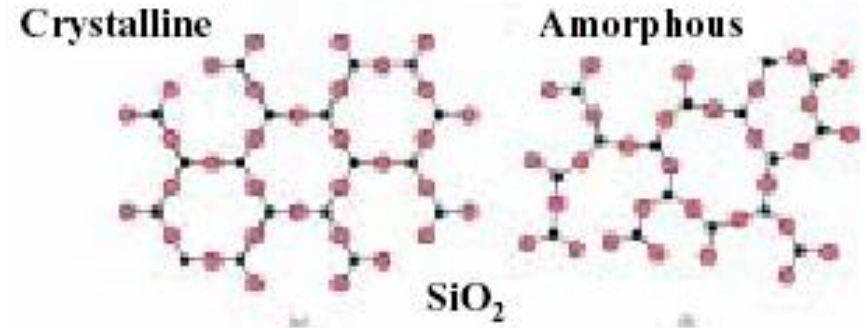
- Silicon
  - Atomic model
    - Electron orbits 2-8-4, outer orbit half filled
  - Crystal lattice
    - Covalent bound each (share electron) with 4 other Si atoms
    - Stable, high impedance (poor conductor)

- **Intrinsic Semiconductors**
  - Column 4 atoms in a lattice (Si, Ge)
- **Compound Semiconductors**
  - Column 3-5 atoms (GaAs, InP)
  - Column 2-6 atoms (CdS, CdSe, CdTe, ZnO)
- **Dopants**
  - Replace an intrinsic atom with one that has additional or fewer electrons in outer orbit
  - For Silicon:
    - Fewer electrons: B
    - More Electrons: P or As

# Types of Solids:

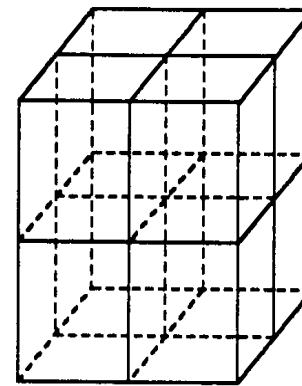
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- ❑ **Crystalline material:** atoms self-organize in a periodic array
- ❑ **Single crystal:** atoms are in a repeating or periodic array over the entire extent of the material
- ❑ **Polycrystalline material:** comprised of many small crystals or **grains**
- ❑ **Amorphous:** lacks a systematic atomic arrangement

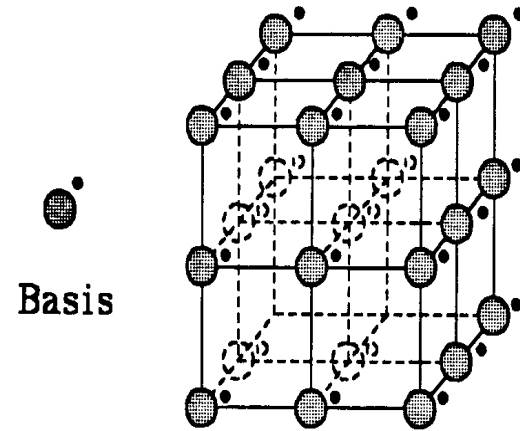


# Crystal structure:

- To discuss crystalline structures it is useful to consider atoms as being hard spheres with well-defined radii.
- In this hard-sphere model, the shortest distance between two like atoms is one diameter.
- We can also consider crystalline structure as a lattice of points at atom/sphere centers.



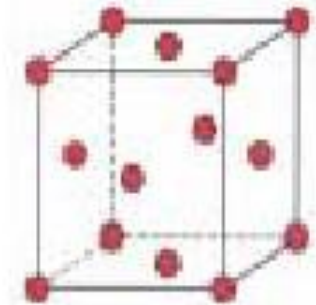
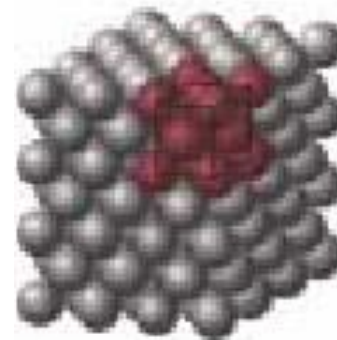
Lattice



Basis

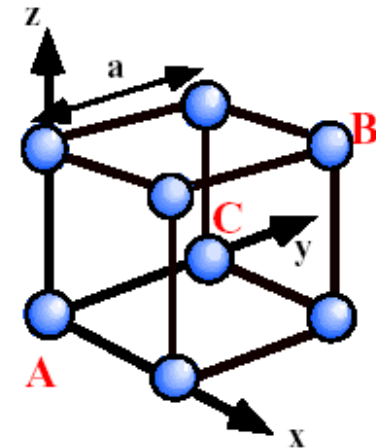
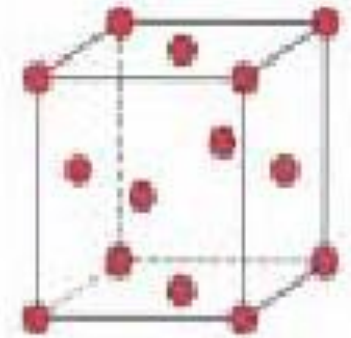
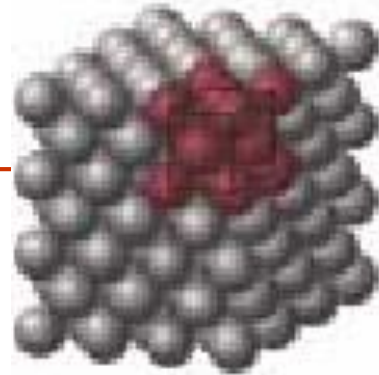
Crystal

Fig. 1.3 Lattice + basis = crystal structure.



# Unit Cell :

- The unit cell is the smallest structural unit or building block that can describe the crystal structure.
- Repetition of the unit cell generates the entire crystal.
- Example: 2D honeycomb net can be represented by translation of two adjacent atoms that form a unit cell for this 2D crystalline structure
- Different choices of unit cells possible, generally choose parallelepiped unit cell with highest level of symmetry

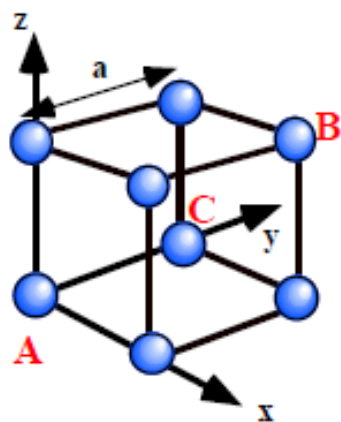


Cubic

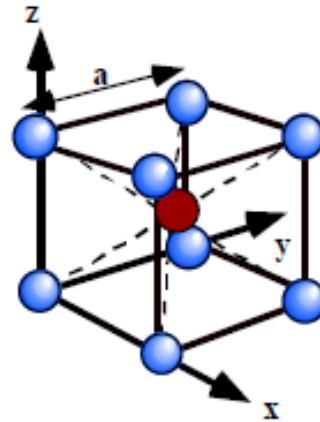
**Crystals are characterized by a unit cell which repeats in the x, y, z directions.**

# Silicon Structure Classification

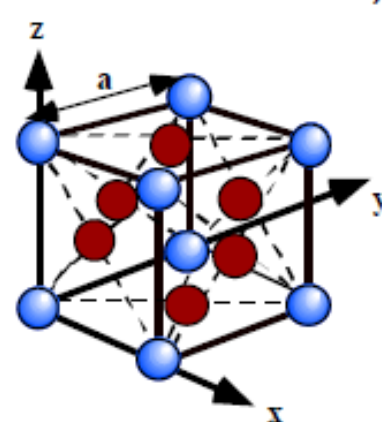
- Single Crystal – periodic arrangement of atoms
- Polycrystalline – small crystals of arbitrary alignment
- Amorphous Silicon – no significant ordering of atoms
  
- Simple Crystal Unit Cells
  - Cubic
  - Body-Centered Cubic (extra atom in the body)
  - Face-Centered Cubic (extra atoms centered on faces)



Cubic



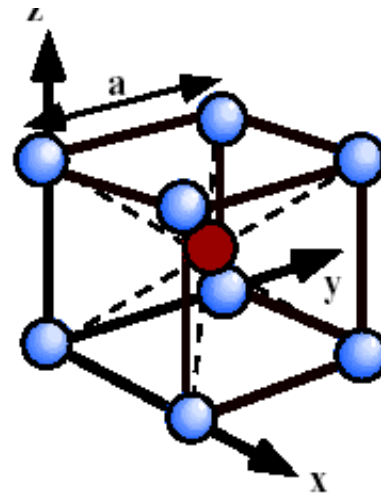
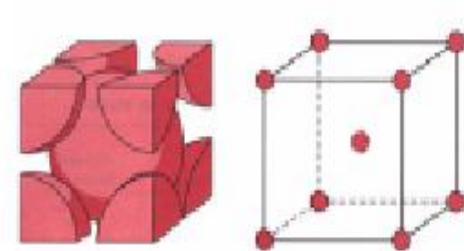
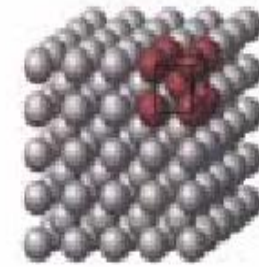
BCC<sup>3</sup>



FCC

# Body-Centered Cubic (BCC) Crystal Structure :

- Atom at each corner and at center of cubic unit cell
- Cr,  $\alpha$ -Fe, Mo have this crystal structure

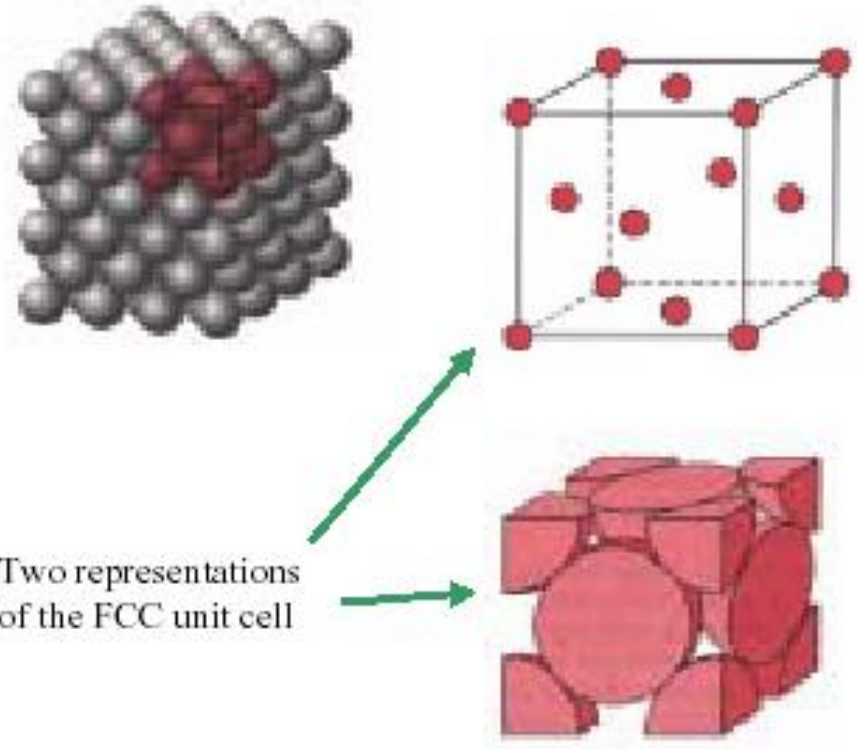
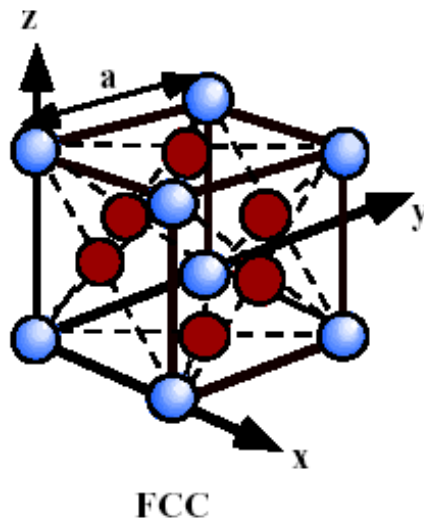


BCC



# Face-Centered Cubic (FCC) Crystal Structure

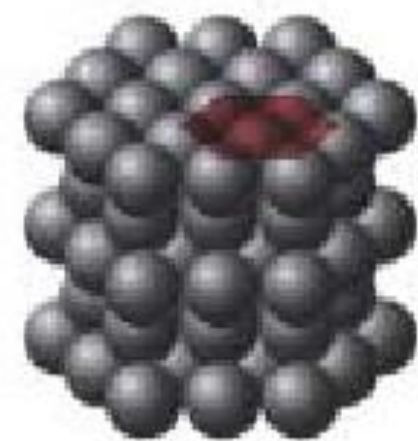
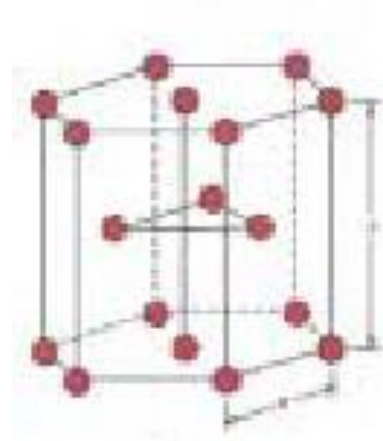
- Atoms are located at each of the corners and on the centers of all the faces of cubic unit cell
- Cu, Al, Ag, Au have this crystal structure



# Hexagonal Close-Packed Crystal Structure :

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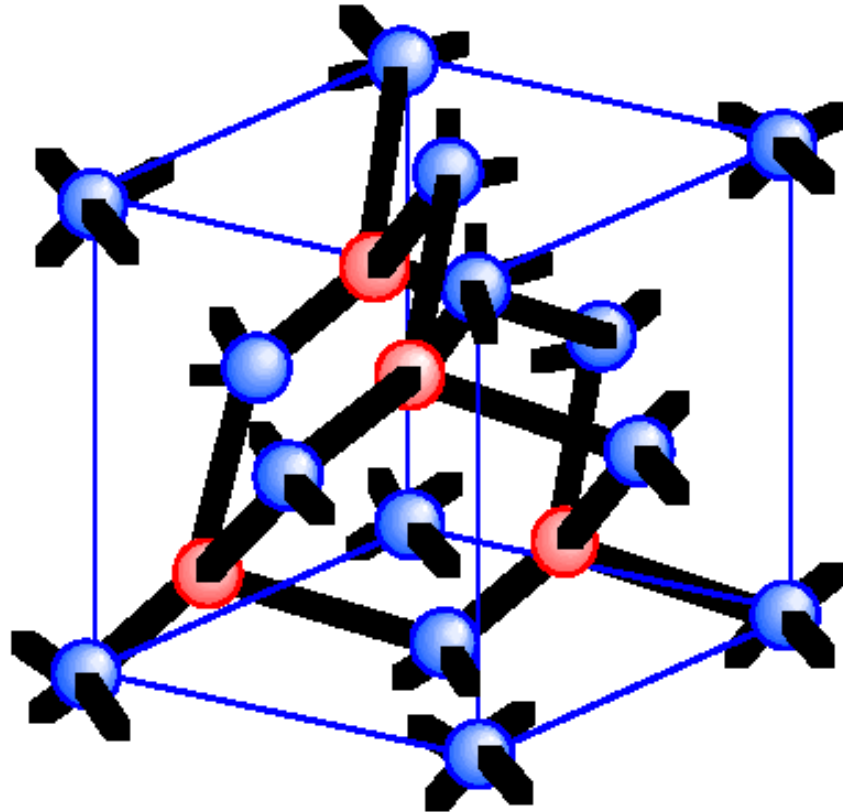
- HCP is one more common structure of metallic crystals
- Six atoms form regular hexagon, surrounding one atom in center. Another plane is situated halfway up unit cell (c-axis), with 3 additional atoms situated at interstices of hexagonal (close-packed) planes
- Cd, Mg, Zn, Ti have this crystal structure



# Basic diamond crystal structure

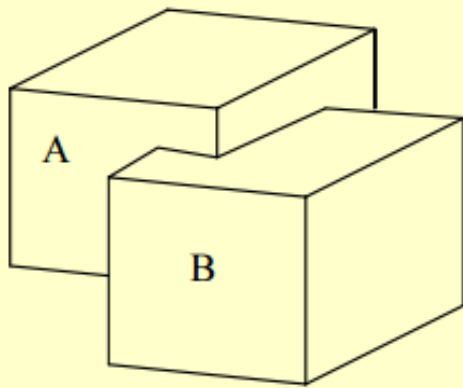
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- Silicon has the basic diamond crystal structure – two merged FCC cells offset by  $a/4$  in  $x$ ,  $y$  and  $z$ .

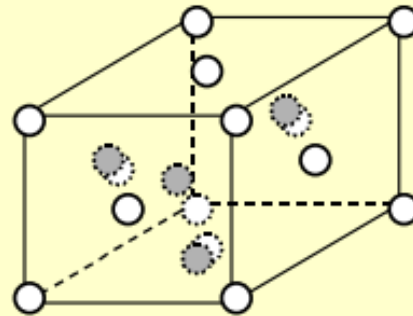


## Single Silicon Crystal Structure-Cont'd

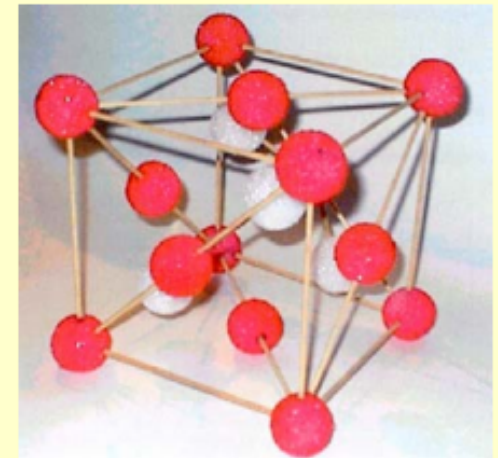
- Single crystal silicon, however has 4 extra atoms in the interior.
- The situation is like to merge two FCC crystals together as shown below:



(a) Merger of two FCC



(b) Merged crystal structure



- Total no. of atoms in a single silicon crystal = 18.
- The unsymmetrical distribution of atoms within the crystal make pure silicon anisotropic in its mechanical properties.
- In general, however, we treat silicon as an isotropic material.

## The 3 Distinct Planes of a Cubic Crystal

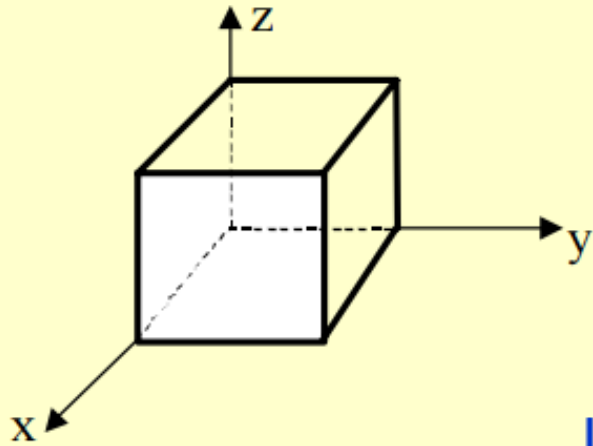


Figure A

Top face: Plane (001)

Right face: Plane (010)

Front face: **Plane (100)**

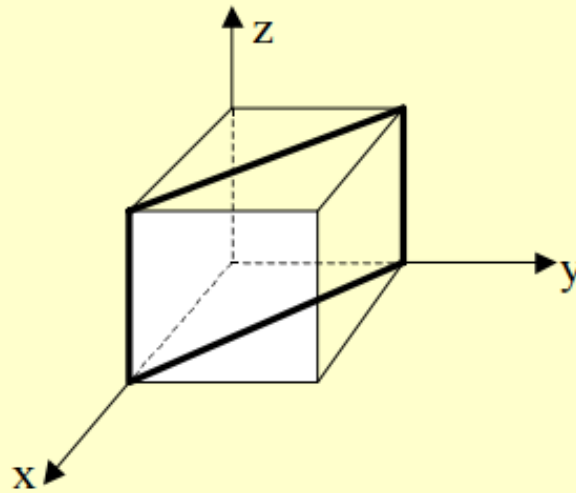


Figure B

Diagonal face: **Plane (110)**

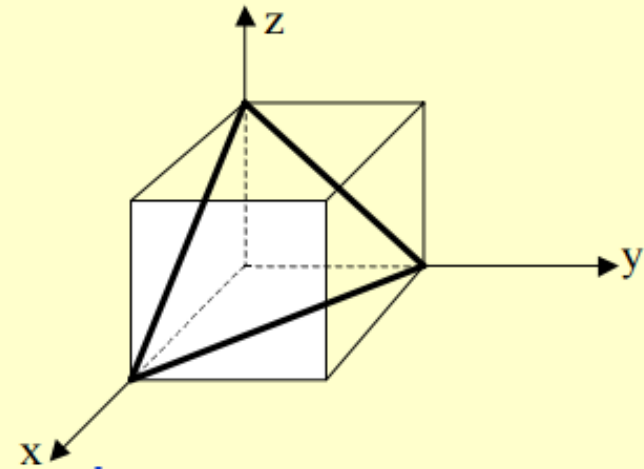
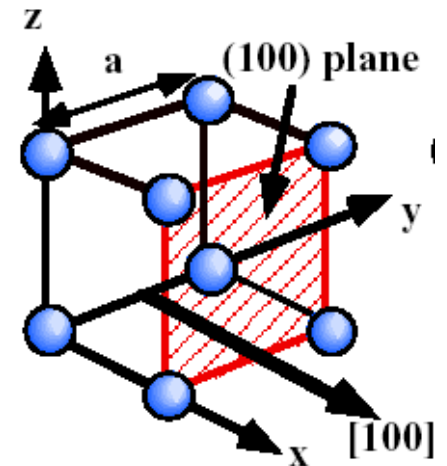
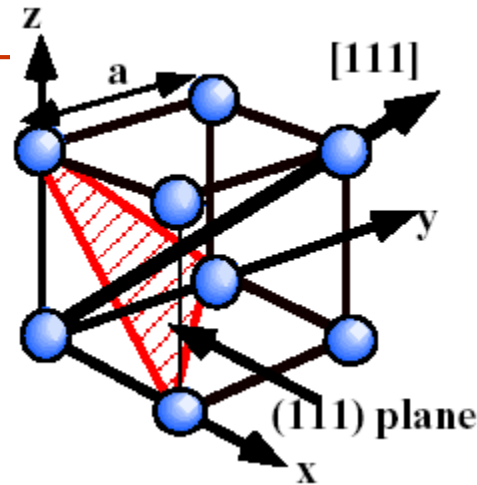


Figure C

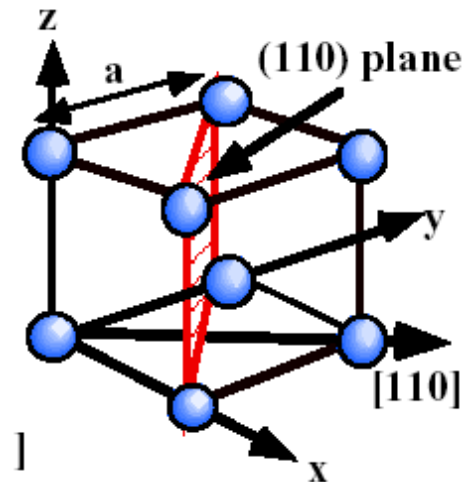
Incline face:  
**Plane (111)**

# Crystal Planes and directions :

- Planes and directions are defined using an x, y, z coordinate system.
- [111] direction is defined by a vector having components of 1 unit in x, y and z.
- Planes are defined by Miller-indices reciprocals of the intercepts of the plane with the x, y and z axes.



**{111} planes oxidize faster than {100} plan because the oxidation rate is Proportional to the number of silicon atom available for reaction.**



*{111} planes in silicon have a largest number of atom/cm-3  
{100} planes the lowest.*

# Defects in crystal :

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- ❑ Nothing in Nature is perfect, and crystals are no exception. Any real crystal contains defects, and these affect its properties in various ways.
- ❑ Defects in diamond alter the colour
- ❑ Defects in semiconductors (of the right kind) allow them to be used to make devices
- ❑ Defects in metals alter their **mechanical properties**
- ❑ Defects affect **thermal and electrical conductivity**.

# Beneficial & Detrimental(crystal defects)

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- Deep states are added to increase the resistivity ( $> 10^6 \text{ W-cm}$ ) of semiconductor material used as substrates (semi-insulating material). The best examples are GaAs:Cr and InP:Fe.
- GaP is an efficient emitter of light. The red light is observed if the crystal contains oxygen together with Zn or Cd. The light is green if GaP is doped with nitrogen and the yellow emission from GaP is obtained by Mg-O doping.
- An increase of switching frequency in silicon junction is obtained by added Gold as deep levels.
- Sensitizing Centers have a large capture cross section for minority carrier, and hence magnitude of photoconductivity, is greatly increased.
- *Thus deep levels are essential for the designing of devices and for their efficient performance.*
- Deep levels may increase the leakage current of devices and also deteriorate the efficiency of photovoltaic.



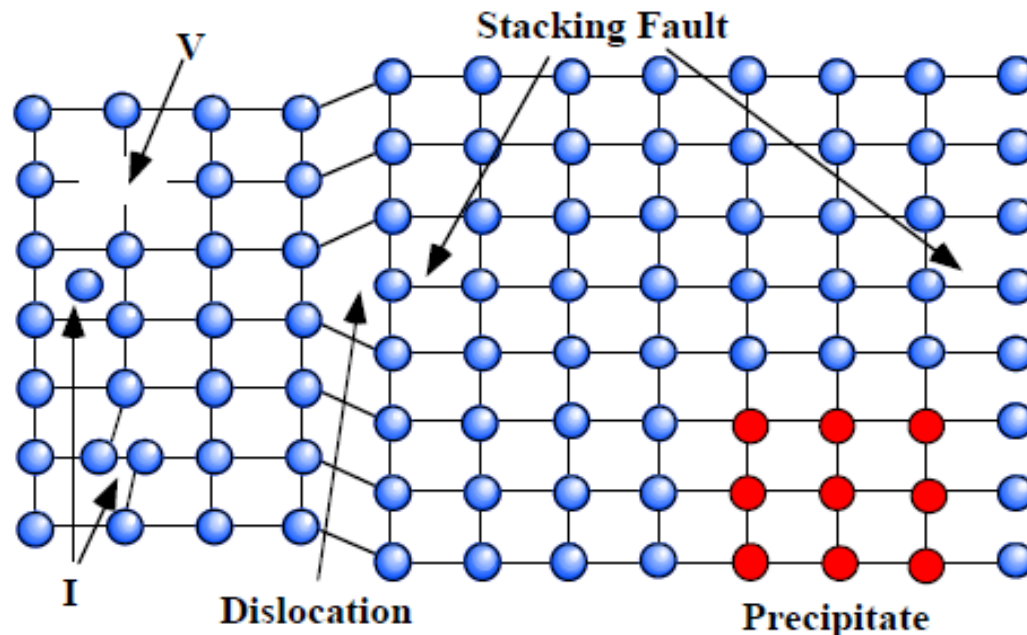
# Defects in Crystals

- Various types of defects can exist in crystal (or can be created by processing steps. In general these are detrimental to device performance.

Linear Defects:  
Dislocation due to  
high stress or rapid  
thermal gradients

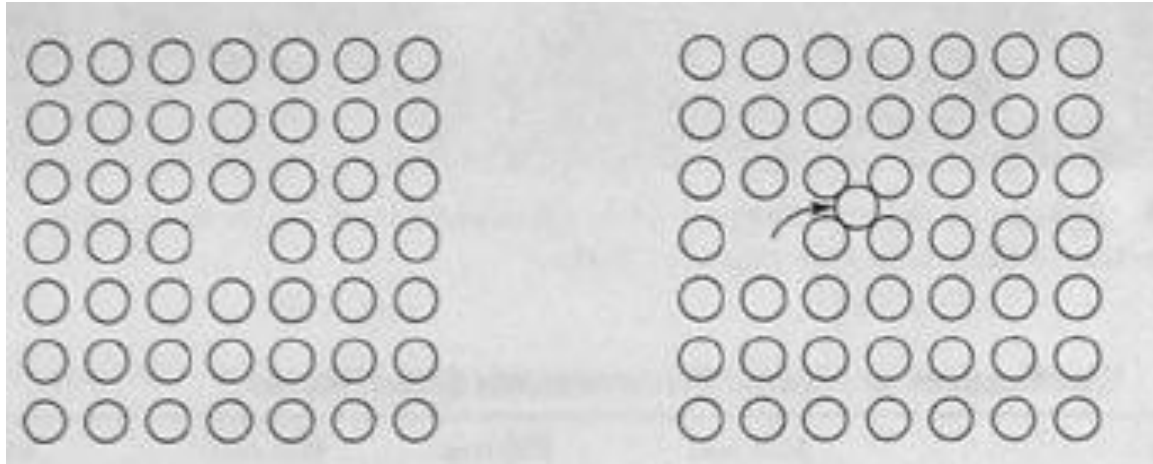
Volume Defects:  
Agglomeration of point  
defects  
Precipitate of dopants

Point Defects:  
V missing/vacancy  
I extra atom/interstitialcy



# Point Defects :

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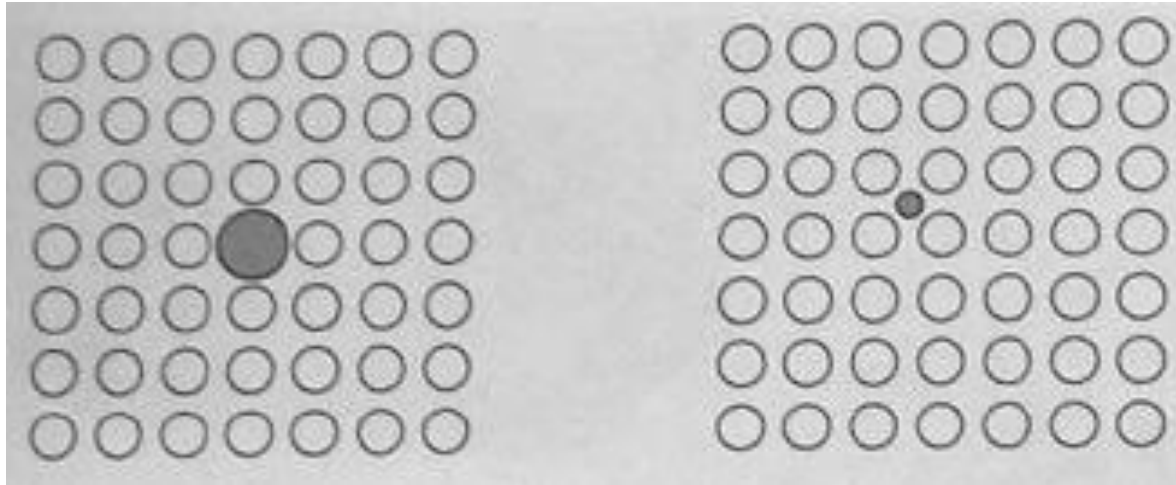
**Lattice  
Vacancy**

**Frenkel-Type  
Defect**

An atom is removed from its regular lattice site; the defect is a *vacancy*.

# Crystal Defects : Point Defects

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## **Substitutional Impurity**

An atom is in a site different from a regular lattice (substitutional) lattice site; the defect is an *interstitial*.

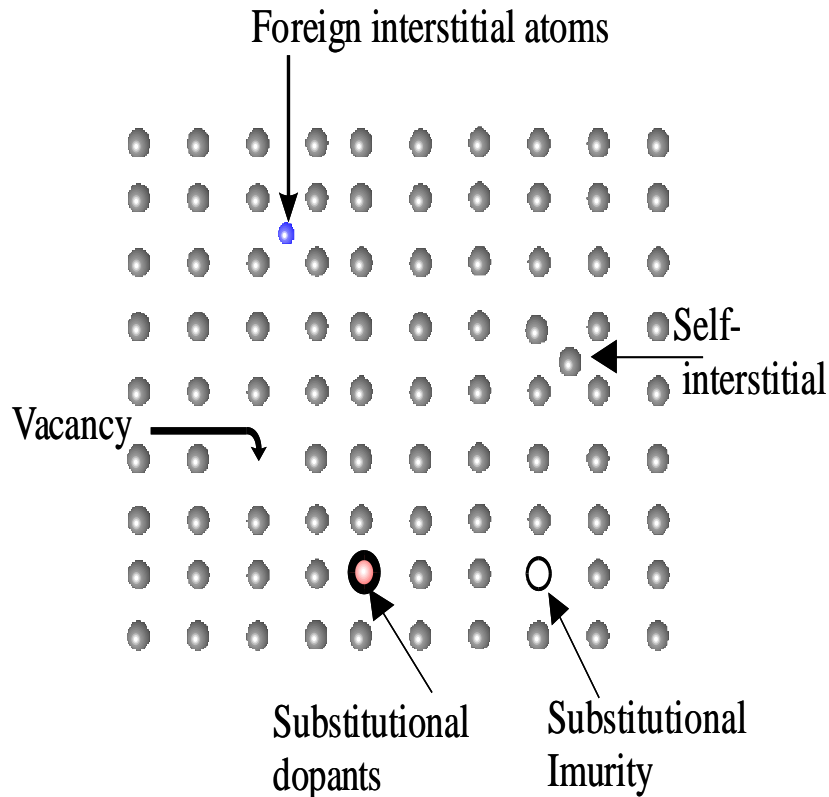
## **Interstitial Impurity**

An interstitial defect can be of the same species as the atoms of the lattice (it is an intrinsic defect, the *self-interstitial*) or of a different nature (it is then an extrinsic defect, an interstitial impurity).

An impurity occupies a substitutional site.

# Point defects in semiconductors

A *point defect* in a crystal is an entity that causes an interruption in the lattice periodicity.

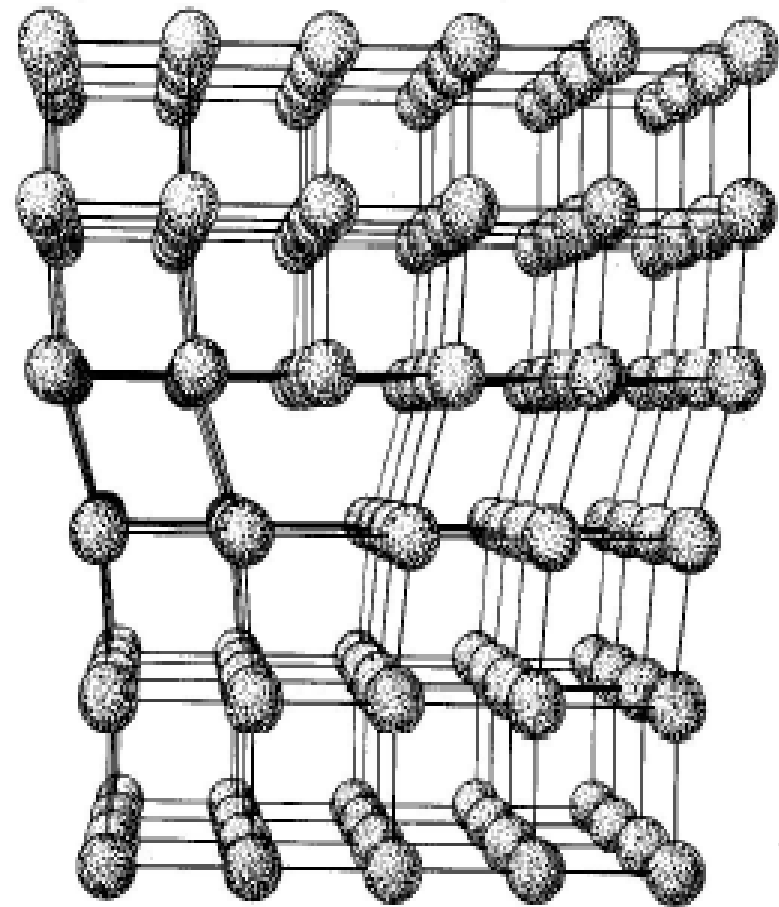


*Point defects play critical role in impurity diffusion and in ion implantation.*

# Line Defects

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- They extend in one Dimension
- Dislocations are More common line defects.
- In this an extra line of atoms is inserted in between of two other line o atoms.
- Simplest type of dislocation is edge detection: In this an extra plane is terminated on one end by the edge of crystal.
- Affects: Create Stress. The bonds just before the insertion of extra plane are stretched and bonds just after the plane are compressed.
- Sources:  
by stress due to temperature gradient  
agglomeration of point defects

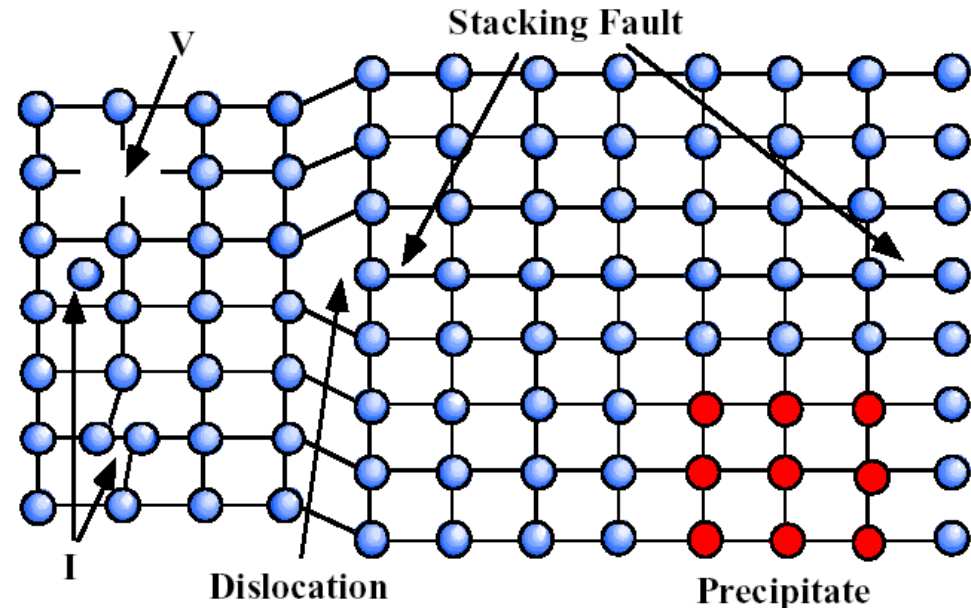


# 2D or Area Defect

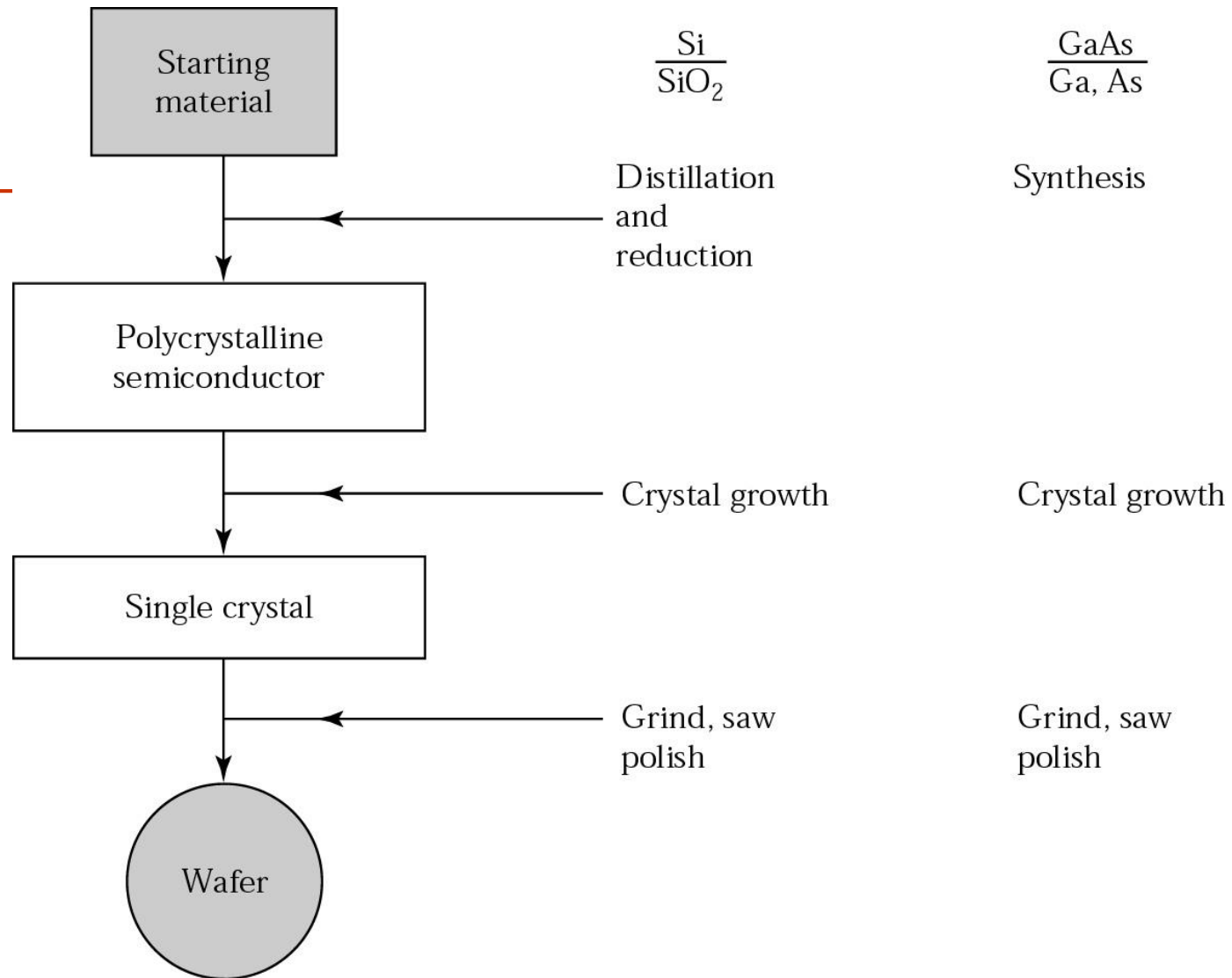
**Stacking Fault:** Extra planes of atoms. In this, the pattern is disrupted in two dimensions and is only regular in the third.

They are terminated by the edge of the crystal or by dislocation line.

**Precipitate:** Bulk defect, irregular in all dimensions. Gathering of impurity defects

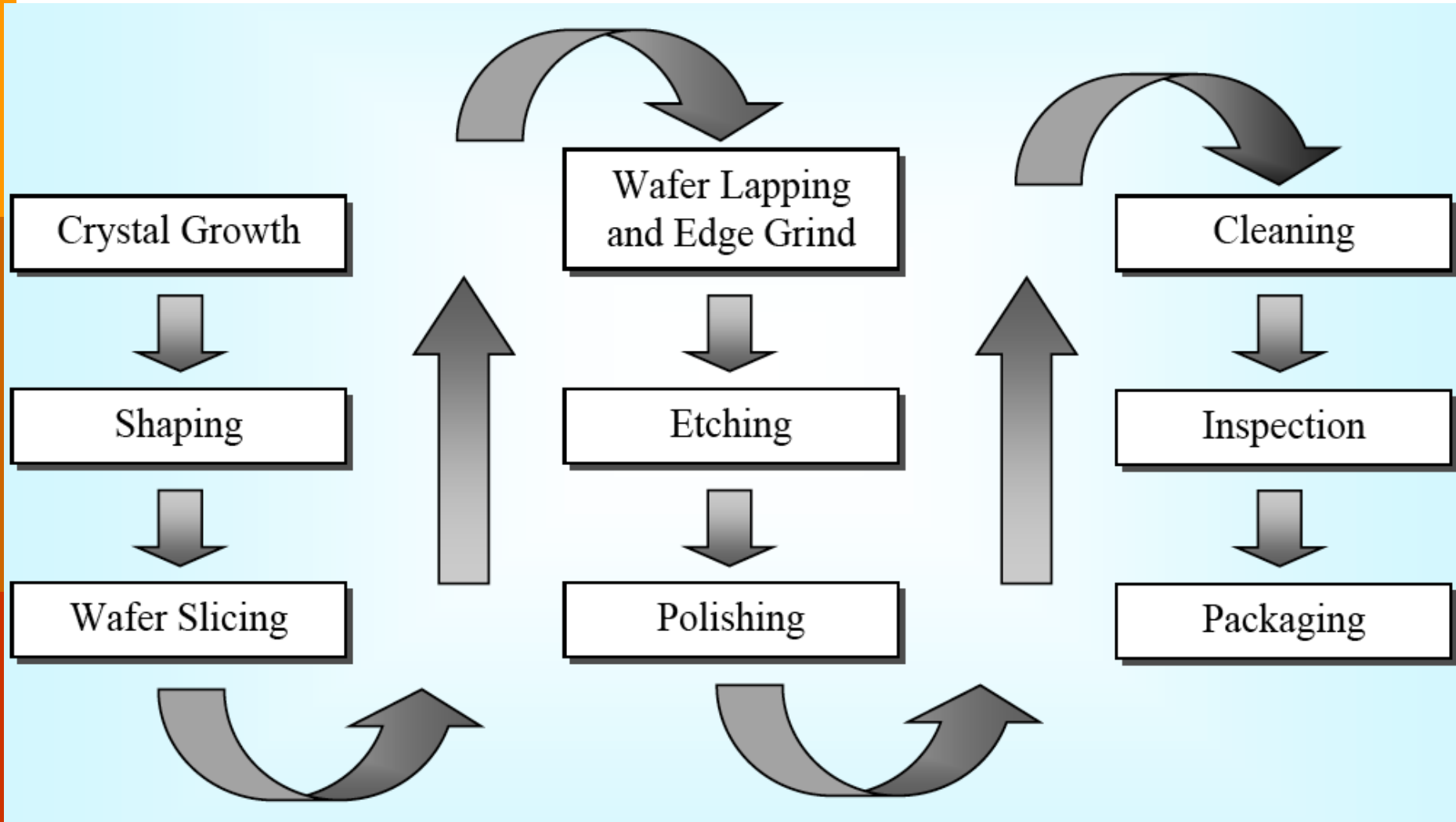


# Crystal growth :



Process flow from starting material to polished wafer.

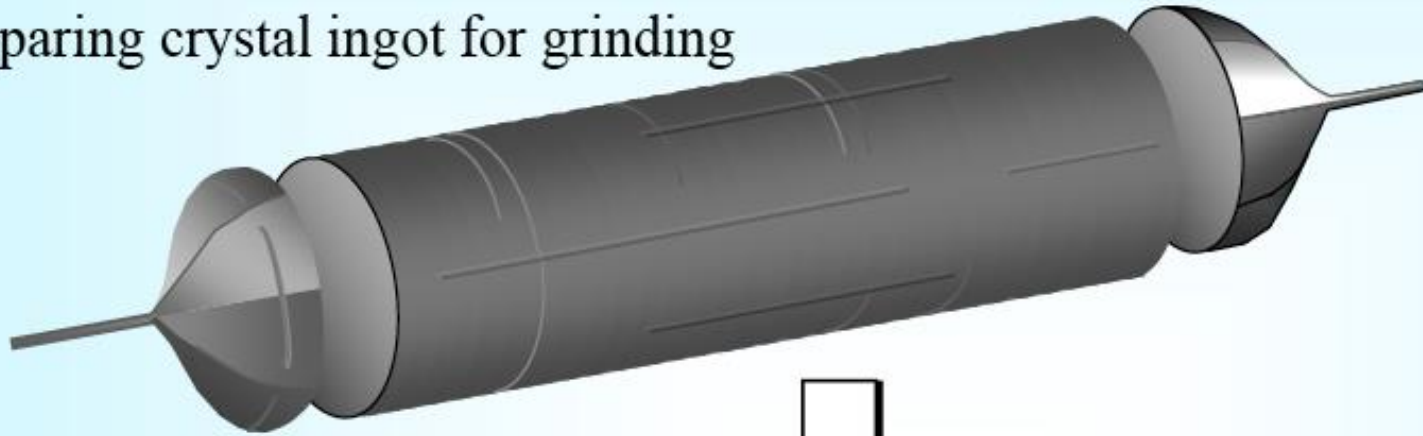
# Steps for wafer preparation



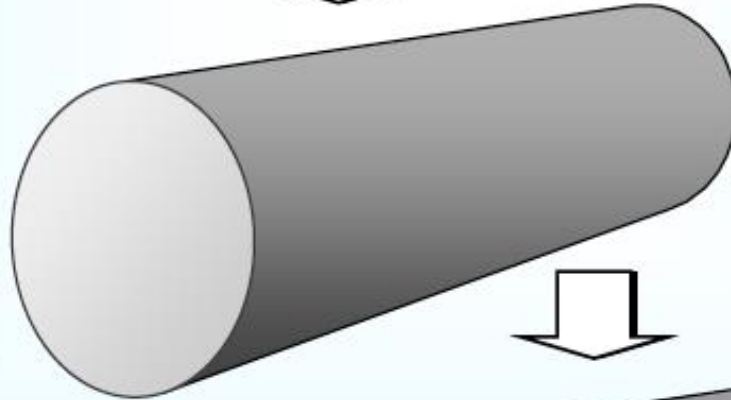


# Ingots grinding

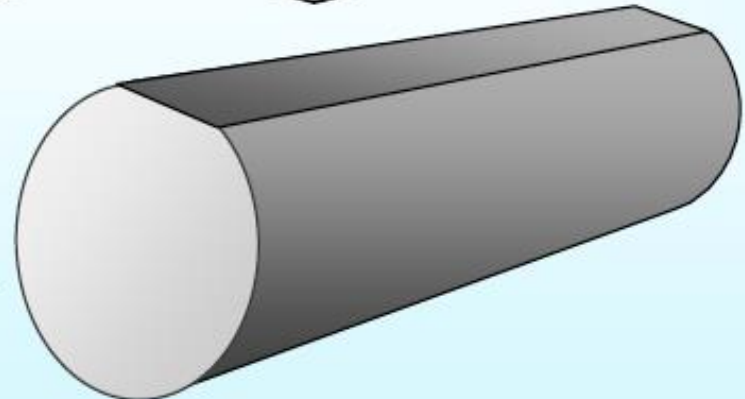
Preparing crystal ingot for grinding



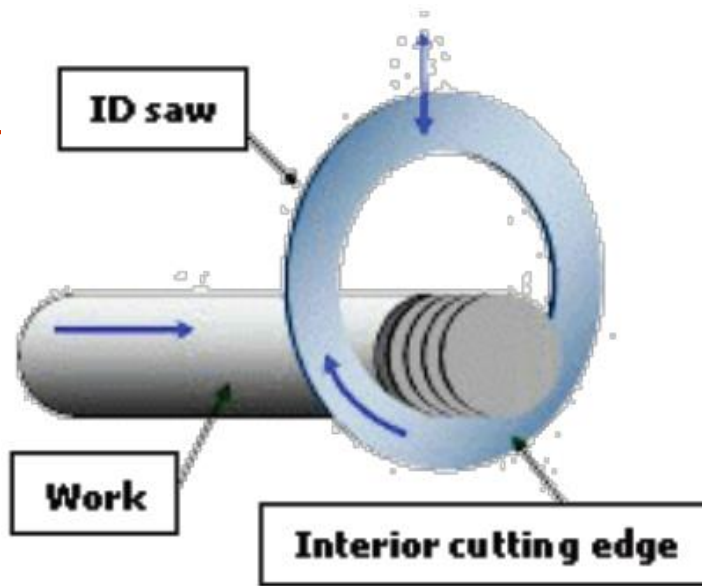
Diameter  
grind



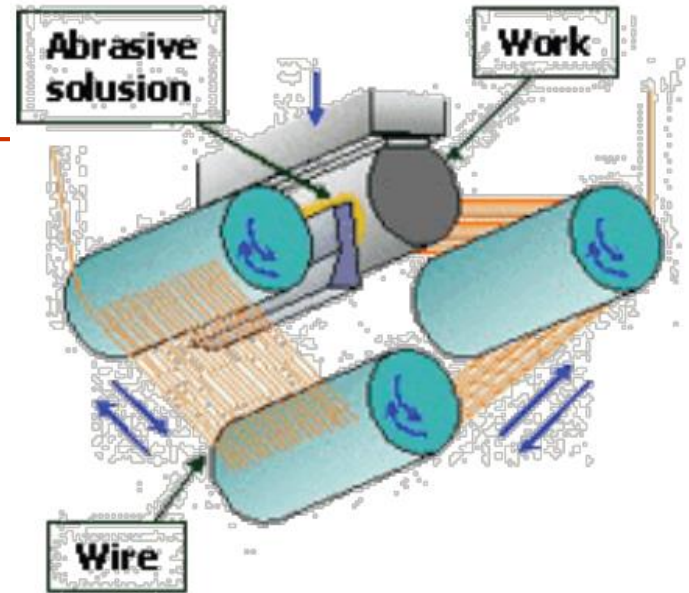
Flat grind



# Wafer slicing



Traditional method of slicing



Wire saw for large wafers

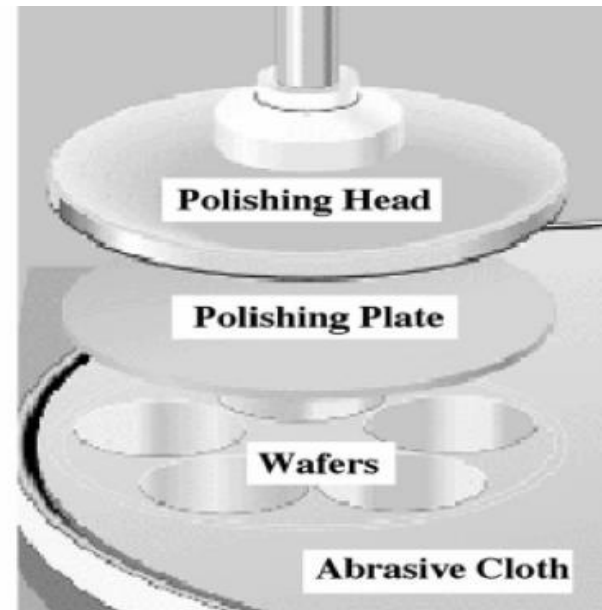
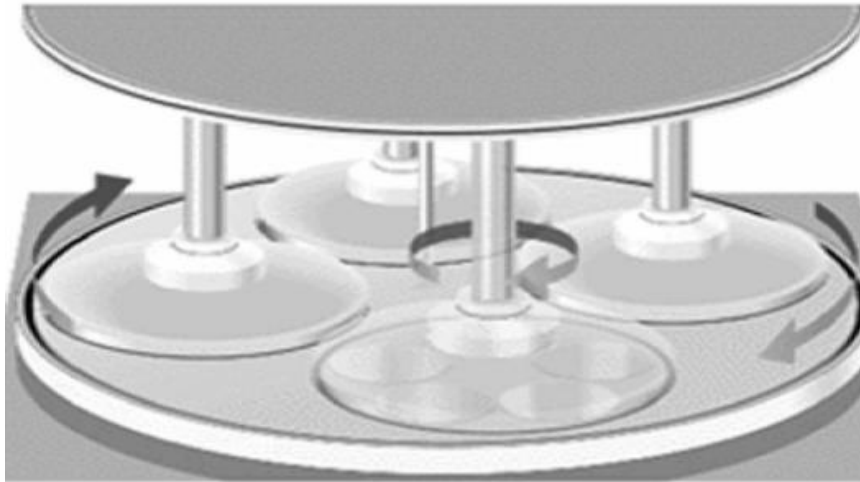


The saw blade itself is about  $400\mu\text{m}$  thick, together with the loss at the seed and tail end of the crystal, **only 50% of the boule ends up in wafer form.**

After slicing, mechanical lapping and wet chemical etching is performed before final chemical mechanical polishing.

# Wafer polishing

## Chemical mechanical polishing



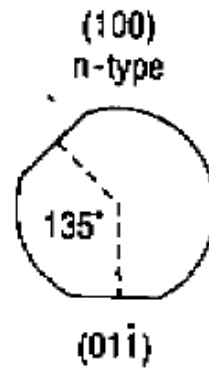
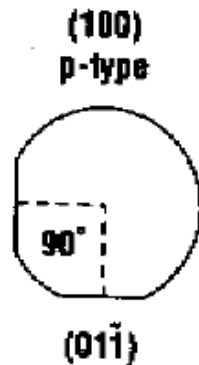
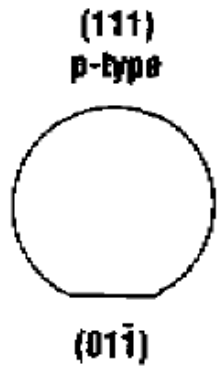
Slurry consists of nano-particles (10nm  $\text{SiO}_2$  or  $\text{Al}_2\text{O}_3$ ) and chemicals (NaOH).



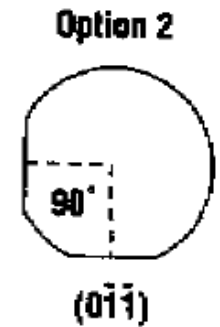
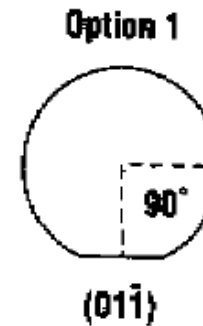
The rotation and pressure generates heat that drives a chemical reaction in which  $\text{OH}^-$  radicals from the NaOH oxidize the silicon. The  $\text{SiO}_2$  particles abrade the oxide away.

# Standard flat Orientations for Different Semi-conductor Wafers :

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(A) Si slices



(B) GaAs slices

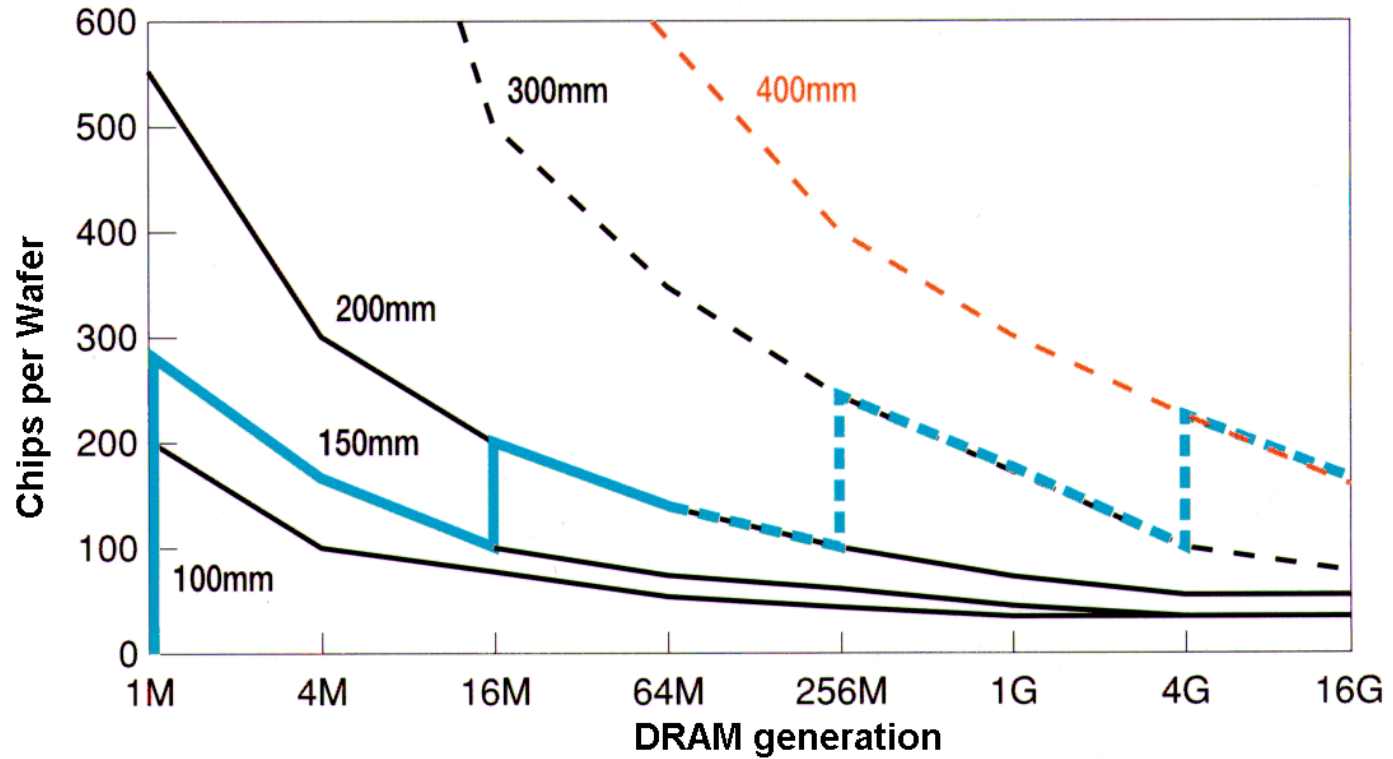
### 3 Typical specification for 2-in. GaAs wafers

	LEC	Vertical Gradient Freeze
Resistivity ( $\Omega$ -cm)	$>2 \times 10^7$	$>10^7$
Mobility ( $\text{cm}^2$ -V/s)	$>4000$	$>5000$
Carrier concentration ( $\text{cm}^{-3}$ )	$<10^8$	—
Etch pit density ( $\text{cm}^{-2}$ )	$7 \times 10^4$ (typical)	$<10^3$
Flatness ( $\mu\text{m}$ )	$<4$	$<5$
Thickness ( $\mu\text{m}$ )	450	500
Cost ( $\$/\text{cm}^2$ )	10	15

### Typical specifications for state of the art silicon wafer

Cleanliness (particle/ $\text{cm}^2$ )	$<0.03$
Oxygen concentration ( $\text{cm}^{-3}$ )	Specified $\pm 3\%$
Carbon concentration ( $\text{cm}^{-3}$ )	$<1.5 \times 10^{17}$
Metal contaminants bulk (ppb)	$<0.001$
Grown in dislocation ( $\text{cm}^{-2}$ )	$<0.1$
Oxidation induced stacking faults ( $\text{cm}^{-3}$ )	$<3$
Diameter (mm)	$\geq 150$
Thickness ( $\mu\text{m}$ )	625 or 675
Bow ( $\mu\text{m}$ )	10
Global flatness ( $\mu\text{m}$ )	3
Cost ( $\$/\text{cm}^2$ )	0.2

# Advantage of larger diameter wafers



More chips per wafer for larger wafer.

Thank You

