BE / ETRx / Sem VII / Rev

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Communication - Network

**Con. 6133–10.** **(REVISED COURSE)** **GT–8829**

(3 Hours) **[Total Marks : 100**

**N.B. : 1)** Question no.1 is **compulsory**
2) Attempt any **four** any four questions from remaining.
3) Assume **suitable data** whenever necessary

Q.1 a) Differentiate between TCP and UDP. 20

b) Layers of the internet model correlate to the layers of the OSI model explain.

c) Explain the looping problem in bridge LAN. How to solve it.

d) Distinguish between packet switching & circuit switching

e) Explain the ISDN channel structure for basic & primary services.

Q.2. a) Draw the layered OSI network architecture. Explain the function of each layer and show the path of actual and virtual connection between the layers. 10

b) Explain in detail Repeaters, Bridges, Routers and Switches. 10

Q.3.a) Explain XDSL technologies and its application. Explain in detail ADSL. 10

b) What is the exterior and interior routing? Explain in brief distance vector routing and path vector routing. 10

Q.4.a) Draw block diagram of functional architecture of ISDN and explain ISDN channels and interface 10

b) With respect to MAC protocol explain 10

i) Token Ring

ii) FDDI

Q.5. a) Write short note on 10

i) IEEE 802.2

ii) IEEE802.3

b) Explain leaky bucket and Token bucket algorithm in details. 10

Q.6.a) what is protocol performance? Derive the relation for protocol performance for 10

i) Stop and wait flow control mechanism

ii) Sliding window protocol mechanism.

b) Explain different types of ARQ techniques and compare their merits and demerits 10

Q.7.Write short note on (Any Three) 20

i) Utilities ii) SONET ISDN

iii) Berkeley API iv) Error control Techniques.

BE/ETRX/Sem VII/REV
VLSI Design

14/12/10

**Con. 6040-10.** **( REVISED COURSE )** **GT-8820**

( 3 Hours ) **[ Total Marks : 100**

**N.B.** : (1) Question No. **1** is **compulsory.**
(2) Attempt any **four** questions out of question nos. **2** to **7.**
(3) Draw **neat** diagrams wherever **required.**

1. (a) Compare Ion Implantation and Diffusion. **20**
(b) Explain constant field scaling in MOS Device.
(c) Draw stick Diagram for CMOS Invertor.
(d) Implement function using CMOS f = $\overline{ab+abc+a}$

2. (a) Explain Twin tub process in detail. **10**
(b) Calculate the threshold voltage $V_{TO}$ at $V_{SB}$ = 0, for a polysilicon gate N-channel MOS transistor, with the following parameters :— **10**
Substrate doping density $N_A = 10^{16}$ cm$^{-3}$,
Polysilicon gate dopping density $N_O = 2 \times 10^{20}$ cm$^{-3}$,
Gate oxide thickness tox = 300°A and
Oxide interface fixed charge density Nox = $4 \times 10^{10}$ cm$^{-2}$.

3. (a) Draw circuit of 2 input NAND gate, stick Diagram and Layout. **10**
(b) For a CMOS invertor find the region of operation :— **10**
(i) $V_{in} < V_{th}$
(ii) $V_{in} > C_{DD} + V_{tp}$
(iii) $V_{in} = V_{IL}$
(iv) $V_{in} = V_{IH}$
(v) $V_{in}$ = switching threshold.

4. (a) Compare resistive, Enhancement, Depletion load NMOS and CMOS invertor **10**
(b) Consider a CMOS invertor with the following parameters :— **10**
**NMOS** $V_{TO,n} = 0{\cdot}6$ V, $\mu_n$ Cox = 60 $\mu$A/V$^2$ and $(W/L)_n = 8$
**PMOS** $V_{TO,P} = -0{\cdot}7$ V, $\mu_p$ Cox = 25 $\mu$A/V$^2$ and $(W/L)_p = 12$
Calculate the noise margins and the switching threshold (Vth) of this circuit. The power supply voltage is $V_{DD} = 3{\cdot}3$ V.

5. (a) Write Verilog code of 1 Bit full adder using any style and instantiate it to design a 4 Bit full Adder. **10**
(b) Explain the method to design 4:1 MUX using pass transistor logic. Draw complete stick diagram. **10**

5. (a) Write Verilog code of 1 Bit full adder using any style and instantiate it to design a 4 Bit full Adder. **10**

(b) Explain the method to design 4:1 MUX using pass transistor logic. Draw complete stick diagram. **10**

6. (a) Explain short channel effect in terms of :— **15**
   (i) Velocity Saturation.
   (ii) Mobility Degradation.
   (iii) Channel Length Modulation.
   (iv) Threshold Voltage.
   (v) Hot Electron Effect.

(b) An NMOS transistor with K = 20 $\mu A/V^2$ and $V_{TH}$ = 1·5V is operated at $V_{GS}$ = 5V and $I_D$ = 100 $\mu A$. Find $V_{DS}$. **5**

7. Attempt any **three** :— **20**
   (a) Compare Burried and Butting contact.
   (b) Explain Latchup in CMOS and prevention.
   (c) Compare Semi custom and Full custom design.
   (d) Generate Verilog code for 4 Bit Shift Register.

Oct-10-27

BE/ETRX/Sem VII/Rev
Filter Design
27-2-10

Con. 5861–10. (REVISED COURSE) GT–8823

( 3 Hours ) [ Total Marks : 100

**N.B. :** (1) Question **No. 1** is **compulsory**.
(2) Attempt any **four** questions out of the remaining **six** questions.
(3) Draw **suitable** diagrams and graphs wherever **necessary**.
(4) **Figures** to the **right** indicate **full** marks.

1. (a) Explain the difference between Butterworth, Chebyshev and Elliptical filters. Mention their merits and demerits. Derive expression for the order of Butterworth filter. **10**
   (b) What is Frequency Warping ? When do we use Bilinear transformation technique ? What is an antialiasing filter ? Why it is used ? **10**

2. (a) Explain the working principle of a switched capacitor filter. What are the necessary conditions for the implementation of a switched capacitor filter. What type of switches are used and what are its advantages ? Explain its implementation in a typical op-amp based integrator. **10**
   (b) Using bilinear transformation design a Digital Bandpass Chebyshev filter with the following specification $\alpha_p$ = 2 dB in the passband, (950 Hz) ≤ f ≤ (1150 Hz) $\alpha_s$ = 20 dB in the stopband, 0 ≤ f ≤ (550 Hz) and (2150 Hz) ≤ f ≤ ∞ sampling frequency f = 8 KHz. **10**

3. (a) Write difference between IIR and FIR filter. Explain frequency sampling method using suitable example. **10**
   (b) Convert the following pole-zero IIR filter into a lattice-ladder structure :– **10**

$$y(n) = -0{\cdot}9\, y(n-1) + 0{\cdot}8\, y(n-2) - 0{\cdot}5\, y(n-3) + x(n) + 2x(n-1) + 3x(n-2) + 2x(n-3)$$

4. (a) Explain a Linear phase FIR filter for the case of constant phase delay and group delay, using suitable equations. Draw Impulse response sequences of symmetric sequences for (i) N odd and (ii) N even. **10**
   (b) A low pass digital filter has following specifications :– **10**

$$0{\cdot}8 \le |H(e^{jw})| \le 1 \quad \text{for } 0 \le w \le 0{\cdot}2\,\pi$$
$$|H(e^{jw})| \le 0{\cdot}2 \quad \text{for } 0{\cdot}6\,\pi \le w \le \pi$$

   Determine the order of Chebyshev and Butterworth filter to meet the following specification.

5. (a) What is an adaptive filter ? What are its advantages ? Which type of problem can be solved using adaptive filter. **10**
   (b) Convert a second order Butterworth filter (Low Pass) to Digital filter using impulse invariant techniques. **10**

4. (a) Explain a Linear phase FIR filter for the case of constant phase delay and group delay, using suitable equations. Draw Impulse response sequences of symmetric sequences for (i) N odd and (ii) N even. **10**

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5. (a) What is an adaptive filter ? What are its advantages ? Which type of problem can be solved using adaptive filter. **10**

(b) Convert a second order Butterworth filter (Low Pass) to Digital filter using impulse invariant techniques. **10**

6. (a) Design a Butterworth bandstop filter with 2 dB passband edges of 30 Hz and 100 Hz and 40 dB stopband edges of 50 Hz and 70 Hz. **10**

(b) Explain Basic Weiner filter. **10**

**OR**

Explain the method of matched Z–transform.

7. (a) Explain Decimation and Interpolation. When it is required ? Take suitable examples. **10**

(b) Explain subband coding (**Or**) Quadrature mirror filtering. **10**

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BE/ETRX/Sem VII/REV

Power Elect & drives.

VT-Oct-10-106

**Con. 6525–10.**

**(REVISED COURSE)**

9/12/10

**GT–8832**

( 3 Hours )

**[ Total Marks : 100**

**N.B. :** (1) Question **No. 1** is **compulsory**.
(2) Attempt any **four** questions from remaining **six** questions.
(3) **Figures** to the **right** indicate **full** marks.
(4) Assume **suitable** data, if **any**.

Q1) Attempt the following (20)
a) Discuss the different factors for selection of battery for UPS.
b) State and explain briefly, the basic principle of operation of the dual converter.
c) State the need of reduction of harmonics in inverter output.
d) State briefly, the control strategies employed in chopper for operating the switches.

Q2) a) With the help of circuit diagram and relevant waveforms, explain the operation of single phase, half-wave converter drive for a separately excited DC motor. (10)
b) Discuss the variable-frequency control method of an induction motor. (10)

Q3) a) Derive an expression of output voltage of single phase fully controlled converter with source inductance. (10)
b) Design a parallel inverter to feed a load at 200 V, 50 Hz and peak load current is 2 A, $E_{dc}$ = 40 V. Specify the rating of SCRs, transformer and commutating components. (10)

Q4) a) Describe the operation of step up chopper and derive an expression for output voltage of it in terms of duty-cycle. (12)
b) With the help of a circuit diagram, explain the working of SMPS. (08)

Q5) a) Explain sinusoidal pulse modulation as used in PWM inverter. (10)
b) Draw and explain the torque –speed characteristic at different firing angles, for a full converter feeding a separately excited DC motor. (10)

Q6) a) Discuss briefly, the stator voltage control scheme of an induction motor. (10)
b) Derive the expression for commutating components L & C for a voltage commutated chopper. (10)

Q7) Write short note on : (20)
a) Regenerative braking
b) Slip energy recovery scheme
c) McMurray inverter

BE/ETRX/Sem VII/old
Instrumentation SYS.

VT-Oct-10-5

9/12/10

**Con. 5552–10.** **(OLD COURSE)** **GT–8004**

( 3 Hours ) **[ Total Marks : 100**

**N.B.** : (1) Question **No. 1** is **compulsory**.
(2) Attempt any **four** questions out of remaining **six** questions.
(3) **Figures** to the **right** indicate **full** marks.

1. (a) Represent the response of a first order system to a step input and ramp input graphically. **5**
   (b) Explain the principle of Hall effect. **5**
   (c) Explain the block diagram of Generalized data acquisition system. **5**
   (d) Explain the operating principles of photo conductive cell and photo voltaic cell. Also state their applications. **5**

2. (a) Explain with neat sketches, the working, construction, advantages and disadvantages of resistance thermometer. Give the signal conditioning circuit for measurement. **10**
   (b) Discuss the piezoelectric transducer with signal conditioning system for vibration measurement. **10**

3. (a) Explain any one electrical method of differential pressure measurement. **10**
   (b) Describe different types of capacitive transducers and compare their sensitivities. Give one application of each. **10**

4. (a) Explain Absorbtion type and Transmission type of Torque measurement. **10**
   (b) Describe how strain is measured by using Wheatstone Bridge Circuits ? Also discuss the train balancing circuit. **10**

5. (a) With the help of neat diagrams, explain phase sensitive detectors in displacement measurement using LVDT. Why are the phase sensitive detectors required ? **10**
   (b) Explain seeback and peltier effect in thermocouples. Also explain the need for compensation for reference junction temperature. **10**

6. (a) Explain multichannel Analog multiplexed system. Compare the digital multiplexed multi-channel data acquisition system with it. **10**
   (b) With the help of neat diagram, explain how a pitot tube can be used for flow measurement. Derive the expression for the fluid velocity from Bernoulli's theorem. **10**

7. Write short-notes on :– **20**
   (a) Virtual Instrumentation
   (b) Classification of Transducers with one example of each
   (c) Digital accelerometer
   (d) Ultrasonic flow meter.

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B.E. ETRx / sem VII / old

Elective - I. wireless. com

Con. 5581-10. **( OLD COURSE )** **GT-7995**

( 3 Hours ) **[ Total Marks : 100**

**N.B.** : (1) Question No. **1** is **compulsory.**
(2) Solve any **four** questions from question Nos. **2** to **7**.
(3) Draw **neat** sketches wherever **required**.

1. (a) Explain with respect to GSM System :— Authentication center, Home location register and dedicated control channels. **10**
   (b) Explain in short the umbrella cell approach. What do you mean by cell dragging ? **10**

2. (a) Explain with neat block diagram the voice modulation process in AMPS system. What is requirement of SAT tones and signalling tones in AMPS system ? **10**
   (b) Explain functional model of DECT along with its FDMA/TDMA/TDD structure. **10**

3. (a) What are different diversity schemes used in mobile radio environment ? Hence explain maximal gain combining and equal gain combining techniques. **10**
   (b) Explain with suitable block diagram the modulation process on reverse IS-95 channel. **10**

4. (a) Explain security and privacy procedures in GSM. **10**
   (b) Explain different methods to configure and assign radio channels in CDPD. **10**

5. (a) Differentiate between fast fading and slow fading. **5**
   (b) Prove that for a hexagonal geometry the co-channel reuse ratio is given by **5**
   $Q = \sqrt{3N}$ where $N = i^2 + ij + j^2$
   (c) Explain orthogonal covering in CDMA. **5**
   (d) Explain cell breathing. **5**

6. (a) Describe knife edge diffraction model with example. **10**
   (b) Describe different approaches used to increase the coverage area of cell site. **10**

7. (a) Explain in detail HSCSD. **10**
   (b) Explain GPRS architecture, uplink and downlink channels. **10**

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B.E / ETRx / Sem VII / old
Electronic & Microcomputer sys & Design

P4 Con No 69

Con. 5743–10. **(OLD COURSE)** **GT–8002**

(3 Hours) **[Total Marks : 100**

**NB.** 1. **Question no.1** is compulsory.
2. Attempt any **five** out of remaining questions.
3. Illustrate **answers with sketches** wherever required.
4. Figures to the **right** indicate **full** marks.
5. Use legible handwriting. Use a **blue/black** ink pen to write answers.
6. Use of **pencil** should be done only to draw **diagrams** and **graphs.**

Q1 a) Explain Bus Parking of PCI bus. 05
b) Explain different USB transfer types. 05
c) Explain Zone Bit Recording. 05
d) Explain instruction-pairing rules for Pentium Processor. 05

Q2 a) Expiain register model of IDE, also explain what is CHS addressing and LBA addressing in IDE 10

b) Explain the function of following PCI signals
1. LOCK# 2. IDSEL 3. FRAME# 4. TRDY# 5. IRDY# 10
(#: These signals are active low signals)

Q3 a) Explain reflected wave switching and shared interrupts in PCI bus. 10

b) Explain error-handling signals of Pentium processor. 10

Q4 a) Explain SCSI bus phases with neat timing diagrams. 10

b) Explain code cache organization of Pentium Processor and also explain What is split line access? 10

Q5 a) Explain MESI model of Pentium data cache. 10

b) Explain following terms of USB bus 10
1. Host controller 2. USB Hub 3. NAK and ACK token
4. Transaction frame 5.USB driver

Q6 a) Explain branch prediction logic in Pentium and D1 stage of Pentium processor pipeline. 10

b) Explain bank conflict for simultaneous data access and clean line replacement in data cache of Pentium Processor. 10

Q7 Write short notes on following 20
1. System Management mode of Pentium
2. Latency timer in PCI bus
3. PCI hidden bus arbitration
4. Central Resources for PCI based devices

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