Design of JFET amplifier

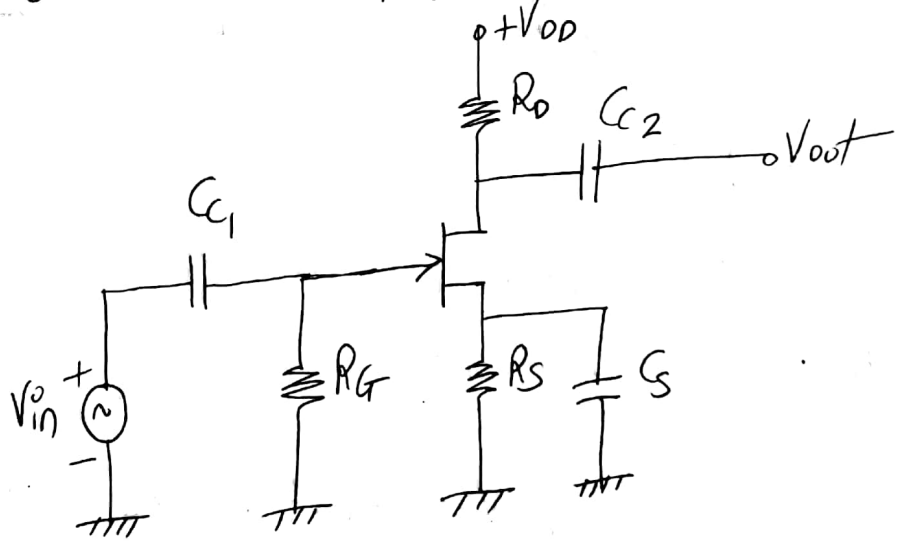
24/11/19

① Zero temperature drift technique } Use Self-bias
② Mid-point biasing technique

→ Standard values of R & C :-

1, 1.2, 1.5, 1.8, 2.2, 2.7, 3.3, 3.9, 4.2, 4.7
5.1, 5.6, 6.2, 6.8, 7.5, 8.2, 9.1 & multiples of 10

Self-bias JFET amplifier circuit to be designed



Design means to determine the values of R_G, R_D, R_S C_{C1}, C_{C2} & C_S

Design 01:-

Design a single stage CS JFET amplifier to give o/p voltage of 2V and voltage gain of −10. The circuit should be suitable for operation upto frequency of 20Hz

Note: If freq^n is not given assume it to be 50Hz

Soln:- A] We use zero-temperature drift biasing :-

1] **Data:** $|A_v| = 10$, $V_o = 2V$, $f_L = 20Hz$

2] **Selection of JFET :-**

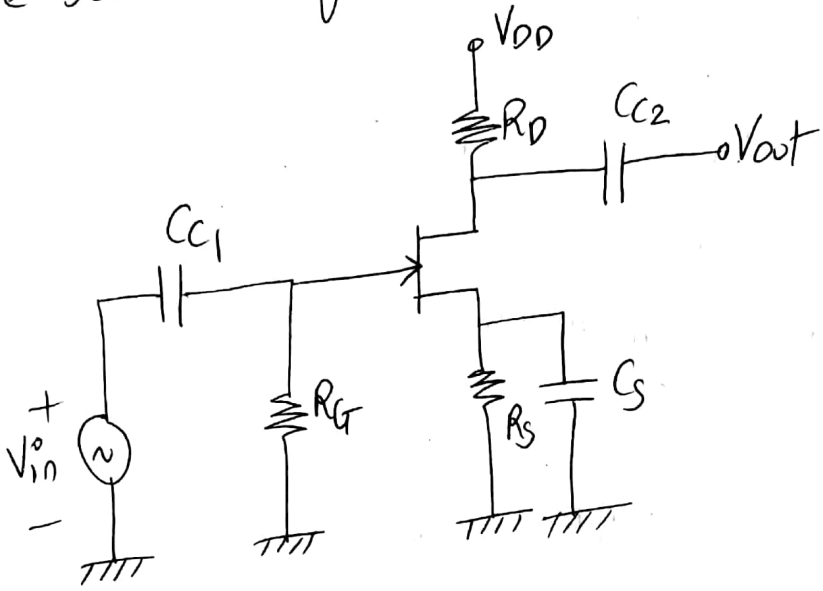
We select n-JFET BFW11 for the datasheet with following specifications:-

$g_{mo} = 5600\ \mu\mho$, $V_p = -2.5V$, $r_d = 50K\Omega$

$I_{DSS} = 7mA$

3] Selection of Biasing network:

We select self-bias circuit for our design



4] Selection of Q-point

i) For zero-temp. drift, $|V_p| - |V_{GS}| = 0.63$

$2.5 - |V_{GS}| = 0.63$

ie $|V_{GS}| = 1.87$

ie $\boxed{V_{GS} = -1.87\,V}$

ii) $I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2 = 7mA\left(1 - \frac{(-1.87)}{(-2.5)}\right)^2$

$\boxed{I_D = 0.44\,mA}$

iii) $g_m = g_{mo}\left(1 - \frac{V_{GS}}{V_P}\right) = 5600\times10^{-6}\left(1 - \frac{(-1.87)}{(-2.5)}\right)$

$\boxed{g_m = 1.4112\ \frac{mA}{V}}$

5) Selection of R_S :-

$$V_{GS} = -R_S I_D \quad \text{------ Self-bias}$$

$$\text{ie } R_S = \frac{-V_{GS}}{I_D} = \frac{-(-1.87)}{0.44\,mA} = 4.25K\Omega$$

Select L.S.V to maintain Q-pt in middle of transfer curve

Select $\boxed{R_S = 3.9K\Omega(std), 1/4W}$

6) Selection of R_D :

$$A_V = -g_m(r_d \,||\, R_D)$$

$$A_V = -g_m\left(\frac{r_d R_D}{r_d + R_D}\right)$$

$$-10 = -1.4112\times10^{-3}\left(\frac{50K\Omega\, R_D}{R_D + 50K\Omega}\right)$$

Solving we get,

$$R_D = 8.256K\Omega$$

Select H.S.V to increase the gain

Select $\boxed{R_D = 9.1K\Omega, 1/4W\,(std)}$

If R_L is given, then

$$A_V = -g_m(r_d \,||\, R_D \,||\, R_L)$$

7] Select of R_G :

To prevent loading of preceding stage,

Select $\boxed{R_G = 1M\Omega (std),\ 1/4W}$

8] Selection of V_{DD} :

$$V_{DS} \geq V_{opeak} + |V_p| \quad \text{---- (condition for undistorted o/p)}$$

$$V_{DS} = 1.5\left(V_{opeak} + |V_p|\right)$$

$$\boxed{V_{DS} = 1.5\left(V_{opeak} + 2.5\right)}$$

→ The value is multiplied by 1.5 to take care of saturation voltages, tolerance in resistance value, variation in supply voltage and device parameter variation

$$V_{orms} = 2V \quad \dashrightarrow \quad V_{opeak} = 2\sqrt{2}$$

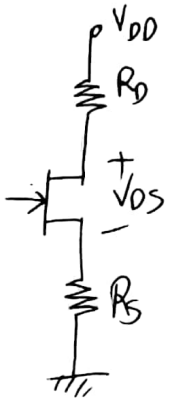
ie $V_{DS} = 1.5\left(2\sqrt{2} + 2.5\right)$

$= 7.99V$

$$\boxed{V_{DS} = 8V}$$

KVL to D-S loop,

$$V_{DD} - I_D R_D - V_{DS} - I_D R_S = 0$$



$$V_{DD} = V_{DS} + I_D (R_D + R_S)$$

$$V_{DD} = 8 + 0.44 \times 10^{-3} (3.9K + 9.1K)$$

$$V_{DD} = 13.72V$$

Select $\boxed{V_{DD} = 15\,V}$

g] Selection of C_S :-

$$f_L = 20Hz$$

$$X_{C_S} \leq 0.1\, R_S$$

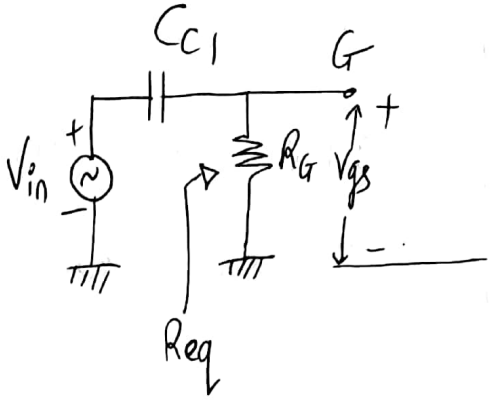
ie $$\frac{1}{2\pi f_L C_S} \leq 0.1\, R_S$$

ie $$C_S \geq \frac{1}{2\pi f_L \times 0.1 \times R_S} \geq \frac{1}{2\pi \times 20 \times 0.1 \times 3.9K\Omega}$$

$$C_S \geq 20.4\mu F$$

Select $\boxed{C_S = 22\mu F / 25V}$ H.S.V

10] Selection of C_{C_1}:



$$C_{C_1} = \frac{1}{2\pi f_{L_{C_1}} R_{eq}}$$

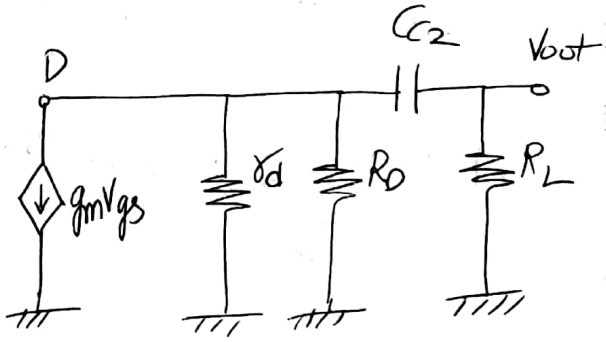
$$f_{L_{C_1}} = f_L = 20Hz$$

$$R_{eq} = R_G = 1M\Omega$$

$$C_{C_1} = \frac{1}{2\pi \times 20 \times 1M\Omega} = 7.957\,nf$$

Select $\boxed{C_{C_1} = 8.2nf/25V}$ H.S.V

11] Selection of C_{C_2}:



$$C_{C_2} = \frac{1}{2\pi f_{L_{C_2}} R_{eq}}$$

$$R_{eq} = r_d \,||\, R_D + R_L$$

If R_L is not given, select $R_L = R_{i_{nextstage}}$

$R_L = R_{G_{ns}} = 1M\Omega$

$$R_{eq} = r_d \,||\, R_D + 1M\Omega$$

$$R_{eq} = 9.1K \,||\, 50K + 1M\Omega$$

$$R_{eq} = 7.698K + 1M\Omega = 1.0077M\Omega$$

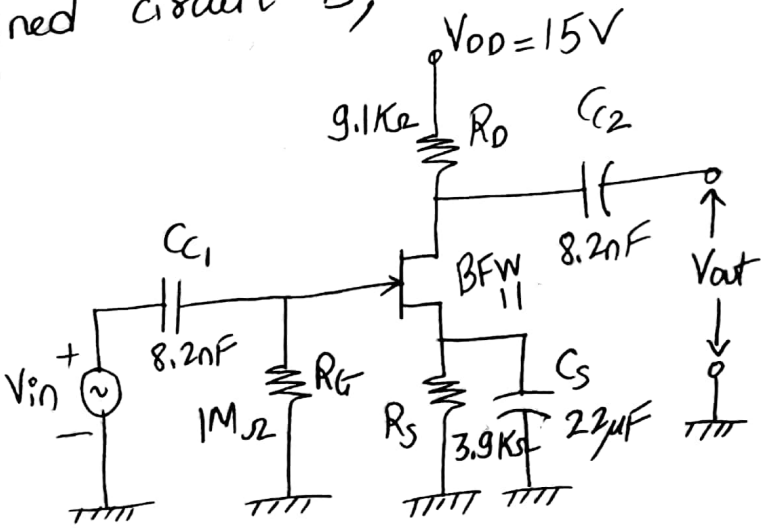
$$C_{C_2} = \frac{1}{2\pi f_{LC_2} R_{eq}} \qquad f_{LC_2} = f_L = 20Hz$$

$$= \frac{1}{2\pi \times 20 \times 1.0077M}$$

$$C_{C_2} = 7.89nf$$

Select $\boxed{C_{C_2} = 8.2nf/25V}$ H.S.V

12] Designed circuit is,



Designed single stage CS JFET amplifier using zero-temperature drift technique

Design 01 can also be implemented using mid-point biasing technique

B] Mid-point biasing

1] Data : $|A_V| = 10$, $V_o = 2V$, $f_L = 20Hz$

2] Selection of JFET :

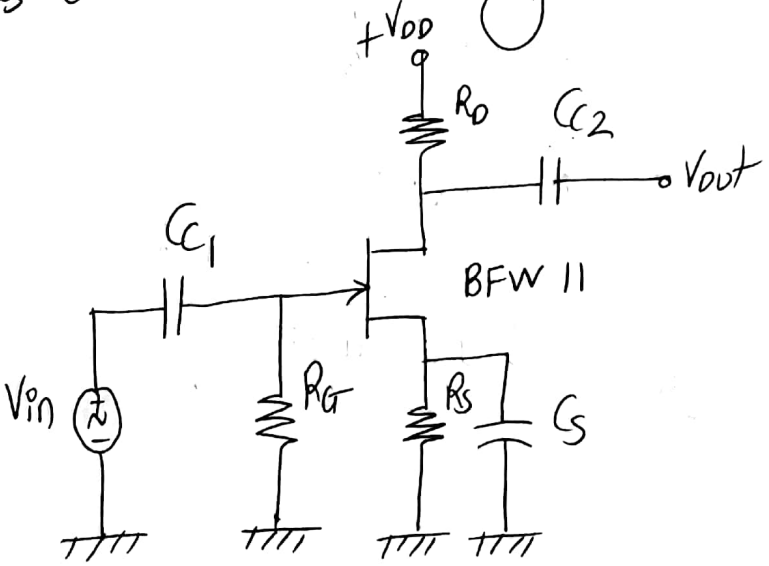
We select n-channel JFET BFW11 from the datasheet with following specifications: -

$g_{mo} = 5600 \mu\upsilon$, $V_p = -2.5V$, $\gamma_d = 50K\Omega$

$I_{DSS} = 7mA$

3] Selection of Biasing circuit :-

Self-bias circuit is used to give mid-point biasing.



4) Selection of Q-point :

i) For mid-point biasing, $I_D = \frac{I_{DSS}}{2}$

ie $I_D = \frac{7mA}{2} = 3.5mA$

ii) $I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2$

$\frac{3.5mA}{7mA} = \left(1 - \frac{V_{GS}}{V_P}\right)^2 \Rightarrow 0.5 = \left(1 - \frac{V_{GS}}{V_P}\right)^2$

OR

$V_{GS} = V_P\left[1 - \sqrt{\frac{I_D}{I_{DSS}}}\right]$

$= -2.5\left[1 - \sqrt{\frac{1}{2}}\right]$

$\boxed{V_{GS} = -0.732\,V}$

iii) $g_m = g_{mo}\left(1 - \frac{V_{GS}}{V_P}\right)$

$= 5600 \times 10^{-6}\left(1 - \frac{(-0.732)}{(-2.5)}\right)$

$\boxed{g_m = 3.96\ mS}$

5] Selection of R_S :

$$V_{GS} = -I_D R_S \quad \text{---------- Self-bias}$$

$$R_S = \frac{-V_{GS}}{I_D} = \frac{-(-0.732)}{3.5mA}$$

$$R_S = 209\,\Omega$$

Select $\boxed{R_S = 220\,\Omega_{(std)},\ 1/4W}$ H.S.V

6] Selection of R_D :

$$A_V = -g_m(r_d \| R_D)$$

$$-10 = -3.96 \times 10^{-3}\left(\frac{50K \times R_D}{50K + R_D}\right)$$

Solving, we get

$$R_D = 2.67K\Omega$$

Select $\boxed{R_D = 2.7K\Omega_{(std)},\ 1/4W}$

7] Selection of R_G :

Select $\boxed{R_G = 1M\Omega,\ 1/4W}$

8] Selection of V_{DD} :-

$$V_{DS} \geq V_{opeak} + |V_p|$$

$V_{rms} = 2V$

$V_{opeak} = 2\sqrt{2}\ V$

$$V_{DS} = 1.5(V_{opeak} + 2.5)$$

$$= 1.5(2\sqrt{2} + 2.5)$$

$$V_{DS} \simeq 8V$$

KVL to D-S loop gives,

$$V_{DD} - I_D R_D - V_{DS} - I_D R_S = 0$$

$$V_{DD} = V_{DS} + I_D(R_D + R_S)$$

$$V_{DD} = 8 + 3.5mA\,(2.7K + 220)$$

$$V_{DD} = 18.22V$$

Select $\boxed{V_{DD} = 20V}$

9] Selection of C_S :-

$$X_{C_S} \leq 0.1 R_S$$

$$\frac{1}{2\pi f_{L_S} C_S} \leq 0.1 R_S$$

$f_{L_S} = f_L = 20Hz$

$$C_S \geq \frac{1}{2\pi f_L \times 0.1 R_S} \geq \frac{1}{2\pi \times 20 \times 0.1 \times 220}$$

$C_S \geq 361.715\,\mu F$

Select $\boxed{C_S = 390\,\mu F/25V}$ H.S.V

10] Selection of C_{C_1}:

$$C_{C_1} = \frac{1}{2\pi f_{LC_1} R_{eq}} \qquad f_{LC_1} = f_L = 20Hz$$

$$R_{eq} = 1M\Omega = R_G$$

$$\text{ie } C_{C_1} = \frac{1}{2\pi \times 20 \times 1M\Omega} = 7.95\,nf$$

Select $\boxed{C_{C_1} = 8.2nf/25V}$ H.S.V

11] Selection of C_{C_2}: (Step 11 similar to Zero-temp drift)

$$C_{C_2} = \frac{1}{2\pi R_{eq} f_{LC_2}} \qquad f_{LC_2} = f_L = 20Hz$$

$$R_{eq} = r_d \,||\, R_D + R_L \qquad R_L = R_G = 1M\Omega \text{ (next stage)}$$

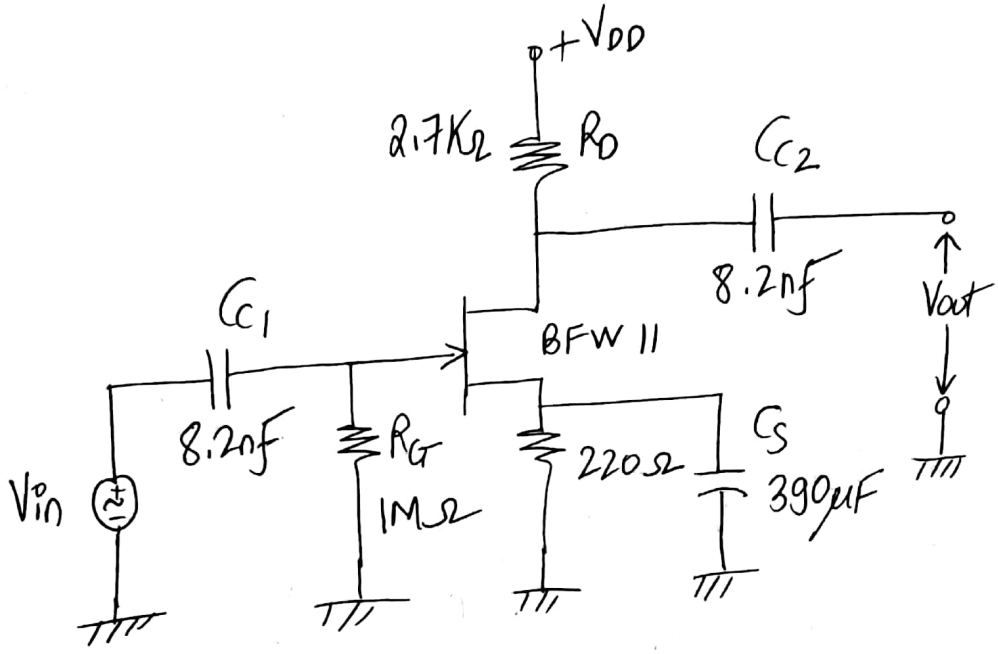
$$= (2.7K \,||\, 150K) + 1M\Omega$$

$$R_{eq} \simeq 1M\Omega$$

$$C_{C_2} = \frac{1}{2\pi \times 1M \times 20} = 7.95\,nf$$

Select $\boxed{C_{C_2} = 8.2nF/25V}$ H.S.V

12] Designed circuit is,



Designed single-stage CS JFET amplr using Mid-point biasing technique