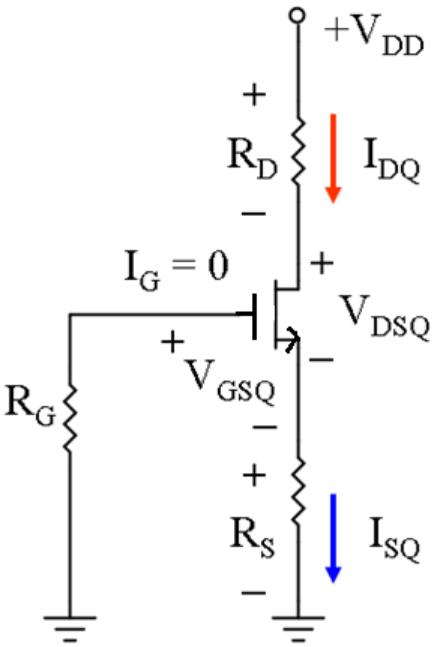
DESIGN OF MOSFET SELF BIASING CIRCUIT

Design MOSFET self-biasing circuit to achieve Q – Point of V_{DSQ} and I_{DQ} employing N-channel MOSFET. Also draw neatly the designed circuit with standard component values. For NMOS E type: k_n & V_{TN} will be given.



STEP 1 – Calculation of Gate Resistor (R_G)

To maintain high input resistance or input impedance (R_i or Z_i) gate resistor (R_G) has to be kept extremely high in order to prevent or minimize the loading effects. Hence select the nearest highest value of the gate resistor (R_G) which is $R_G = 1\ M\Omega$.

STEP 2 – Calculation of Source Resistor (R_S)

For the MOSFET self-biasing circuit, applying KVL in the gate-to-source loop :-

$$V_{GS} = -I_D R_S \quad \ldots\ldots\ldots (1)$$

The gate-to-source voltage (V_{GS}) can be easily calculated from Equation 2:-

$$I_D = k_n (V_{GS} - V_{TN})^2 \quad \ldots\ldots\ldots (2)$$

Calculate V_{GS} from (2) & substitute it in (1) to obtain the value of the source resistor (R_S).

STEP 3 – Calculation of Drain Resistor (R_D)

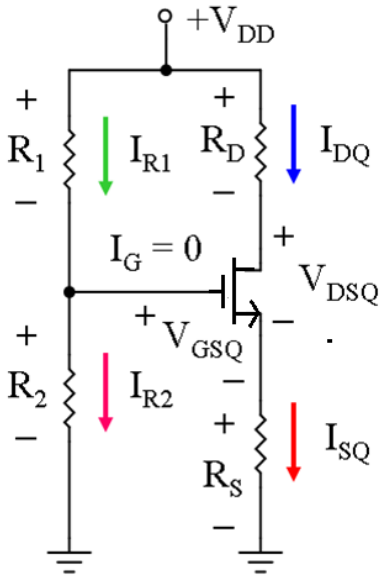
Applying KVL in the drain-to-source loop:-

$$R_D = \frac{V_{DD} - V_{DS} - I_D R_S}{I_D} \quad \ldots\ldots\ldots (3)$$

Calculate R_D from (3) to obtain the value of the source resistor (R_D).

DESIGN OF MOSFET E TYPE VOLTAGE DIVIDER BIASING CIRCUIT

Design MOSFET voltage divider biasing circuits to achieve Q-Point of V_{DSQ} and I_{DQ} employing N-channel MOSFET. Also draw neatly the designed circuit with standard component values. For NMOS E type: k_n & V_{TN} will be given.



STEP 1 – Selection of Biasing Resistors (R_1 & R_2)

Applying the voltage divider rule at the gate terminal:-

$$V_G = V_{DD}\, R_2 / (R_1 + R_2) \ldots\ldots\ldots\ldots (1)$$

Assume V_G as typically 25 % of the DC supply voltage ($+V_{DD}$) where V_G = 25 % of $+V_{DD}$
Assume R_2 = ____ kΩ (select any standard value from 100 kΩ to 470 kΩ) hence from above equation calculate R_1 & select nearest standard value.

STEP 2 – Calculation of Source Resistor (R_S)

For the MOSFET voltage divider biasing circuit, applying KVL in the gate-to-source loop:-

$$V_{GS} = V_G - I_D R_S \ldots\ldots\ldots\ldots (2)$$

The gate-to-source voltage (V_{GS}) can be easily calculated from Equation (3):-

$$I_D = k_n (V_{GS} - V_{TN})^2 \ldots\ldots\ldots\ldots (3)$$

Calculate V_{GS} from (3) & substitute it in (2) to obtain the value of the source resistor (R_S)

STEP 3 – Calculation of Drain Resistor (R_D)

Applying KVL in the drain-to-source loop:-

$$R_D = \frac{V_{DD} - V_{DS} - I_D R_S}{I_D} \ldots\ldots\ldots\ldots (4)$$