NATIONAL INSTITUTE OF TECHNOLOGY ROURKELA

DESIGN AND SIMULATION OF DOUBLE GATE FETs USING ATLAS

BY-

DEBASHISH SAHU (110EI0254)

ASHISH KUMAR TIRKEY (110EI0155)

UNDER GUIDANCE OF:

PROF. P.K. TIWARI

DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGG.

NATIONAL INSTITUTE OF TECHNOLOGY

ROURKELA, ODISHA(769008)

CERTIFICATE OF COMPLETION

It is here by certified that the thesis titled "*DESIGN AND SIMULATION OF DOUBLE GATE FETs USING ATLAS*" submitted to the National Institute of Technology, Rourkela by DEBASHISH SAHU(110EI0254) and ASHISH KUMAR TIRKEY(110EI0155) for the B.TECH degree in Electronics & Instrumentation Engineering, is a authenticated record of systematical and scientific research work completed successfully by them under my direction and guidance.

PROF. P.K. TIWARI

DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

NATIONAL INSTITUTE OF TECHNOLGY ROURKELA

ODISHA, INDIA (769008)

ACKNOWLEDGEMENT

I would like to convey my special thanks and gratitude towards PROF. P.K. TIWARI, who guided me to complete this project on the topic (DESIGN AND SIMULATION OF DOUBLE GATE FETs), by which I have done a lot of research work and i learned about so many new things, I am always thankful. And I would also thank the M.Tech scholars who helped me out in many fields during the completion of the project work.

INDEX

ABSTRACT-

In this project we have numerically simulated DOUBLE GATE FETs structure through ATLAS device simulator. Analysis and comparative study of the electrical characteristics of DOUBLE GATE FETs with that of conventional SOI MOSFETs has been done. As CMOS scaling is approaching the limits imposed by oxide tunneling and voltage non-scaling, DOUBLE GATE FETs has become a important part of VLSI research. An analytical model is developed using ATLAS simulator to analyze short channel effects (SCE), potential distributions, impact ionization ,ion scattering ,hot electron effect ,sub threshold swing,. Complete structure was designed and all possible errors were optimized.

1.INTRODUCTION-

The silicon metal oxide semiconductor field effect transistor (MOSFET) is one of the major and vital components in the semiconductor world. Since its first practical use 50 years ago, the MOSFET has a vital use in integrated circuits (ICs) to serve as a basic operating device in switching functions for digital circuits and as an amplifier device for analog applications. While the basic planar structure of the MOSFET has remained mostly unchanged, its size has been shrunk by many orders of magnitude over the past thirty years. The trend showing an exponentially increasing number of transistors on a chip was first predicted in 1965 and has since come to be known as ‘Moore’s Law’ shows a plot of the minimum feature size in the MOSFET, the gate length, over time. The main driving forces behind gate length scaling are the higher switching speed and packing density that result from making the transistors smaller. Device scaling has enabled IC chips to operate faster and with greater functionality each new technology generation. the exponential increase in microprocessor performance, represented by millions of instructions per second (MIPs), over technology generations.

1.1. MOSFET - Metal-Oxide-Semiconductor Field-Effect Transistor-

These devices are used heavily to design analogue and digital circuits. It has two types that are n-type MOSFET and p-type MOSFET. Silicon, SiGe is mostly used for manufacturing of these devices. Gate terminal has a very small and thin layer of polysilicon layer which is covered by silicon dioxide which is the insulator that is present between the current carrying channel and gate terminal. When voltage is applied to source and gate, an electric field is generated in the oxide layer of the FET and it creates an inverse channel in the conducting path which is the depletion region. In n-type majority carriers are electrons and in p-type holes.

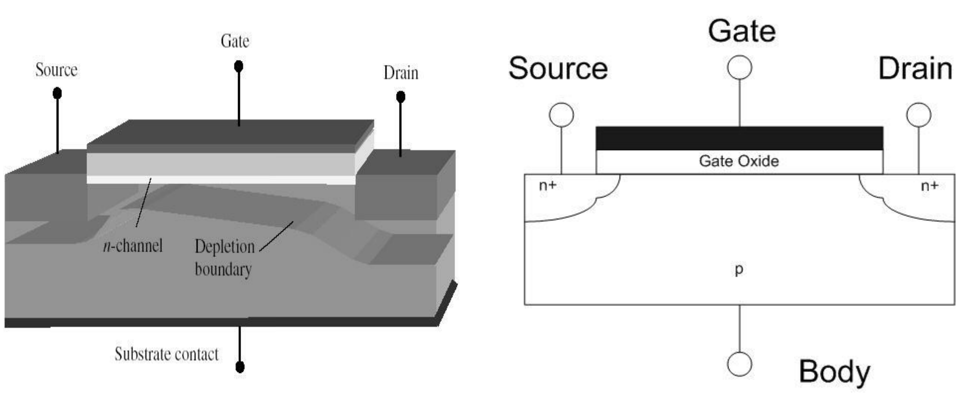


Fig. 1.1 structure of bulk MOSFET [1]

1.1.1. MOSFET operation-

There are generally 3 modes of operation in mosfets. The first one is the cut-off mode where the applied gate voltage is less than threshold voltage. Since it's not operating there is no current passing or flowing through the device. The second one is where the drain to source voltage is less than the difference between the gate to source voltage and threshold voltage in this region the current varies linearly with voltage. The third one is the saturation mode where drain to source voltage is greater than the difference between the gate to source voltage and threshold voltage. It is highly conducting mode in which the switch remains in the on state and the drain voltage is much greater than gate voltage half part of the channel remains in the off-state and it is known as the pinch-off voltage. When it happens the MOSFET stops to operate in linear region and it moves towards the saturation region. Mainly the linear mode is used in digital circuits and the saturation mode is widely used in analog circuits.

It has two modes depletion mode and enhancement mode. In depletion mode no gate voltage applied but in enhancement mode the gate terminal has certain potential connected to it.

- DEPLETION MODE

- ENHANCEMENT MODE

1.1.2 DEPLETION MODE-

These type of MOSFETs conducts when they no gate voltage is applied. The flow of ions is not anot stopped. As the gate is made more negative than the source, a depletion region is created in the N type channel, reducing conduction between source and drain. Even in the absence of the gate voltage it conducts.

1.1.3 ENHANCEMENT MODE-

When the surface of the device is reduced, it won't have conducting channel unless a gate voltage is applied to it. . The electrons at the oxide and the semiconductor junction are present in a thin layer which is called inversion layer. And thse devices are called enhancement mode devices.

1.2 Limitation and Disadvantage of the MOSFETs-

In digital world a large no of CMOS circuits are used in which millions of MOSFETs are to be used due to lack of scaling techniques, high power dissipation, time delay due to parasitic capacitance it is unsustainable and it consumes large energy with time delay. so it seems to be unfit for the modern era of technology. It was difficult to optimize all the parameters like threshold voltage, channel shortening, and barrier lowering which is induced by high drain voltage accurately. So MOSFETs and DOUBLE GATE MOSFETs came to the market.

1.3 SOI MOSFET-

This type of MOSFETs is somewhat different than the bulk MOSFETs. In the place of substrate there is a layer of silicon dioxide present at the bottom of the channel so that the channel is isolated from the substrate. The oxide layer is called the buried oxide or the BOX which act as insulator for the channel. So it's the silicon on insulator MOSFET. The channel is not affected by the substrate layer. The body capacitance is also less as the buried oxide layer which is smaller than substrate which is present in the bulk MOSFET.

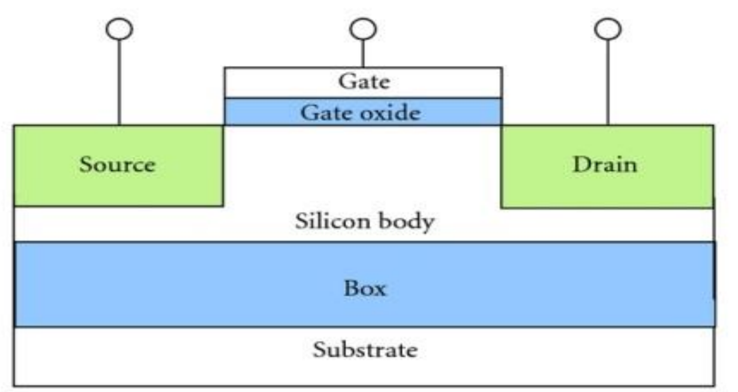


Fig. 1.2 SCHEMATICS OF SOI MOSFETs [2]

There are two types of SOI MOSFET and partially depleted.

- Fully depleted SOI MOSFET.
- Partially depleted SOI MOSFET.

1.3.1 PARTIALY DEPLETED SOI MOSFET-

In partially depleted SOI MOSFETs the distance between the gate and the buried oxide layer is greater than depletion region but in case of fully depleted SOI MOSFETs the distance is less than the depletion region. The PD SOI MOSFETs has the area between the source and drain which is reduced as a result the parasitic capacitance decreases and the delay also diminishes to a smaller value which is very useful for designing high-speed circuits. But if we compare the potential the FD SOI MOSFETs are better than the partially depleted. The channel length and width are much lesser than original, shows high conduction.

1.3.2 FULLY DEPLETED SOI MOSFET-

In fully depleted SOI MOSFETs the distance between the gate and the buried oxide layer is smaller than te depletion region. If we analyse the behaviour of these MOSFETs we can conclude that the front gate that is present outside with the source and the drain , and the back gate they are cupled during the entire device operation electrostatically. The fully depleted device parameters like drain current, threshold voltage , trans conductance depends on the voltage applied to the back voltage. It’s somewhat different from the partially depleted SOI MOSFETs. The energy difference between the front gate and back gate is higher in case of partially depleted MOSFETs.

1.3.3 DISADVANTAGE AND LIMITATION OF SOI MOSFETs-

- The oxide layer is directly attached to the channel so there is some leakage current.

- The changing and fluctuating variables which are the intrinsic parameters cannot be controlled by doped channel and impurities are not minimized.

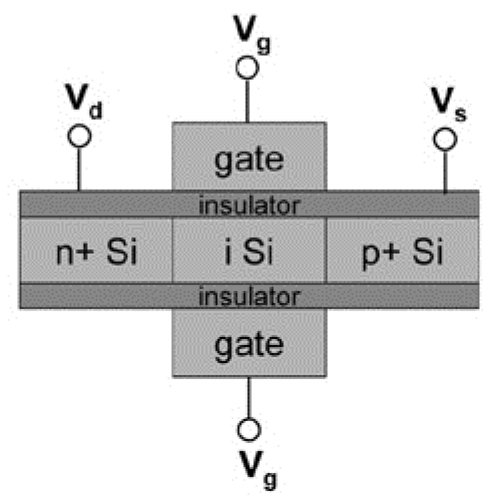
- Presence of short channel effect, kink effect make it unworthy for the use in large scale

- Sub threshold swing are greater as a result the fluctuation of drain current in the sub threshold region is higher which is undesirable.

- As the junction is attached with field implant and substrate the bulk MOSFETs have higher capacitance and the SOI MOSFETs have less junction capacitance as the it’s only attached to buried oxide.

1.4 DOUBLE GATE FETs-

The Double-Gate FET is definitely wise choice in place of BULK MOSFETs. In this device both the gates are placed in symmetry covering the channel which are present at the opposite of each other. The channel is formed near the gate. In this device both the gates are connected to the same potential and they have the same dimensions so it is known as symmetric DG-FET.



(DOUBLE GATE FET)

Fig. 1.3 A SIMPLE DG FET [2]

The presence of double gate provides electrostatic control over the channel in which the drain field line cannot effect or disturb the channel and it promisingly reduces the short channel effects. Leakage current is reduced because te substrate is replaced by the second gate. The DG-FETs are of smaller dimension as compare to bulk type. The body is undoped in this type MOSFETs it enhances the electrical characteristics like mobility ion transfer and removes the drawback which were present in conventional model.

.

1.4.1 OPERATION

The effect of gate voltage was studied which was applied on source body. In the off-state. Two important factors are doping of the source and drain and the work function of the gate. The electron can't be transferred from source to the body without threshold voltage so gate potential is applied on the both terminals as it start to increase the potential of the surface start to increase which reduces the source limit. The gate potential forward biases the source-body junction. In vertical direction the body potential is unchanged. As the source limit is reduced, exponential increase of injecting electron from source to body is noticeably seen. This is due to increase in the energy level of electrons. Thus it operates.

1.4.2 PROBLEM DUE TO MIS-ALIGNMENT-

The major precaution while designing the DG device is doesn't misalign the two gates they should be present at opposite to each other and they should be symmetric. Generally the top gate is symmetric with the source and the drain because it's placed outside if the bottom gate is not in symmetry it will overlap with either source or drain which will cause disturbance in channel flow and lekage current.

2.1 SIMULATION OF FETs USING ATLAS-

2.1.1 Atlas inputs and Outputs-

It uses two types of input file

- A text file that contains Atlas commands.
- A structure file that defines the structure to be simulated.

Atlas produces three types of output files

- The runtime output that gives error and warning messages as the simulation proceeds, After the input is loaded .
- The log file that stores voltage and currents.
- The structure file that stores 2D and 3D data relating to the values of solution variables.

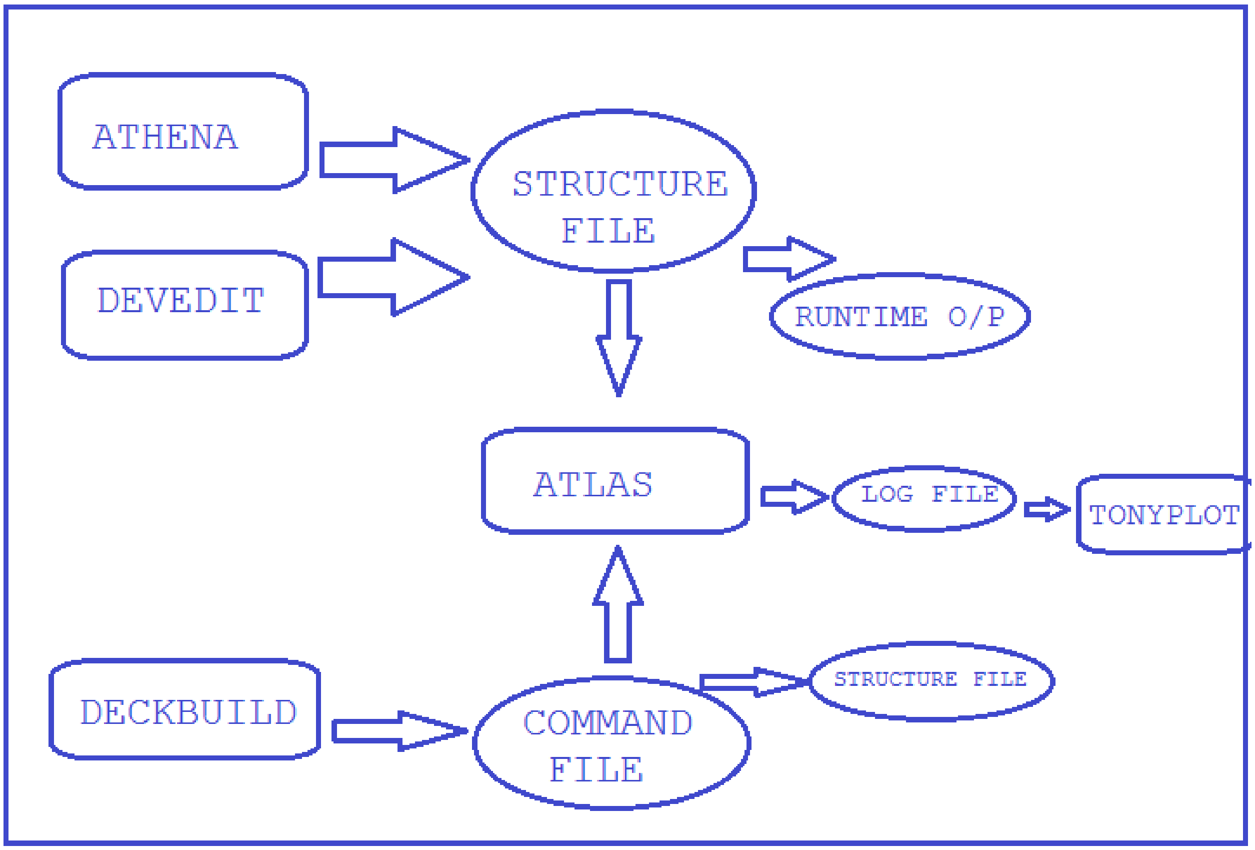


Fig. 2.1 flow of data in atlas

The above flow chart shows the flow of data during the entire simulation. The output of Athena, Devedit and Deckbuild enters to the structure file and command file sequentilay then we get the logfile which has the output along with structure file. It shows the runtime O/P. In tonyplot we get the detail of the structure.

2.1.2 BASIC OPERATION TO CREATE INPUT FILE

- Loading the diode structure.
- Specifying the electrodes(anode and cathode).
- Selecting the bipolar models and the impact ionization model.
- Specifying the numerical method.
- Reverse biasing the diode to obtain the breakdown curve.
- Saving the log and structure files.
- Generate the log file for the tonyplot and the output.

2.1.3 Sequence of steps to generate the structural model-

- Program is written in deck build.

- 3D device Models are generated using DEVEDIT.

- ATLAS combines both command and structure files and generates the log file after compilation.

- TONYPLOT shows the structural output.

- In this shoftware mesh is generated for different parts like source, gate, and drain through iteration methods.

- Then doping concentration and work functions are defined sequentially.

3 RESULTS:

3.1 STRUCRURE OF CONVENTIONAL SOI MOSFET-

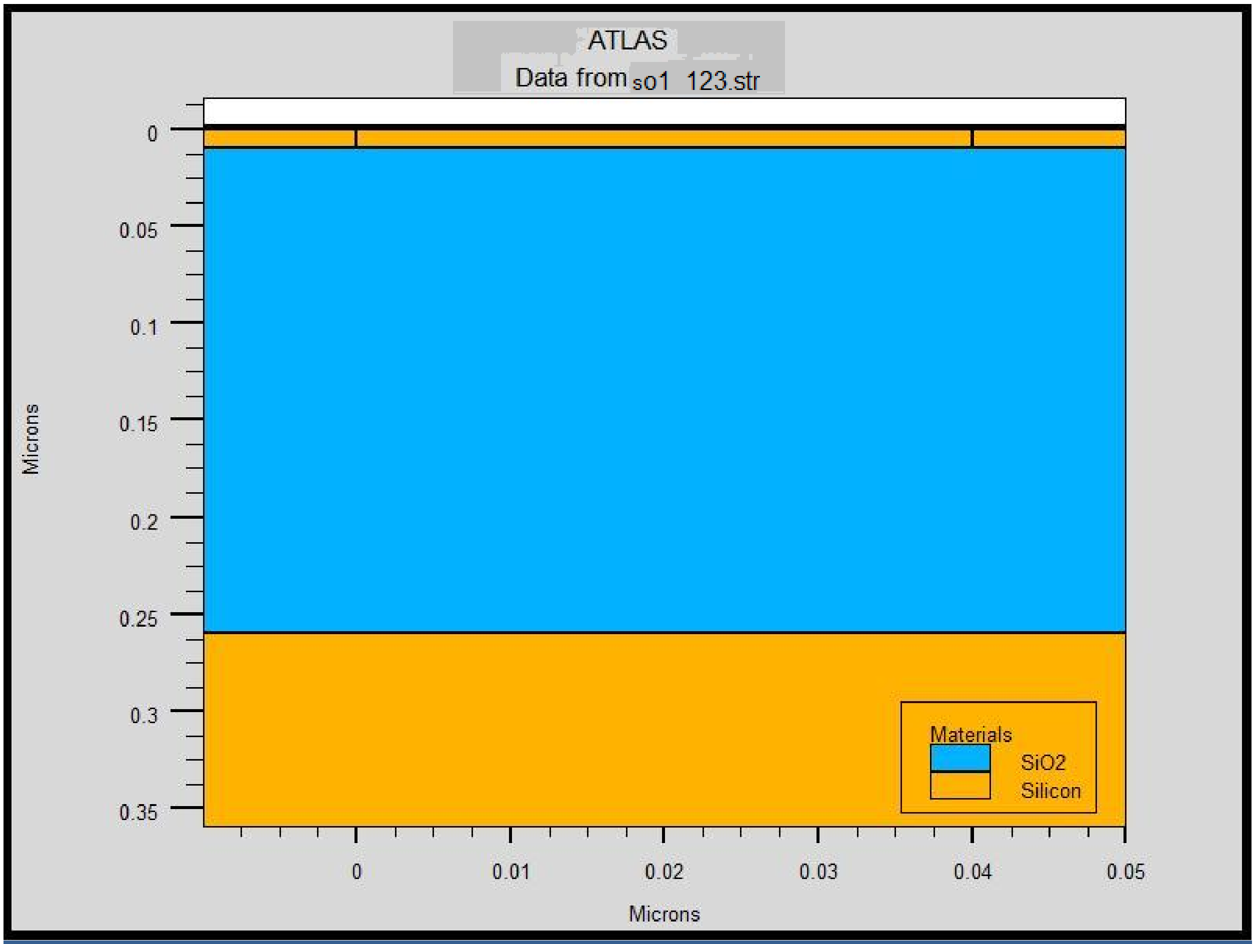


Fig. 3.1 Structure of SOI MOSFET of channel length 45nm

Reg. 1: SiO2 layer of LENGTH 2nm after the S/D/G

Reg. 2-gate of width 10nm and lengthth 40 nm

Reg. 3- SiO2 layer of width 250nm and length 60nm and

Reg. 4-substrate of si below insulator of length 60nm and width 100nm

Reg. 5-source region of width 10 nm and length 10nm

Reg. 6-drain region of width 10nm and width 10 nm

Hence by dividing the above structure into specific regions, we have been able to

In second reg. the concentration of doping is, p-type 2k x10^{14}

In fourth reg. the concentration of doping is, p-type 2k x10^{14}

In fifth reg. the n-type doping is 2x10^{20}

In sixth reg. the n-type doping is 2x10^{20}

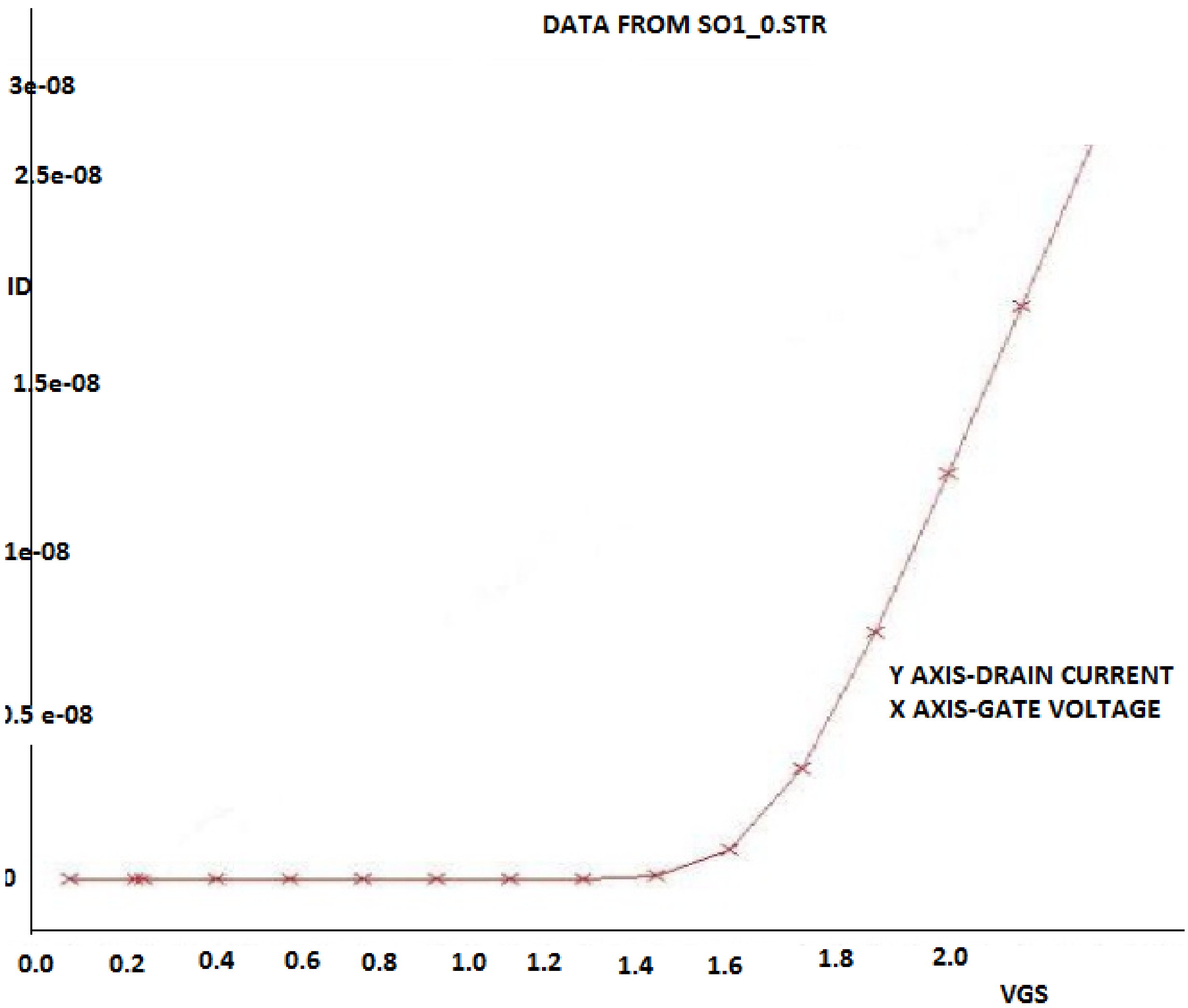


Fig. 3.2 Id v/s Vgs of SOI MOSFET

The above graph shows the relationship between drain current and gate voltage of conventional SOI MOSFET.

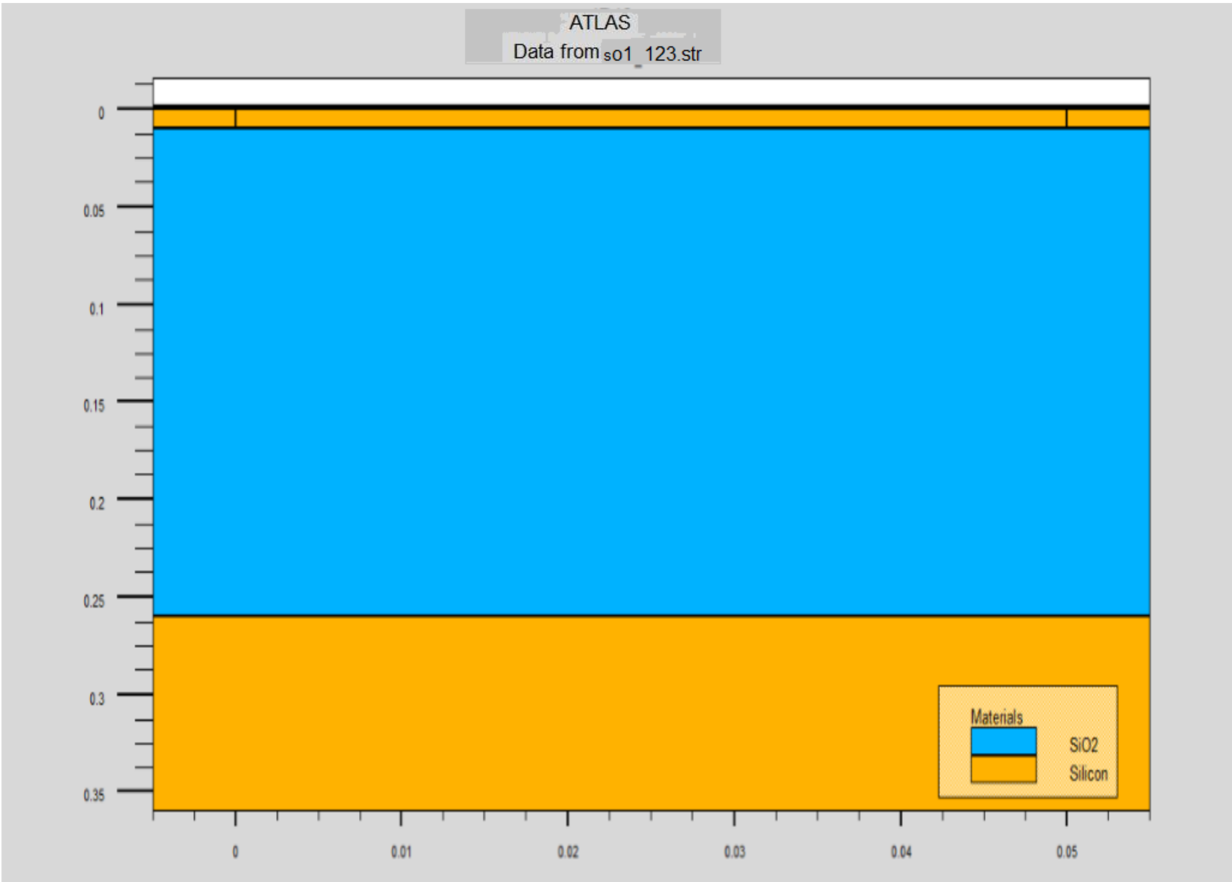


Fig. 3.3 Structure of SOI MOSFET of channel length 55nm

3.2 STRUCRURE OF DOUBLE GATE FET-

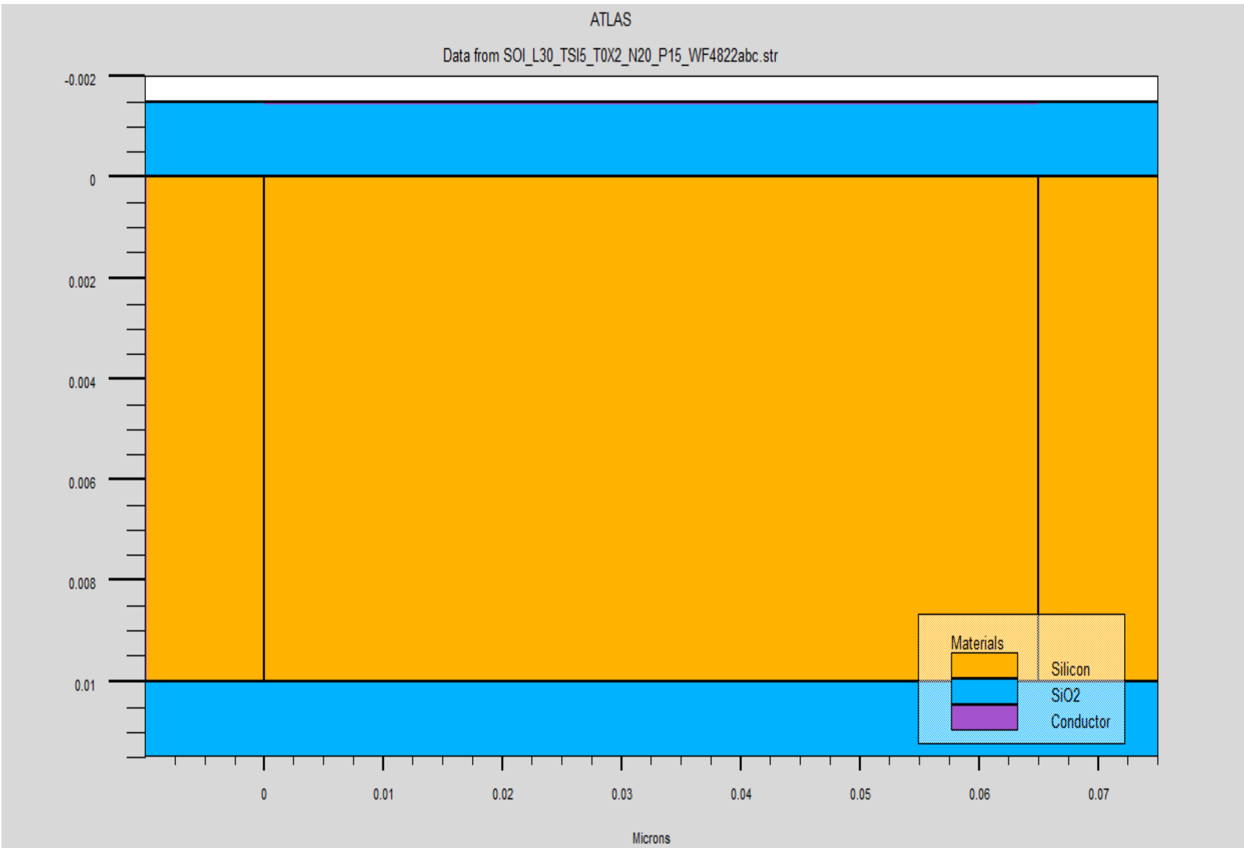


Fig. 3.4 simulated structure of DG FET

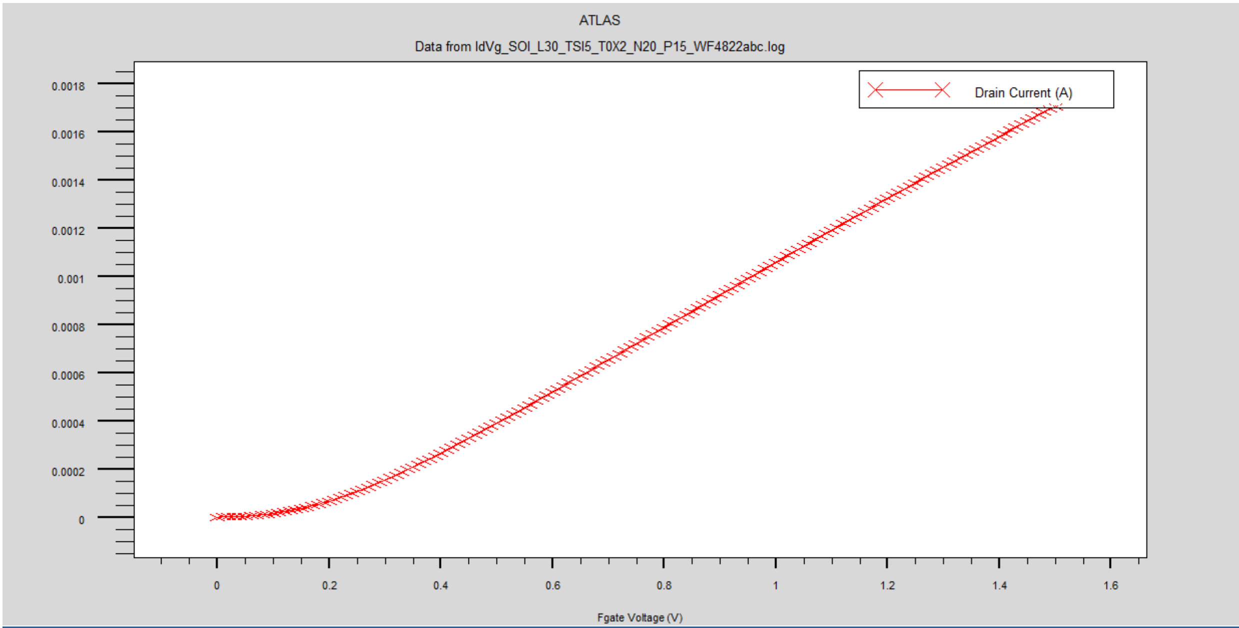


Fig. 3.5 Id v/s Vgs of DG FET

The above structure is generated for double gate FET by defining it's parameters in the same as previous one. And this shows the relationship between drain current and gate voltage..

3.3 COMPARISON OF ELECTRICAL CHARCTERISTICS-

3.3.1 DRAIN CURRENT v/s Vgs-

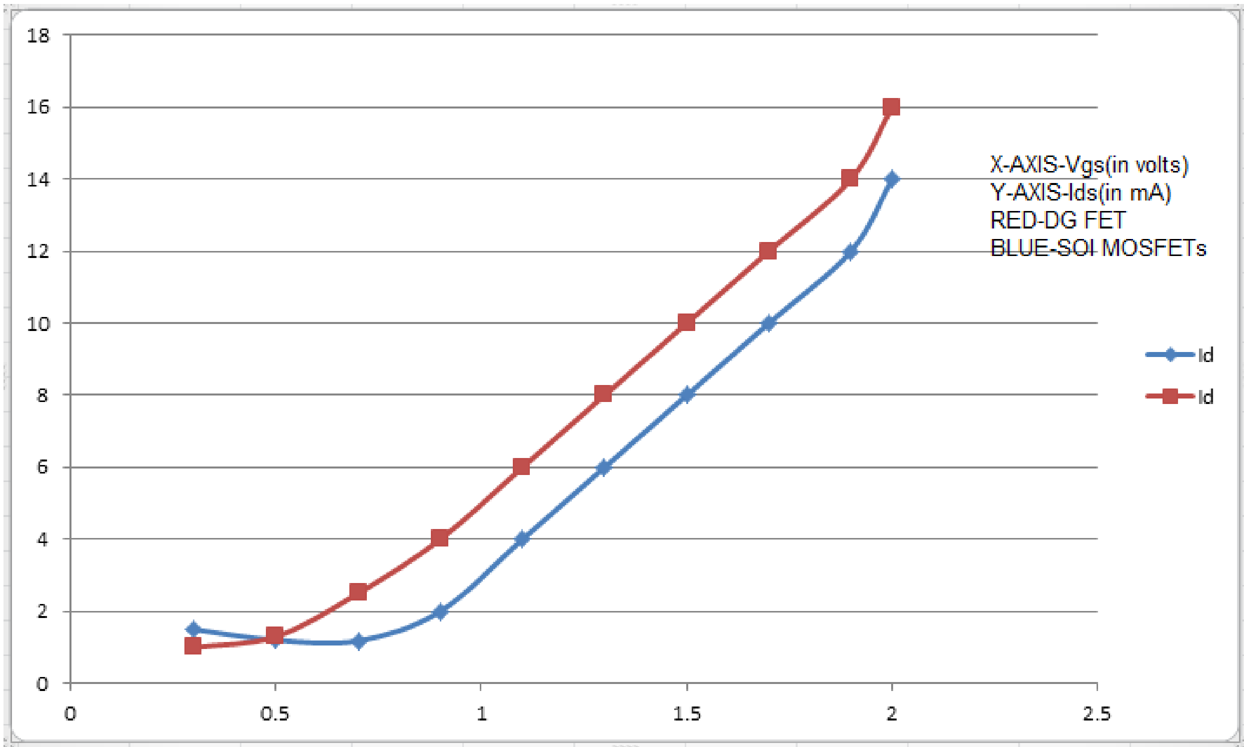


Fig. 3.6 Comparison of Id v/s Vgs

DISCUSSION-

After analyzing the results it is definitely clear that the drain current characteristics of DG FET are better than of SOI MOSFET. The presence of double gate drives the drain current to a higher value as compared to SOI MOSFET because of the higher resistance due to the substrate present near the channel. The DG FET has lower resistance and the movements of ions are more due to the potential applied from two gate terminals.

3.3.2 DRAIN CURRENT v/s Vds-

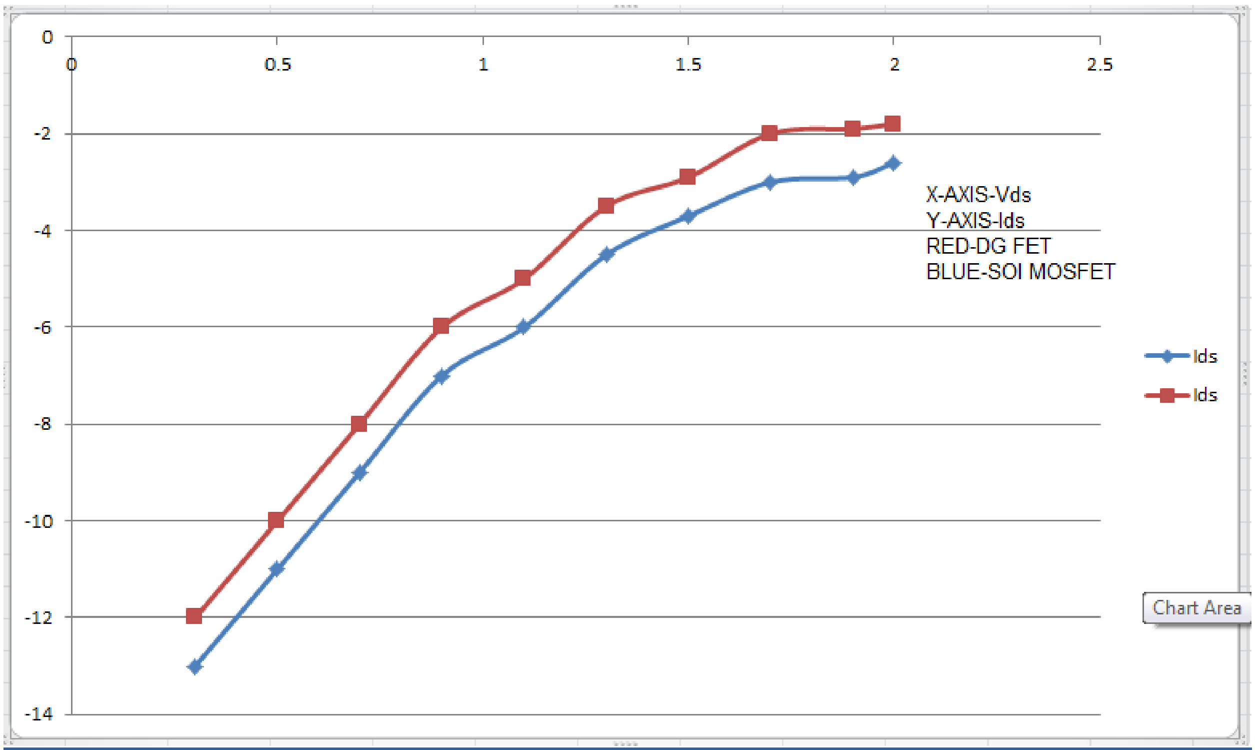


Fig. 3.7 Comparison of Id v/s Vds

DISCUSSION-

After analyzing the results it is definitely clear that the drain current characteristics of DG FET are better than of SOI MOSFET. The presence of double gate drives the drain current to a higher value as compared to SOI MOSFET because of the higher resistance due to the substrate present near the channel. The DG FET have lower resistance and the channel in is electrostatically isolated from the drain voltage so it gives better output.

3.3.3 SUB THRESHOLD SWING v/s CHANNEL LENGTH-

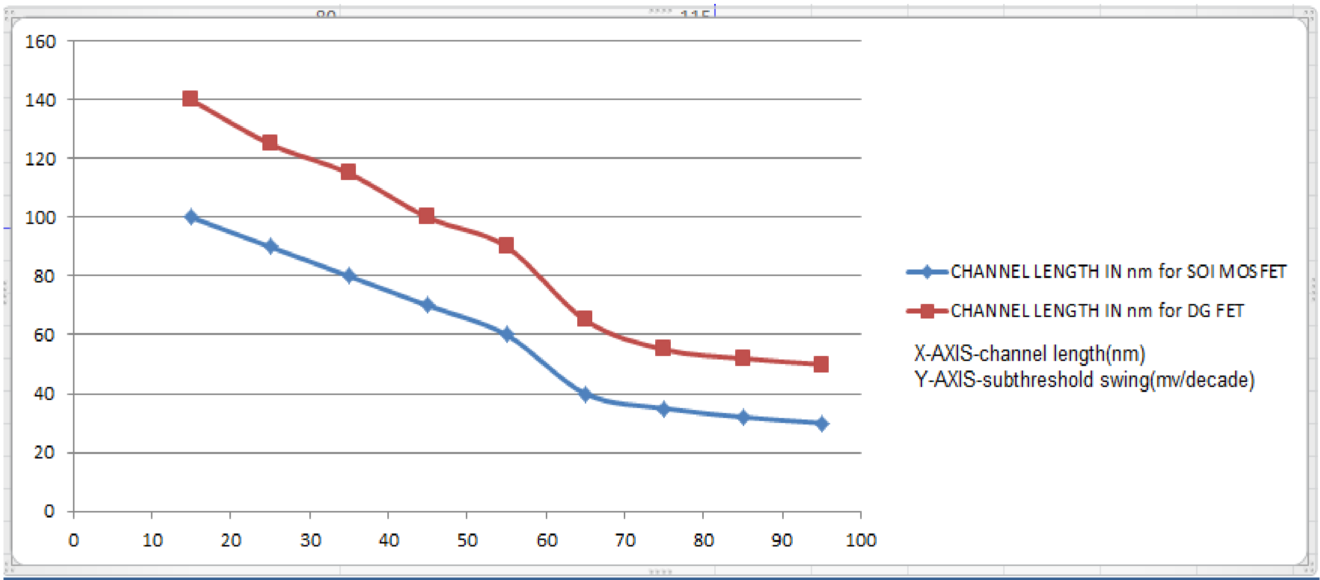


Fig. 3.8 Comparison of Sub Threshold Swing

DISCUSSION-

Sub threshold is the swing generated by the drain current when the gate voltage is varied or increased from zero to the threshold voltage. The fluctuation in drain current is measured in mv/decade and the x-axis is the channel length in nm. The swing in DG FET is lower than SOI MOSFET and which ideal characteristics for FET. For ideal transistor the drain current should be zero up to the threshold voltage. So we can conclude that DG FET successfully removes the sub threshold swing.

WORK FOR FUTURE-

As DG FETS and SOI MOSFETs have remarkably small structure it has promising future in VLSI and IC design. It's highly reliable, low cost ,has very less power dissipation and mostly very small range of size(Nano-scale) which will be very useful in designing complementary MOS circuit which has very large demand in electronics industry fulfilling all the requirements for sustainable design of ICs.Integrating with high packing consisting of large no of devices is a big goal to achieve. In near future if successful hardware implementation will be possible it will completely change the scenario of CMOS circuit design. Low energy consumption, low power dissipation, low scale size really needed for the future design and fabrication of ICs so future research work and development should be done to develop DG FETs and SOI MOSFETs.

CONCLUSION-

By analyzing we got the electrical characteristics and found that general MOSFET is affected by short channel effects like Barrier Lowering due to increase in drain voltage, impact ionization, ion scaterring.It is perfect place the deep source drain close enough before the gate edge to lower the resistance which is in series with the body due to reduced thin body. If we place the source & drain close together the FET will be more susceptible towards short channel effect. In double gate structure the parasitic capacitance is reduced quite remarkably.

Through experimental measurement, the DOUBLE GATE structure has many advantages over conventional SOI MOSFETs. A slight draw back in the DOUBLE GATE structure arises due to misalignments which can be optimized by careful design and simulation. There is also enhanced drain current output for DG FETs than conventional SOI MOSFETs. Overall the electrical characteristics are better than conventional SOI MOSFETs.

APPENDIX-

CODE FOR THE DG FET-

```
go atlas
Mesh space.mult=4.0
X.mesh loc=-0.010 spac=0.05
X.mesh loc=-0.0005001 spac=0.05
X.mesh loc=-0.0005 spac=0.0001
X.mesh loc=0.00 spac=0.0001
X.mesh loc=0.001 spac=0.0001
X.mesh loc=0.001001 spac=0.0002
X.mesh loc=.063999 spac=0.0002
X.mesh loc=.064 spac=0.0001
X.mesh loc=.065 spac=0.0001
X.mesh loc=.0655 spac=0.0001
X.mesh loc=.0655001 spac=0.05
X.mesh loc=.075 spac=0.05

Y.mesh loc=-.0015 spac=0.01
Y.mesh loc=-0.00001 spac=0.01
Y.mesh loc=0.00 spac=0.0001
Y.mesh loc=0.001 spac=0.0001
Y.mesh loc=0.001001 spac=0.0002
Y.mesh loc=.008999 spac=0.0002
Y.mesh loc=.009 spac=0.0005
Y.mesh loc=.010 spac=0.0005
Y.mesh loc=.01001 spac=0.0005
Y.mesh loc=.0115 spac=0.0005

Region number=1 x.min=-0.010 x.max=0.00 y.min=0.00 y.max=0.010 material=Silicon
```

Region number=2 x.min=0.065   x.max=0.075 y.min=0.00 y.max=0.010 material=Silicon

Region number=3 x.min=-0.010   x.max=0.075 y.min=-0.0015 y.max=0.00 material=SiO2

Region number=4 x.min=0.00 x.max=0.065 y.min=0.000 y.max=0.010   material=Silicon

Region number=5 x.min=-0.010 x.max=0.075 y.min=0.010 y.max=0.0115   material=SiO2

Electrode name=source number=1 x.min=-0.010 x.max=-0.010 y.min=0.000 y.max=0.010

Electrode name=drain number=2   x.min=0.075 x.max=0.075 y.min=0.000 y.max=0.010

Electrode name=fgate number=3 x.min=0.000 x.max=0.065 y.min=-0.0015 y.max=-0.0015

Electrode name=bgate number=4 x.min=0.000 x.max=0.065 y.min=0.0115 y.max=0.0115

doping uniform conc=1e20 n.type direction=y region=1

doping uniform conc=1e20 n.type direction=y region=2

doping uniform conc=1e17 p.type direction=y region=4

contact name=drain neutral

contact name=source neutral

contact name=fgate workfunction=4.25

contact name=bgate neutral

material material =Silicon EG300=1.08

material material =Silicon NC300=2.8e19

material material =Silicon NV300=1.04e19

material material =Silicon PERMITTIVITY=11.8

material material =Silicon MUN=2360

material material =Silicon AFFINITY=4.284

```
models srh analytic fldmob b.electrons=2 b.holes=1 evsatmod=0 hvsatmod=0 cvt \
        fermi print temperature=300

method   newton itlimit=25 trap atrap=0.5 maxtrap=4 autonr nrcriterion=0.1 \
        tol.time=0.005 dt.min=1e-25

solve init
solve vdrain=1
solve vdrain=0 vstep=0.01 vfinal=1 name=drain
solve vfgate=-.26
solve vbgate=-.24

log outf=IdVg_SOI_L30_TSI5_T0X2_N20_P15_WF4822abc.log

solve vfgate=0 vstep=0.01 vfinal=0.5 name=fgate

output band.param con.band val.band e.mobility ex.velocity ey.velocity e.velocity


save outf= SOI_L30_TSI5_T0X2_N20_P15_WF4822abc.str
tonyplot SOI_L30_TSI5_T0X2_N20_P15_WF4822abc.str
tonyplot IdVg_SOI_L30_TSI5_T0X2_N20_P15_WF4822abc.log


extract name="subvt_SOI_L30_TSI5_T0X2_N20_P15_WF4822abc"
1.0/slope(maxslope(curve(v."Fgate",log10(abs(i."drain")))))



quit
```

REFERENCES-

[1] Rohit S. Shenoy, Technology And scaling of Ultrathin body DOUBLE-GATE FETs.

[2] http://www.hindawi.com/journals/apec/2012/565827/fig1/ ,"Multiple Gate MOSFETs"

[3] C.-W. Lee, A. Afzalian, N. D. Akhavan, R. Yan, I. Ferain, and J.-P. Colinge, Appl. Phys. Lett. 94(5), 053511 (2009).

[4] Jean-Pierre Colinge," Multiple-gate SOI MOSFETs" Solid-State Electronics 48 (2004) 897–905.

[5] SILVACO, ATLAS User's Manual

[6] Semiconductor Devices , S.M. sze

[7] Power Electronics Semiconductor Device, Robert Parret

[8] A. Blake, M. White, A.-M. Kelleher, B. McCarthy, and R. Murphy, Nat. Nanotechnol. 5(3), 225–229 (2010), C.-W. Lee, A. Afzalian, N. D. Akhavan, R. Yan, I. Ferain, P. Razavi, B. O'Neil

[9] "TriGate MOSFETs & Dual-gate (FinFET) and: Simulation and design,", December 2003, K.P. Roenker