8.2 POWER TRANSISTORS

Objective: • Describe the characteristics of BJT and MOSFET power transistors, and analyze the temperature and heat flow characteristics of devices using heat sinks.

In our previous discussions, we have ignored any physical transistor limitations in terms of maximum current, voltage, and power. We implicitly assumed that the transistors were capable of handling the current and voltage, and could handle the power dissipated within the transistor without suffering any damage.

However, since we are now discussing power amplifiers, we must be concerned with transistor limitations. The limitations involve: maximum rated current (on the order of amperes), maximum rated voltage (on the order of 100 V), and maximum rated power (on the order of watts or tens of watts).[1] We will consider these effects in the BJT and then in the MOSFET. The maximum power limitation is related to the

maximum allowed temperature of the transistor, which in turn is a function of the rate at which heat is removed. We will therefore briefly consider heat sinks and heat flow.

8.2.1 Power BJTs

Power transistors are large-area devices. Because of differences in geometry and doping concentrations, their properties tend to vary from those of the small-signal devices. Table 8.1 compares the parameters of a general-purpose small-signal BJT to those of two power BJTs. The current gain is generally smaller in the power transistors, typically in the range of 20 to 100, and may be a strong function of collector current and temperature. Figure 8.1 shows typical current gain versus collector current characteristics for the 2N3055 power BJT at various temperatures. At high current levels, the current gain tends to drop off significantly, and parasitic resistances in the base and collector regions may become significant, affecting the transistor terminal characteristics.

The **maximum rated collector current** $I_{C,\text{rated}}$ may be related to: the maximum current that the wires connecting the semiconductor to the external terminals can handle; the collector current at which the current gain falls below a minimum specified value; or the current that leads to the maximum power dissipation when the transistor is in saturation.

Table 8.1 Comparison of the characteristics and maximum ratings of a small-signal and power BJT

Parameter	Small-Signal BJT (2N2222A)	Power BJT (2N3055)	Power BJT (2N6078)
V_{CE}(max) (V)	40	60	250
I_C(max) (A)	0.8	15	7
P_D(max) (W) (at $T = 25$ °C)	1.2	115	45
β	35–100	5–20	12–70
f_T (MHz)	300	0.8	1

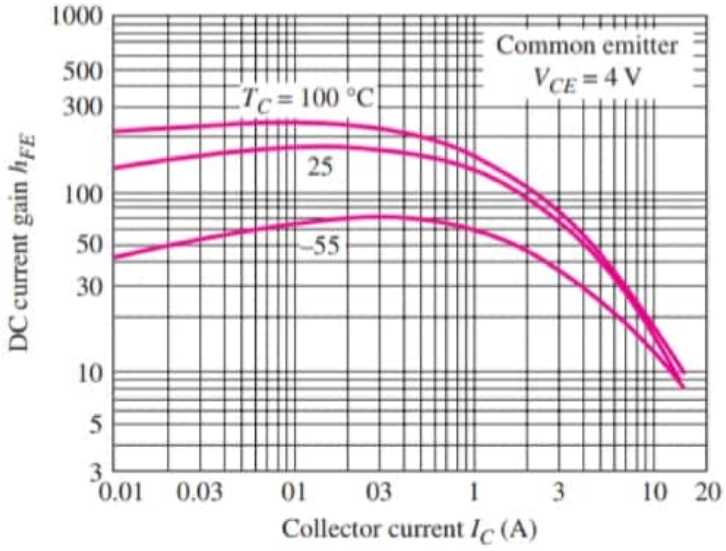

Figure 8.1 Typical dc beta characteristics (h_{FE} versus I_C) for 2N3055

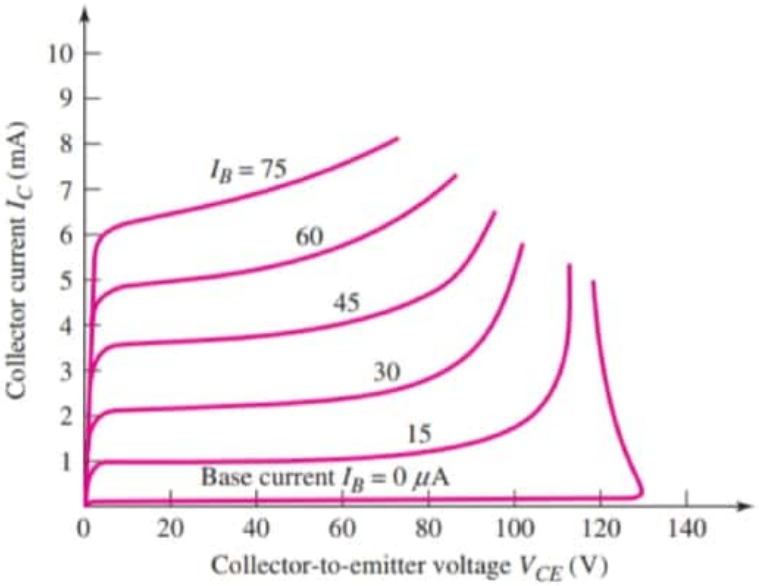

Figure 8.2 Typical collector current versus collector–emitter voltage characteristics of a bipolar transistor, showing breakdown effects

The maximum voltage limitation in a BJT is generally associated with avalanche breakdown in the reverse-biased base–collector junction. In the common-emitter configuration, the breakdown voltage mechanism also involves the transistor gain, as well as the breakdown phenomenon on the pn junction. Typical I_C versus V_{CE} characteristics are shown in Figure 8.2. The breakdown voltage when the base terminal is open circuited ($I_B = 0$) is V_{CEO}. From the data in Figure 8.2, this value is approximately 130 V.

When the transistor is biased in the active region, the collector current begins to increase significantly before breakdown voltage V_{CEO} is reached, and all the curves tend to merge to the same collector–emitter voltage once breakdown has occurred. The voltage at which these curves merge is denoted $V_{CE(\text{sus})}$ and is the minimum voltage necessary to sustain the transistor in breakdown. From the data in Figure 8.2, the value of $V_{CE(\text{sus})}$ is approximately 115 V.

Another breakdown effect is called **second breakdown,** which occurs in a BJT operating at high voltage and a fairly high current. Slight nonuniformities in current density produce local regions of increased heating that decreases the resistance of the semiconductor material, which in turn increases the current in those regions. This effect results in positive feedback, and the current continues to increase, producing a further increase in temperature, until the semiconductor material may actually melt, creating a short circuit between the collector and emitter and producing a permanent failure.

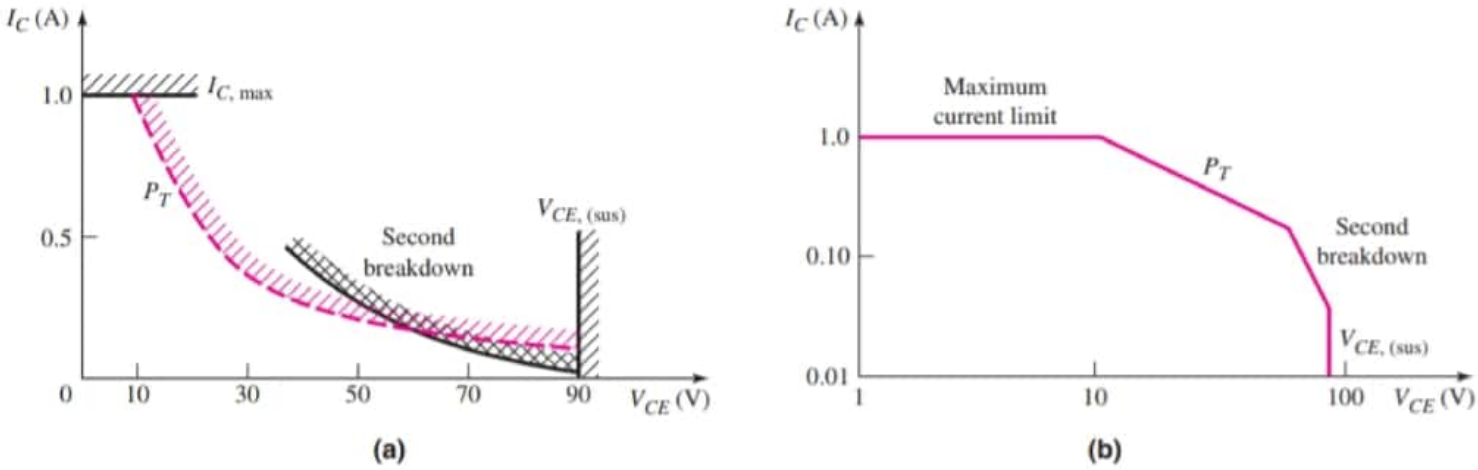

Figure 8.3 The safe operating area of a bipolar transistor plotted on: (a) linear scales and (b) logarithmic scales

The average power dissipated in a BJT must be kept below a specified maximum value, to ensure that the temperature of the device remains below a maximum value. If we assume that the collector current and collector–emitter voltage are dc quantities, then at the **maximum rated power** P_T for the transistor, we can write

$$P_T = V_{CE} I_C \tag{8.4}$$

The maximum current, voltage, and power limitations can be illustrated on the I_C versus V_{CE} characteristics, as shown in Figure 8.3. The average power limitation P_T is a hyperbola described by Equation (8.4). The region where the transistor can be operated safely is known as the **safe operating area (SOA)** and is bounded by $I_{C,\max}$, $V_{CE(\text{sus})}$, P_T, and the transistor's second breakdown characteristics curve. Figure 8.3(a) shows the safe operating area, using linear current and voltage scales; Figure 8.3(b) shows the same characteristics using logarithmic scales.

The i_C–v_{CE} operating point may move momentarily outside the safe operating area without damaging the transistor, but this depends on how far the Q-point moves outside the area and for how long. For our purposes, we will assume that the device must remain within the safe operating area at all times.

EXAMPLE 8.1

Objective: Determine the required current, voltage, and power ratings of a power BJT.

Consider the common-emitter circuit in Figure 8.4. The parameters are $R_L = 8\ \Omega$ and $V_{CC} = 24$ V.

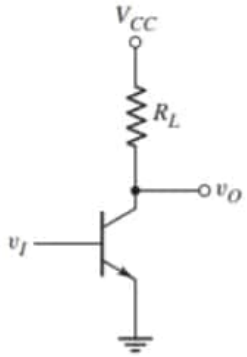

Figure 8.4 Figure for Example 8.1

Solution: For $V_{CE} \cong 0$, the maximum collector current is

$$I_C(\max) = \frac{V_{CC}}{R_L} = \frac{24}{8} = 3\text{ A}$$

For $I_C = 0$, the maximum collector–emitter voltage is

$$V_{CE}(\max) = V_{CC} = 24\text{ V}$$

The load line is given by

$$V_{CE} = V_{CC} - I_C R_L$$

and must remain within the safe operating area, as shown in Figure 8.5.

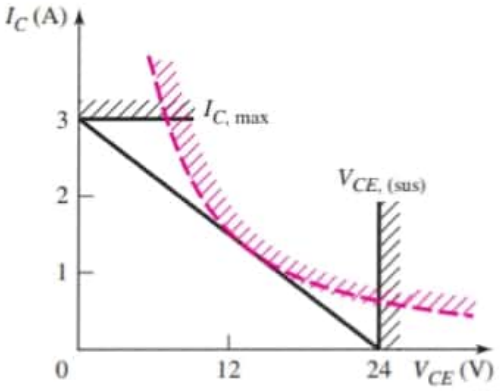

Figure 8.5 DC load line within the safe operating area

The transistor power dissipation is therefore

$$P_T = V_{CE}I_C = (V_{CC} - I_C R_L)I_C = V_{CC}I_C - I_C^2 R_L$$

The current at which the maximum power occurs is found by setting the derivative of this equation equal to zero as follows:

$$\frac{dP_T}{dI_C} = 0 = V_{CC} - 2I_C R_L$$

which yields

$$I_C = \frac{V_{CC}}{2R_L} = \frac{24}{2(8)} = 1.5\,\text{A}$$

The C–E voltage at the maximum power point is

$$V_{CE} = V_{CC} - I_C R_L = 24 - (1.5)(8) = 12\,\text{V}$$

The maximum power dissipation in the transistor occurs at the center of the load line. The maximum transistor power dissipation is therefore

$$P_T = V_{CE}I_C = 12(1.5) = 18\,\text{W}$$

Comment: To find a transistor for a given application, safety factors are normally used. For this example, a transistor with a current rating greater than 3 A, a voltage rating greater than 24 V, and a power rating greater than 18 W would be required.

8.2.2 Power MOSFETs

Table 8.2 lists the basic parameters of two n-channel power MOSFETs. The drain currents are in the ampere range and the breakdown voltages are in the hundreds of volts range. These transistors must also operate within a safe operating area as discussed for the BJTs.

Table 8.2 Characteristics of two power MOSFETs

Parameter	2N6757	2N6792
V_{DS}(max) (V)	150	400
I_D(max) (at $T = 25\,^{\circ}C$)	8	2
P_D (W)	75	20

Power MOSFETs differ from bipolar power transistors both in operating principles and performance. The superior performance characteristics of power MOSFETs are: faster switching times, no second breakdown, and stable gain and response time over a wide temperature range. Figure 8.7(a) shows the transconductance

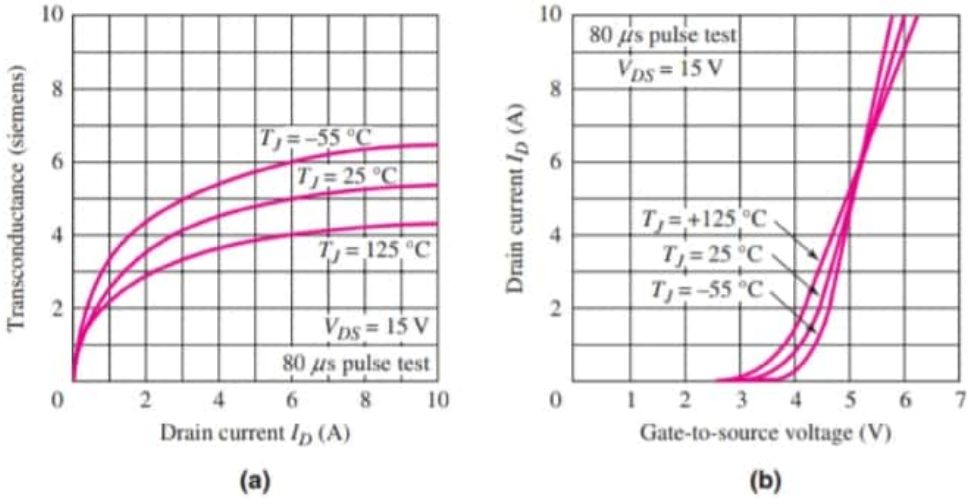

Figure 8.7 Typical characteristics for high-power MOSFETs: (a) transconductance versus drain current; (b) transfer characteristics

of the 2N6757 versus temperature. The variation with temperature of the MOSFET transconductance is less than the variation in the BJT current gain shown in Figure 8.1.

Power MOSFETs are often manufactured by a vertical or double-diffused process, called VMOS or DMOS, respectively. The cross section of a VMOS device is shown in Figure 8.8(a) and the cross section of the DMOS device is shown in Figure 8.8(b). The DMOS process can be used to produce a large number of closely packed hexagonal cells on a single silicon chip, as shown in Figure 8.8(c). Also, such MOSFETs can be paralleled to form large-area devices, without the need of an equivalent emitter ballast resistance to equalize the current density. A single power MOSFET chip may contain as many as 25,000 paralleled cells.

Since the path between the drain and the source is essentially resistive, the **on resistance** $r_{ds}(\text{on})$ is an important parameter in the power capability of a MOSFET. Figure 8.9 shows a typical $r_{ds}(\text{on})$ characteristic as a function of drain current. Values in the tens of milliohm range have been obtained.

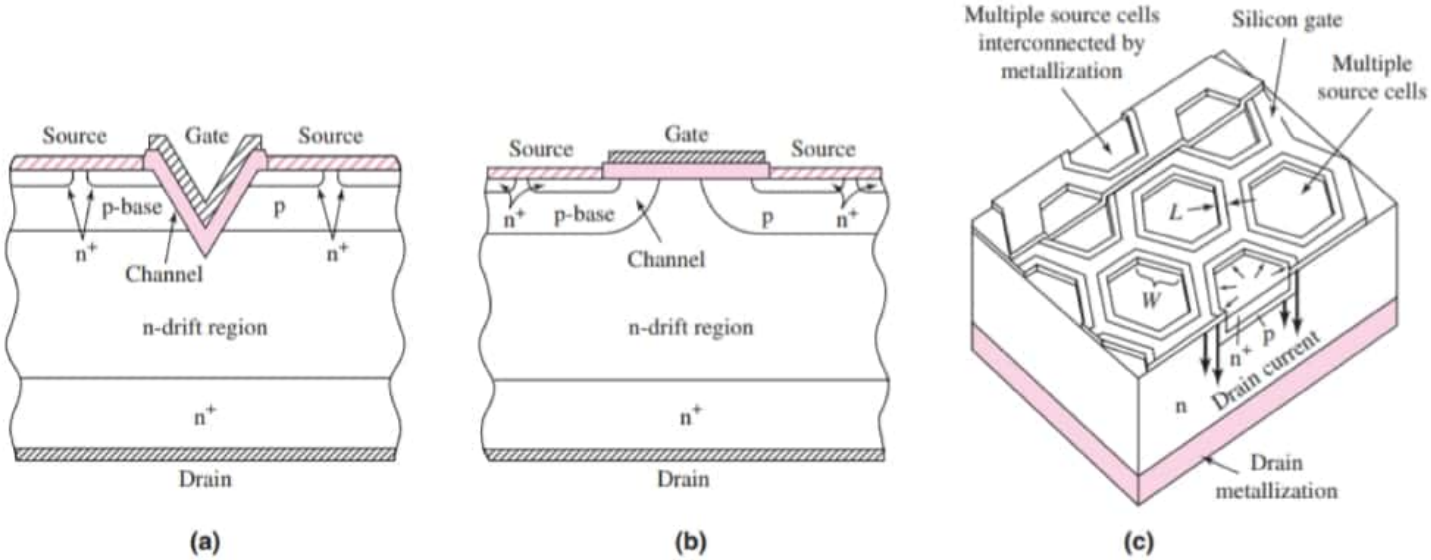

Figure 8.8 (a) Cross section of a VMOS device; (b) cross section of DMOS device; (c) HEXFET structure

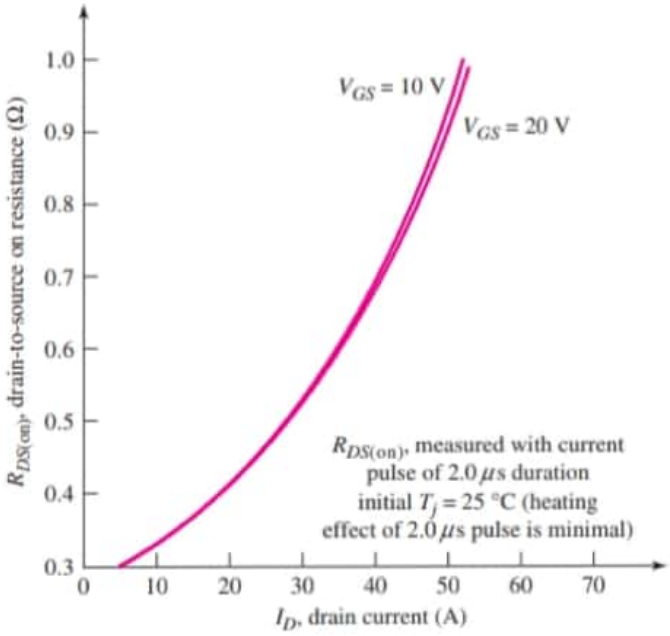

Figure 8.9 Typical drain-to-source resistance versus drain current characteristics of a MOSFET

8.2.3 Comparison of Power MOSFETs and BJTs

Since a MOSFET is a high input impedance, voltage-controlled device, the drive circuitry is simpler. The gate of a 10 A power MOSFET may be driven by the output of a standard logic circuit. In contrast, if the current gain of a 10 A BJT is $\beta = 10$, then a base current of 1 A is required for a collector current of 10 A. However, this required input current is much larger than the output drive capability of most logic circuits, which means that the drive circuitry for power BJTs is more complicated.

The MOSFET is a majority carrier device. Majority carrier mobility decreases with increasing temperature, which makes the semiconductor more resistive. This means that MOSFETs are more immune to the thermal runaway effects and second breakdown phenomena experienced in bipolars. Figure 8.7(b) shows typical I_D versus V_{GS} characteristics at several temperatures, clearly demonstrating that at high current levels, the current actually decreases with increasing temperature, for a given gate-to-source voltage.

8.2.4 Heat Sinks

The power dissipated in a transistor increases its internal temperature above the ambient temperature. If the device or junction temperature T_j becomes too high, the transistor may suffer permanent damage. Special precautions must be taken in packaging power transistors and in providing heat sinks so that heat can be conducted from the transistor. Figures 8.10(a) and (b) show two packaging schemes, and Figure 8.10(c) shows a typical heat sink.

To design a heat sink for a power transistor, we must first consider the concept of **thermal resistance** θ, which has units of °C/W. The temperature difference, $T_2 - T_1$, across an element with a thermal resistance θ is

$$T_2 - T_1 = P\theta \tag{8.5}$$

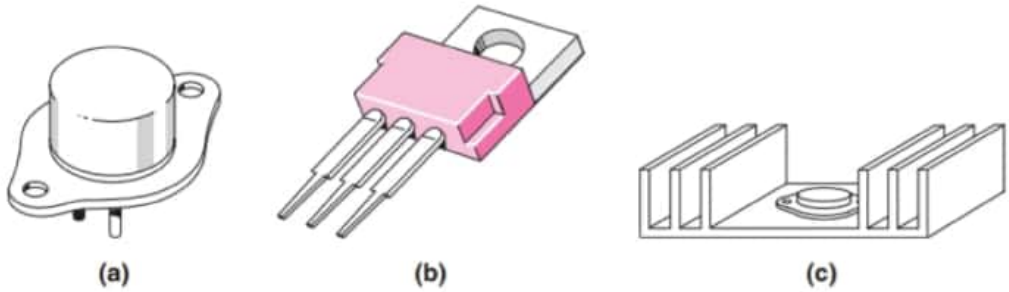

Figure 8.10 Two packaging schemes: (a) and (b) for power transistors and (c) typical heat sink

where P is the thermal power through the element. Temperature difference is the electrical analog of voltage, and power or heat flow is the electrical analog of current.

Manufacturers' data sheets for power devices generally give the maximum operating junction or device temperature $T_{j,\max}$ and the thermal resistance from the junction to the case $\theta_{jc} = \theta_{\text{dev-case}}$.[2] By definition, the thermal resistance between the case and heat sink is $\theta_{\text{case-snk}}$, and between the heat sink and ambient is $\theta_{\text{snk-amb}}$.

The temperature difference between the device and the ambient can now be written as follows, when a heat sink is used:

$$T_{\text{dev}} - T_{\text{amb}} = P_D(\theta_{\text{dev-case}} + \theta_{\text{case-snk}} + \theta_{\text{snk-amb}}) \tag{8.6}$$

where P_D is the power dissipated in the device. Equation (8.6) may also be modeled by its equivalent electrical elements, as shown in Figure 8.11. The temperature difference across the elements, such as the case and heat sink, is the dissipated power P_D multiplied by the applicable thermal resistance, which is $\theta_{\text{case-snk}}$ for this example.

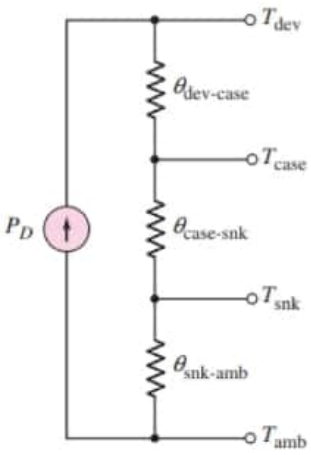

Figure 8.11 Electrical equivalent circuit for heat flow from the device to the ambient

If a heat sink is not used, the temperature difference between the device and ambient is written as

$$T_{\text{dev}} - T_{\text{amb}} = P_D(\theta_{\text{dev-case}} + \theta_{\text{case-amb}}) \tag{8.7}$$

where $\theta_{\text{case-amb}}$ is the thermal resistance between the case and ambient.

EXAMPLE 8.2

Objective: Determine the maximum power dissipation in a transistor and determine the temperature of the transistor case and heat sink.

Consider a power MOSFET for which the thermal resistance parameters are:

$\theta_{\text{dev-case}} = 1.75\,^\circ\text{C/W}$ $\quad$ $\theta_{\text{case-snk}} = 1\,^\circ\text{C/W}$

$\theta_{\text{snk-amb}} = 5\,^\circ\text{C/W}$ $\quad$ $\theta_{\text{case-amb}} = 50\,^\circ\text{C/W}$

The ambient temperature is $T_{\text{amb}} = 30\,^\circ\text{C}$, and the maximum junction or device temperature is $T_{j,\max} = T_{\text{dev}} = 150\,^\circ\text{C}$.

Solution (Maximum Power): When no heat sink is used, the maximum device power dissipation is found from Equation (8.7) as

$$P_{D,\max} = \frac{T_{j,\max} - T_{\text{amb}}}{\theta_{\text{dev-case}} + \theta_{\text{case-amb}}} = \frac{150 - 30}{1.75 + 50} = 2.32\,\text{W}$$

When a heat sink is used, the maximum device power dissipation is found from Equation (8.6) as

$$P_{D,\max} = \frac{T_{j,\max} - T_{\text{amb}}}{\theta_{\text{dev-case}} + \theta_{\text{case-snk}} + \theta_{\text{snk-amb}}}$$
$$= \frac{150 - 30}{1.75 + 1 + 5} = 15.5\,\text{W}$$

Solution (Temperature): The device temperature is $T = 150\ ^\circ\text{C}$ and the ambient temperature is $T_{\text{amb}} = 30\ ^\circ\text{C}$. The heat flow is $P_D = 15.5$ W. The heat sink temperature (see Figure 8.11) is found from

$$T_{\text{snk}} - T_{\text{amb}} = P_D \cdot \theta_{\text{snk-amb}}$$

or

$$T_{\text{snk}} = 30 + (15.5)(5) \Rightarrow T_{\text{snk}} = 107.5\,^\circ\text{C}$$

The case temperature is found from

$$T_{\text{case}} - T_{\text{amb}} = P_D \cdot (\theta_{\text{case-snk}} + \theta_{\text{snk-case}})$$

or

$$T_{\text{case}} = 30 + (15.5)(1 + 5) \Rightarrow T = 123\,^\circ\text{C}$$

Comment: These results illustrate that the use of a heat sink allows more power to be dissipated in the device, while keeping the device temperature at or below its maximum limit.