11.7 Power BJTs

Transistors that are required to conduct currents in the ampere range and to withstand power dissipation in the watts and tens-of-watts ranges differ in their physical structure, packaging, and specification from the small-signal transistors considered in earlier chapters. In this section we consider some of the important properties of power transistors, especially those

aspects that pertain to the design of circuits of the type discussed earlier. There are, of course, other important applications of power transistors, such as their use as switching elements in power inverters and motor-control circuits. Such applications are not studied in this book.

11.7.1 Junction Temperature

Power transistors dissipate large amounts of power in their collector–base junctions. The dissipated power is converted into heat, which raises the junction temperature. However, the junction temperature T_J must not be allowed to exceed a specified maximum, T_{Jmax}; otherwise the transistor could suffer permanent damage. For silicon devices, T_{Jmax} is in the range of 150°C to 200°C.

11.7.2 Thermal Resistance

Consider first the situation of a transistor operating in free air—that is, with no special arrangements for cooling. The heat dissipated in the transistor junction will be conducted away from the junction to the transistor case, and from the case to the surrounding environment. In a steady state in which the transistor is dissipating P_D watts, the temperature rise of the junction relative to the surrounding ambience can be expressed as

$$T_J - T_A = \theta_{JA} P_D \tag{11.69}$$

where θ_{JA} is the **thermal resistance** between junction and ambience, having the units of degrees Celsius per watt. Note that θ_{JA} simply gives the rise in junction temperature over the ambient temperature for each watt of dissipated power. Since we wish to be able to dissipate large amounts of power without raising the junction temperature above T_{Jmax}, it is desirable to have, for the thermal resistance θ_{JA}, as small a value as possible. For operation in free air, θ_{JA} depends primarily on the type of case in which the transistor is packaged. The value of θ_{JA} is usually specified on the transistor data sheet.

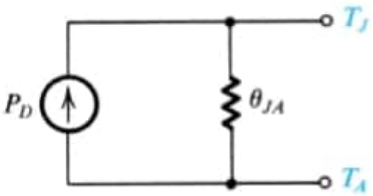

Figure 11.23 Electrical equivalent circuit of the thermal-conduction process; $T_J - T_A = P_D \theta_{JA}$.

Equation (11.69), which describes the thermal-conduction process, is analogous to Ohm's law, which describes the electrical-conduction process. In this analogy, power dissipation corresponds to current, temperature difference corresponds to voltage difference, and thermal resistance corresponds to electrical resistance. Thus, we may represent the thermal-conduction process by the electric circuit shown in Fig. 11.23.

11.7.3 Power Dissipation Versus Temperature

The transistor manufacturer usually specifies the maximum junction temperature T_{Jmax}, the maximum power dissipation at a particular ambient temperature T_{A0} (usually, 25°C), and the

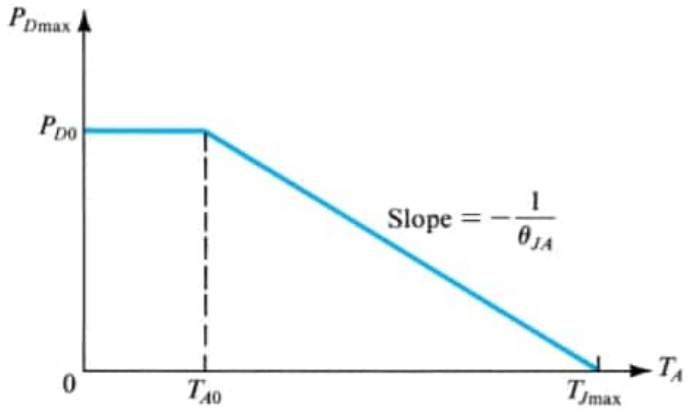

Figure 11.24 Maximum allowable power dissipation versus ambient temperature for a BJT operated in free air. This is known as a "power-derating" curve.

thermal resistance θ_{JA}. In addition, a graph such as that shown in Fig. 11.24 is usually provided. The graph simply states that for operation at ambient temperatures below T_{A0}, the device can safely dissipate the rated value of P_{D0} watts. However, if the device is to be operated at higher ambient temperatures, the maximum allowable power dissipation must be **derated** according to the straight line shown in Fig. 11.24. The **power-derating curve** is a graphical representation of Eq. (11.69). Specifically, note that if the ambient temperature is T_{A0} and the power dissipation is at the maximum allowed (P_{D0}), then the junction temperature will be T_{Jmax}. Substituting these quantities in Eq. (11.69) results in

$$\theta_{JA} = \frac{T_{Jmax} - T_{A0}}{P_{D0}} \tag{11.70}$$

which is the inverse of the slope of the power-derating straight line. At an ambient temperature T_A, higher than T_{A0}, the maximum allowable power dissipation P_{Dmax} can be obtained from Eq. (11.69) by substituting $T_J = T_{Jmax}$; thus,

$$P_{Dmax} = \frac{T_{Jmax} - T_A}{\theta_{JA}} \tag{11.71}$$

Observe that as T_A approaches T_{Jmax}, the allowable power dissipation decreases; the lower thermal gradient limits the amount of heat that can be removed from the junction. In the extreme situation of $T_A = T_{Jmax}$, no power can be dissipated because no heat can be removed from the junction.

Example 11.7

A BJT is specified to have a maximum power dissipation P_{D0} of 2 W at an ambient temperature T_{A0} of 25°C, and a maximum junction temperature T_{Jmax} of 150°C. Find the following:

(a) The thermal resistance θ_{JA}.
(b) The maximum power that can be safely dissipated at an ambient temperature of 50°C.
(c) The junction temperature if the device is operating at $T_A = 25$°C and is dissipating 1 W.

Example 11.7 *continued*

Solution

(a) $\theta_{JA} = \dfrac{T_{J\max} - T_{A0}}{P_{D0}} = \dfrac{150 - 25}{2} = 62.5°\text{C/W}$

(b) $P_{D\max} = \dfrac{T_{J\max} - T_A}{\theta_{JA}} = \dfrac{150 - 50}{62.5} = 1.6\ \text{W}$

(c) $T_J = T_A + \theta_{JA} P_D = 25 + 62.5 \times 1 = 87.5°\text{C}$

11.7.4 Transistor Case and Heat Sink

The thermal resistance between junction and ambience, θ_{JA}, can be expressed as

$$\theta_{JA} = \theta_{JC} + \theta_{CA} \tag{11.72}$$

where θ_{JC} is the thermal resistance between junction and transistor case (package) and θ_{CA} is the thermal resistance between case and ambience. For a given transistor, θ_{JC} is fixed by the device design and packaging. The device manufacturer can reduce θ_{JC} by encapsulating the device in a relatively large metal case and placing the collector (where most of the heat is dissipated) in direct contact with the case. Most high-power transistors are packaged in this fashion. Figure 11.25 shows a sketch of a typical package.

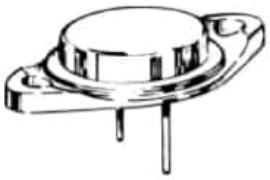

Figure 11.25 The popular TO3 package for power transistors. The case is metal with a diameter of about 2.2 cm; the outside dimension of the "seating plane" is about 4 cm. The seating plane has two holes for screws to bolt it to a heat sink. The collector is electrically connected to the case. Therefore an electrically insulating but thermally conducting spacer is used between the transistor case and the "heat sink."

Although the circuit designer has no control over θ_{JC} (once a particular transistor has been selected), the designer can considerably reduce θ_{CA} below its free-air value (specified by the manufacturer as part of θ_{JA}). Reduction of θ_{CA} can be effected by providing means to facilitate heat transfer from case to ambience. A popular approach is to bolt the transistor to the chassis or to an extended metal surface. Such a metal surface then functions as a **heat sink**. Heat is easily conducted from the transistor case to the heat sink; that is, the thermal resistance θ_{CS} is usually very small. Also, heat is efficiently transferred (by convection and radiation) from the heat sink to the ambience, resulting in a low thermal resistance θ_{SA}. Thus, if a heat sink is utilized, the case-to-ambience thermal resistance given by

$$\theta_{CA} = \theta_{CS} + \theta_{SA} \tag{11.73}$$

can be small because its two components can be made small by the choice of an appropriate heat sink.[2] For example, in very high-power applications the heat sink is usually equipped with fins that further facilitate cooling by radiation and convection.

[2]As noted earlier, the metal case of a power transistor is electrically connected to the collector. Thus an electrically insulating material such as mica is usually placed between the metal case and the metal heat sink. Also, insulating bushings and washers are generally used in bolting the transistor to the heat sink.

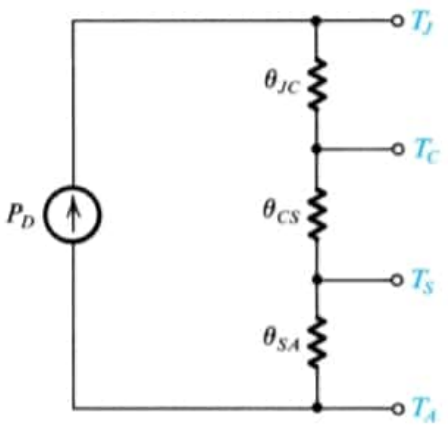

Figure 11.26 Electrical analog of the thermal conduction process when a heat sink is utilized.

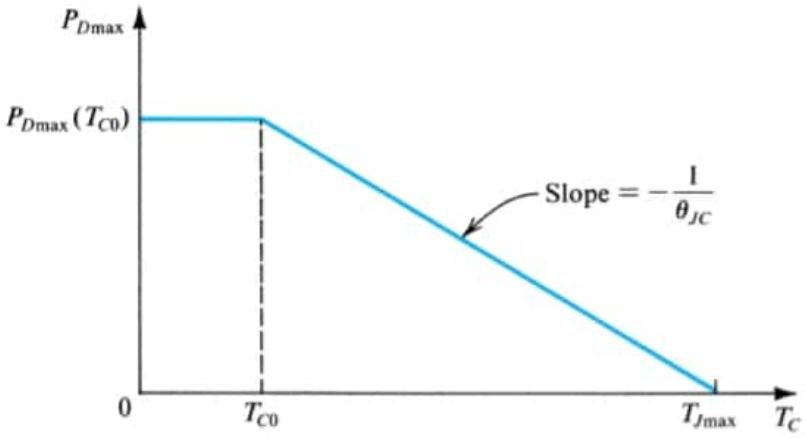

Figure 11.27 Maximum allowable power dissipation versus transistor-case temperature.

The electrical analog of the thermal-conduction process when a heat sink is employed is shown in Fig. 11.26, from which we can write

$$T_J - T_A = P_D(\theta_{JC} + \theta_{CS} + \theta_{SA}) \tag{11.74}$$

As well as specifying θ_{JC}, the device manufacturer usually supplies a derating curve for $P_{D\max}$ versus the case temperature, T_C. Such a curve is shown in Fig. 11.27. Note that the slope of the power-derating straight line is $-1/\theta_{JC}$. For a given transistor, the maximum power dissipation at a *case temperature* T_{C0} (usually 25°C) is much greater than that at an *ambient temperature* T_{A0} (usually 25°C). If the device can be maintained at a case temperature T_C, $T_{C0} \le T_C \le T_{J\max}$, then the maximum safe power dissipation is obtained when $T_J = T_{J\max}$,

$$P_{D\max} = \frac{T_{J\max} - T_C}{\theta_{JC}} \tag{11.75}$$

11.7.5 The BJT Safe Operating Area

In addition to specifying the maximum power dissipation at different case temperatures, power-transistor manufacturers usually provide a plot of the boundary of the safe operating area (SOA) in the i_C–v_{CE} plane. The SOA specification takes the form illustrated by the sketch in Fig. 11.29; the following paragraph numbers correspond to the boundaries on the sketch.

1. The maximum allowable current I_{Cmax}. Exceeding this current on a continuous basis can result in melting the wires that bond the device to the package terminals.
2. The maximum power dissipation hyperbola. This is the locus of the points for which $v_{CE}i_C = P_{Dmax}$ (at T_{C0}). For temperatures $T_C > T_{C0}$, the power-derating curves described in Section 11.7.4 should be used to obtain the applicable P_{Dmax} and thus a correspondingly lower hyperbola. Although the operating point can be allowed to move temporarily above the hyperbola, the *average* power dissipation should not be allowed to exceed P_{Dmax}.
3. The **second-breakdown** limit. Second breakdown is a phenomenon that results because current flow across the emitter–base junction is not uniform. Rather, the current density is greatest near the periphery of the junction. This "**current crowding**" gives rise to increased localized power dissipation and hence temperature rise (at locations called **hot spots**). Since a temperature rise causes an increase in current, a localized form of **thermal runaway** can occur, leading to junction destruction.

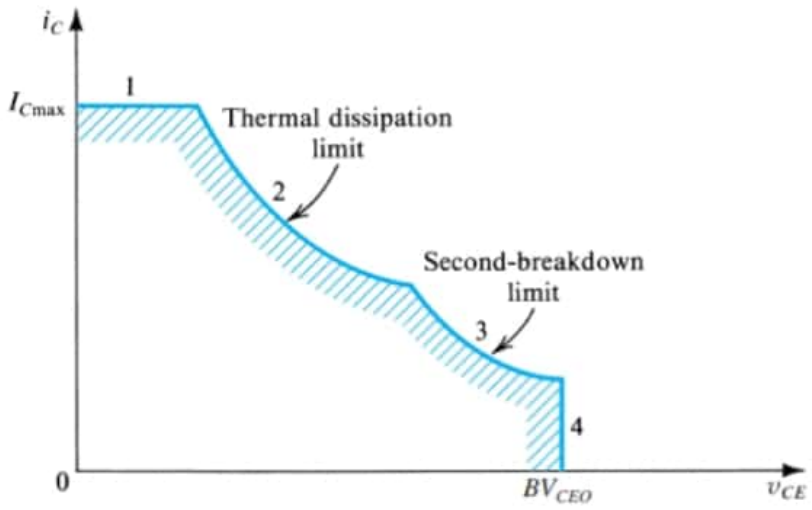

Figure 11.29 Safe operating area (SOA) of a BJT.

4. The collector-to-emitter breakdown voltage, BV_{CEO}. The instantaneous value of v_{CE} should never be allowed to exceed BV_{CEO}; otherwise, avalanche breakdown of the collector–base junction may occur (see Section 6.9).

Finally, it should be mentioned that logarithmic scales are usually used for i_C and v_{CE}, leading to an SOA boundary that consists of straight lines.

11.7.6 Parameter Values of Power Transistors

Owing to their large geometry and high operating currents, power transistors display typical parameter values that can be quite different from those of small-signal transistors. The important differences are as follows:

1. At high currents, the exponential i_C–v_{BE} relationship exhibits a factor of 2 reduction in the exponent; that is, $i_C = I_S e^{v_{BE}/2V_T}$.
2. β is low, typically 30 to 80, but can be as low as 5. Here, it is important to note that β has a positive temperature coefficient.
3. At high currents, r_π becomes very small (a few ohms) and r_x becomes important (r_x is defined and explained in Section 9.2.2).
4. f_T is low (a few megahertz), C_μ is large (hundreds of picofarads), and C_π is even larger. (These parameters are defined and explained in Section 9.2.2).
5. I_{CBO} is large (a few tens of microamps) and, as usual, doubles for every 10°C rise in temperature.
6. BV_{CEO} is typically 50 to 100 V but can be as high as 500 V.
7. I_{Cmax} is typically in the ampere range but can be as high as 100 A.

11.10.2 Characteristics of Power MOSFETs

In spite of their radically different structure, power MOSFETs exhibit characteristics that are quite similar to those of the small-signal MOSFETs studied in Chapter 5. Important differences exist, however, and these are discussed next.

Power MOSFETs have threshold voltages in the range of 2 V to 4 V. In saturation, the drain current is related to v_{GS} by the square-law characteristic of Eq. (11.80). However, as shown in Fig. 11.42, the i_D–v_{GS} characteristic becomes linear for larger values of v_{GS}. The linear portion of the characteristic occurs as a result of the high electric field along the short channel, causing the velocity of charge carriers to reach an upper limit, a phenomenon known as **velocity saturation**[5]. The linear i_D–v_{GS} relationship implies a constant g_m in the velocity-saturation region.

The i_D–v_{GS} characteristic shown in Fig. 11.42 includes a segment labeled "subthreshold." Though of little significance for power devices, the subthreshold region of operation is of interest in very-low-power applications (see Section 5.1.9).

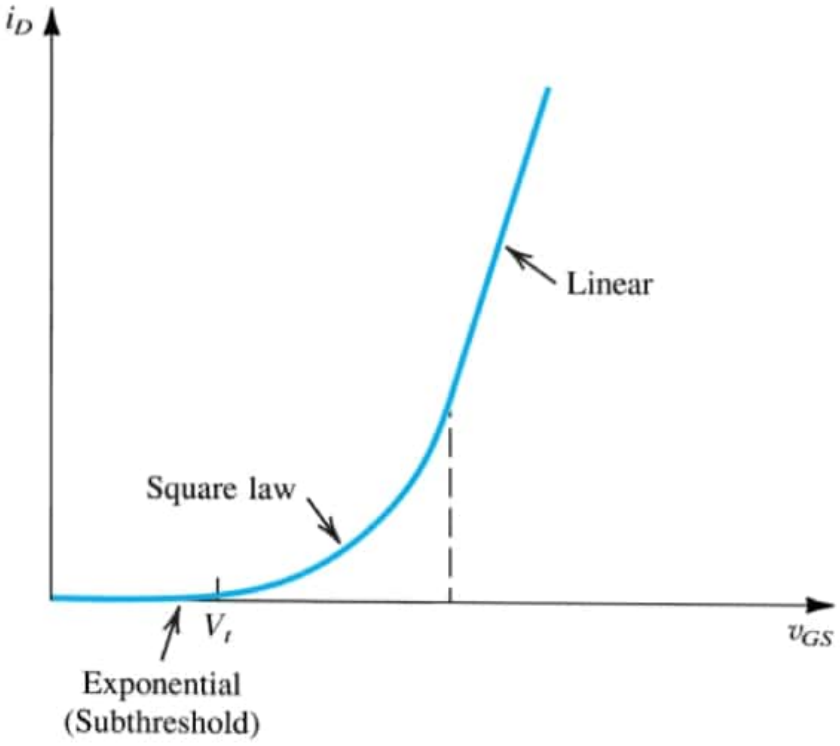

Figure 11.42 Typical i_D–v_{GS} characteristic for a power MOSFET.

11.10.3 Temperature Effects

Of considerable interest in the design of MOS power circuits is the variation of the MOSFET characteristics with temperature, illustrated in Fig. 11.43. Observe that there is a value of v_{GS} (in

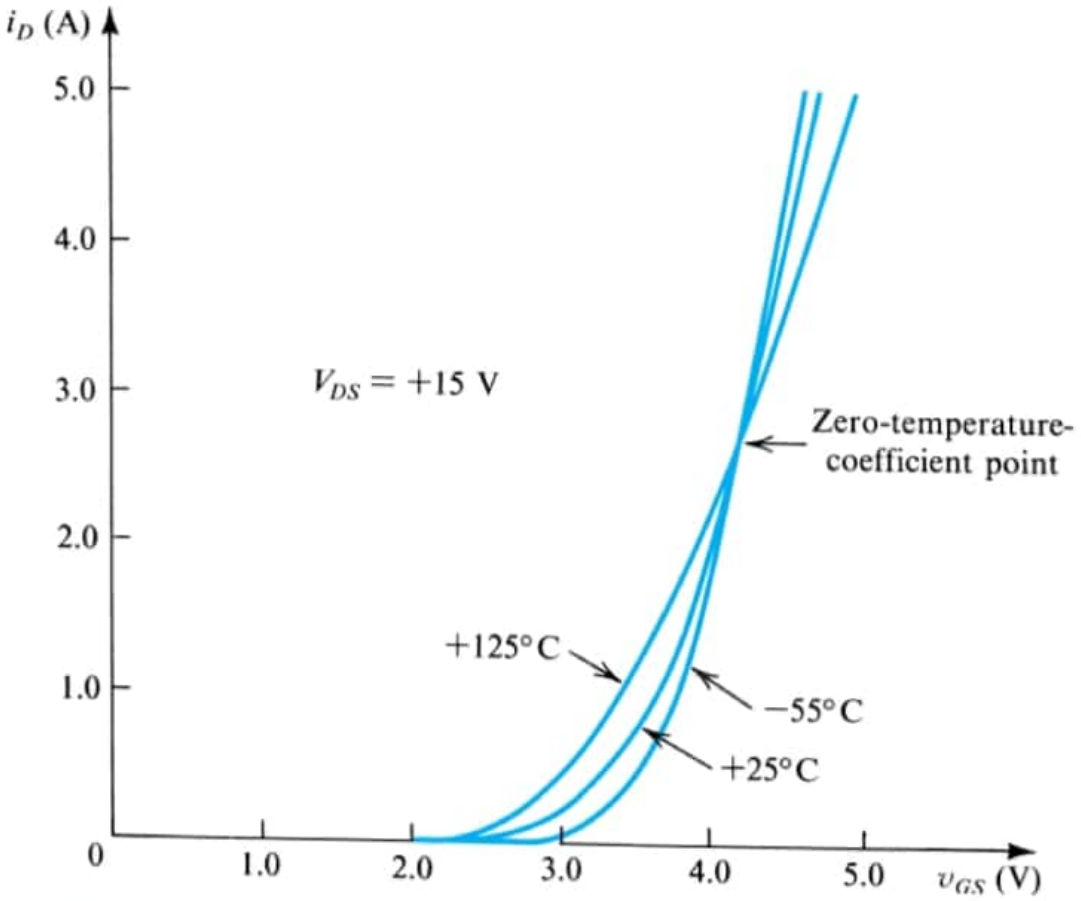

Figure 11.43 The i_D–v_{GS} characteristic curve of a power MOS transistor (IRF 630, Siliconix) at case temperatures of −55°C, +25°C, and +125°C. (Courtesy of Siliconix Inc.)

the range of 4 V to 6 V for most power MOSFETs) at which the temperature coefficient of i_D is zero. At higher values of v_{GS}, i_D exhibits a negative temperature coefficient. This is a significant property: It implies that a MOSFET operating beyond the zero-temperature-coefficient point does not suffer from the possibility of thermal runaway. This is *not* the case, however, at low currents (i.e., lower than the zero-temperature-coefficient point). In the (relatively) low-current region, the temperature coefficient of i_D is positive, and the power MOSFET can easily suffer thermal runaway (with unhappy consequences). Since class AB output stages are biased at low currents, means must be provided to guard against thermal runaway.

The reason for the positive temperature coefficient of i_D at low currents is that $v_{OV} = (v_{GS} - V_t)$ is relatively low, and the temperature dependence is dominated by the negative temperature coefficient of V_t (in the range of –3 mV/°C to –6 mV/°C) which causes v_{OV} to rise with temperature.

11.10.4 Comparison with BJTs

The power MOSFET does not suffer from second breakdown, which limits the safe operating area of BJTs. Also, power MOSFETs do not require the large dc base-drive currents of power BJTs. Note, however, that the driver stage in a MOS power amplifier should be capable of supplying sufficient current to charge and discharge the MOSFET's large and nonlinear input capacitance in the time allotted. Finally, the power MOSFET features, in general, a higher speed of operation than the power BJT. This makes MOS power transistors especially suited to switching applications—for instance, in motor-control circuits.