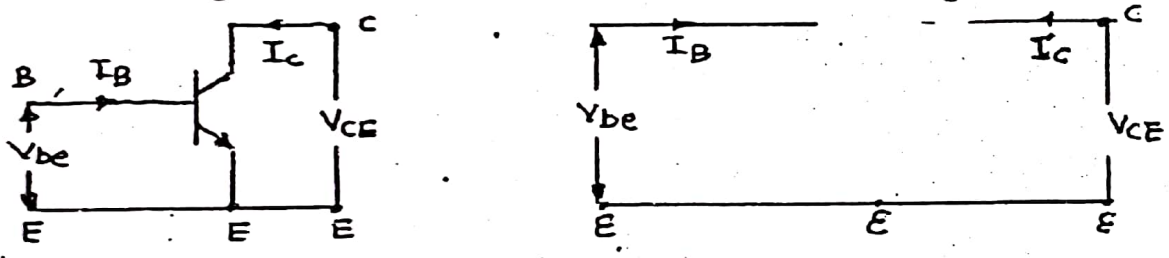
HF Model of BJT : Model is a two port network (TPN) consists of RLC voltage source & current source. Each and every component in BJT model represents physical phenomenon or characteristics of transistor.

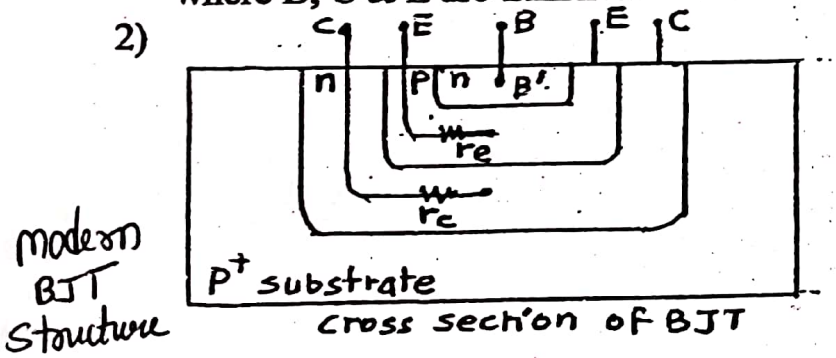
Step by step formation of model :

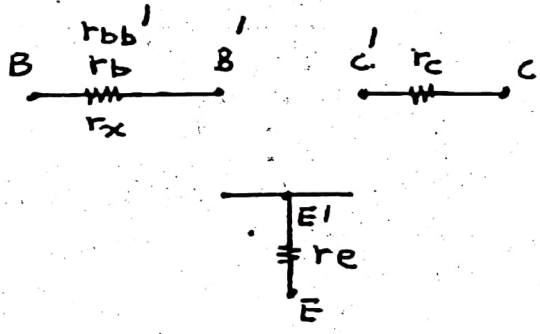
(1) Let us develop HF model of transistor connected in CE configuration



where B, C & E are transistor terminals.

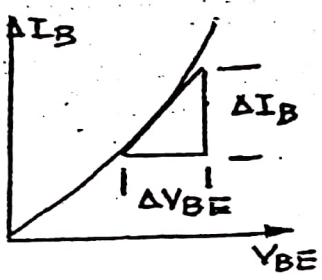
2)

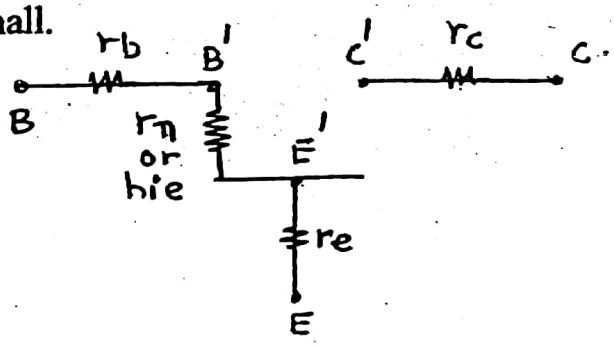




B', C', E' are idealized internal base collector and emitter, $r_b \rightarrow$ base spreading resistor i.e. a resistor between base terminal and internal base, similarly r_c & r_e can also be defined. These resistances are very small.

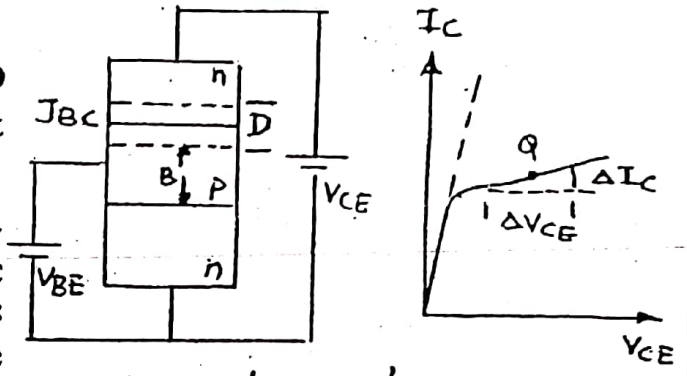
3)





Input characteristic of BJT indicates that as V_{BE} increase, I_B increases exponentially. Inverse of slope of characteristic at Q point represent input resistance of BJT. This point is represented in BJT by connecting a resistance between B' & E'. This is known as input resistance of BJT.

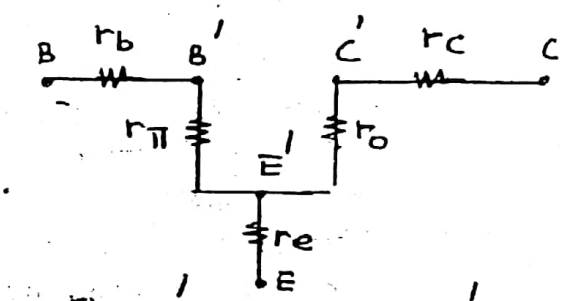
$$h_{ie} = r_\pi = \frac{1}{slope} = \left.\frac{\Delta V_{BE}}{\Delta I_B}\right|_{\Delta V_{CE}=0} \qquad r_\pi \rightarrow 1 \text{ to } 3k\Omega$$



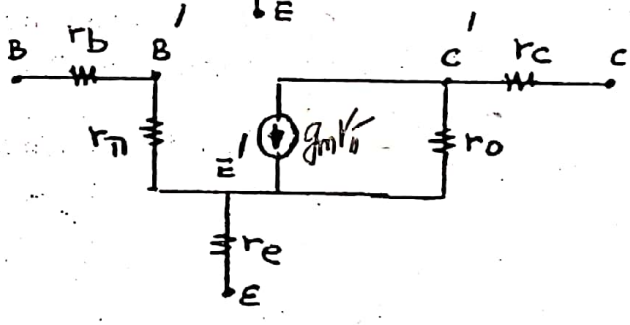
4) As V_{CE} increases, width of depletion region D increases, width of base B decreases, electrons & hole recombination in base region decreases. ∴ number of electron drifting to collector increases. This increases I_C. It means as V_{CE} increases, I_C increases. This is due to early effect & provides slope of charac. This phenomenon is shown in the model by connecting a resistance r_o between C' & E' where.

$$r_o = \left.\frac{1}{slope}\right|_{Qpt} = \left.\frac{\Delta V_{CE}}{\Delta I_C}\right|_{\Delta IB=0}$$

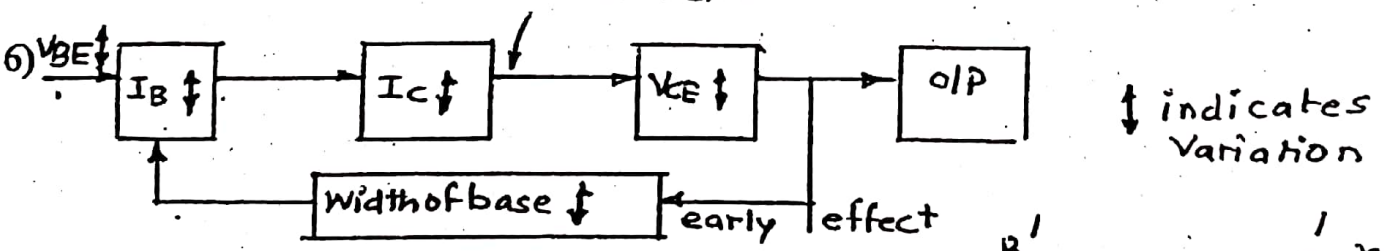
$r_o \rightarrow 40$ to $80k\Omega$



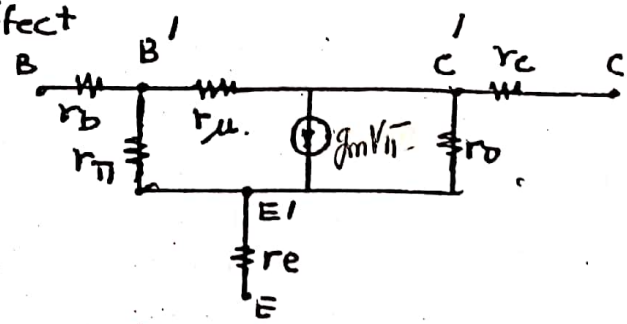
5) BJT is a current control device. Output current I_C is controlled by input current I_B. $I_C = g_m V_\pi$
i.e. $I_C = h_{fe} I_B = \beta I_B$. This characteristic of transistor is shown in model by a dependent current source.
β or $h_{fe} \rightarrow 20$ to 300.



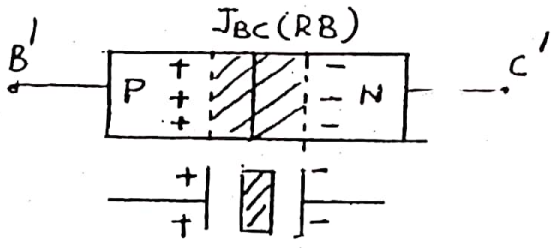
6)

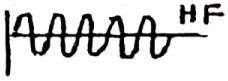


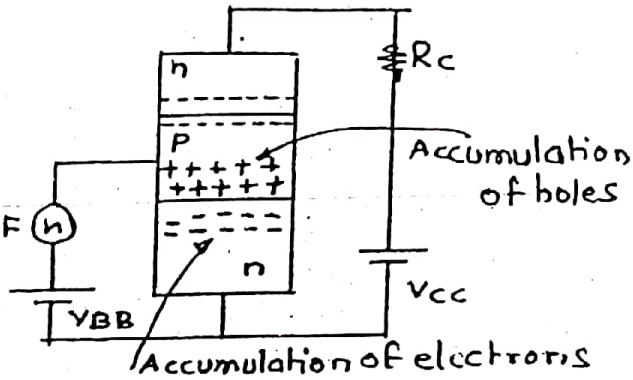
As V_{BE} varies, I_B varies since $I_C = \beta I_B$, I_C varies this changes V_{CE}. Variation in V_{CE} changes reverse bias potential across J_{BC}. This causes variation in base width, which finally changes I_B. It means change in output i.e. V_{CE} causes change in input (I_B). This indicates feedback between output to input. This internal feedback of BJT is represented in model by connecting a resistance r_μ between input & output [C' & B'] $\qquad r_\mu \rightarrow 4$ to $8M\Omega$



7) Junction J_{BE} is reverse bias. This causes an appreciable depletion region to exists across junction. Depletion region doesn't have any free electron in it. ∴ this behaves like insulator and works as dielectric, while P region and N region works as plate with +ve and –ve charges. This forms a capacitance between C' & B'. This is known as transition capacitance (C_T or C_μ).

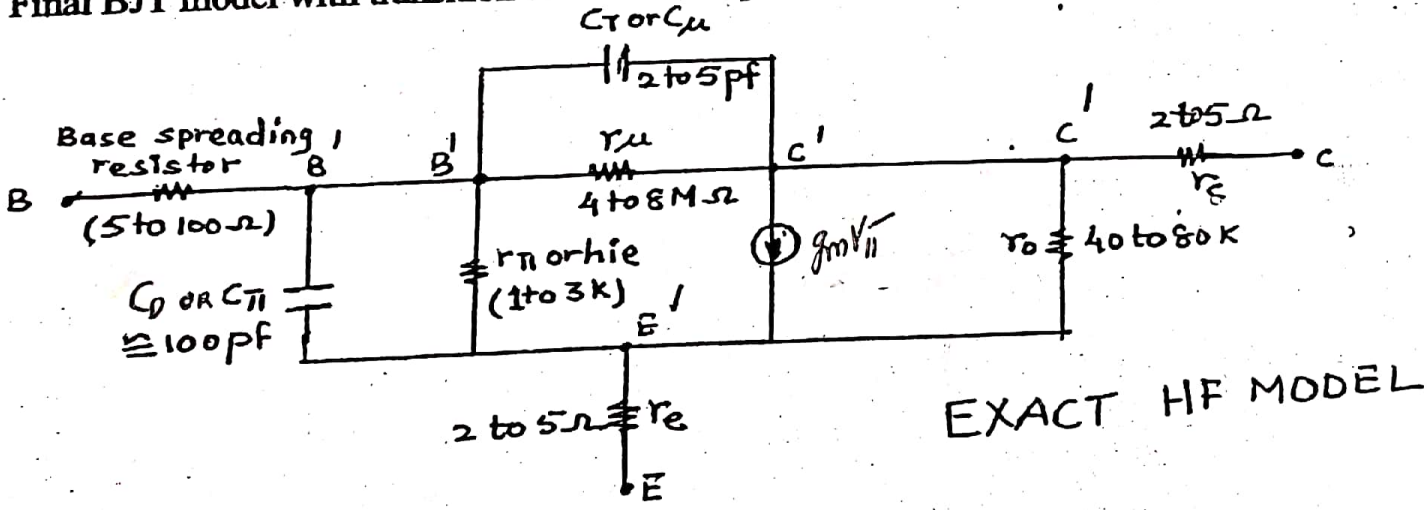


8) At LF  time per cycle is more. Therefore time available for electron to diffuse through J_{BE}, move through base region and drift to collector is large. But at high frequency time per cycle is less. 



∴ electron coming from E did not get enough time to diffuse through J_{BE}. Similarly holes coming from collector did not get enough time to diffuse through forward biased J_{BE}. This causes accumulation of electrons on E side of J_{BE}, while holes gets accumulated on B side of J_{BE}. This phenomenon of charge storage around forward biased J_{BE} is represented in model by a capacitor between B' & E' known as diffusion capacitance C_π or C_D.

Final BJT model with transition & diffusion capacitance is shown below.



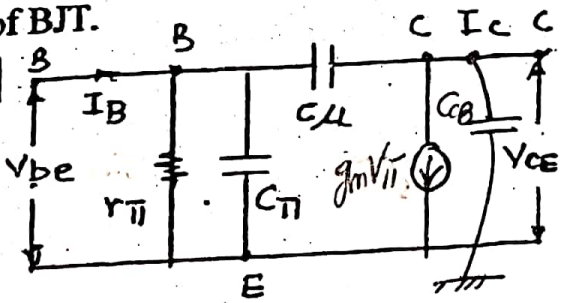
EXACT HF MODEL

* C_π & C_μ → are known as internal stray capacitance of BJT.

* HF model of BJT = MF model + Internal capacitances.

* **Approximate HF model** : In the exact model above r_b, r_e, r_c can be taken as short because they are very small. r_μ, r_o can be taken as open due to high value. Now

$B' = B, C' = C, E' = E$



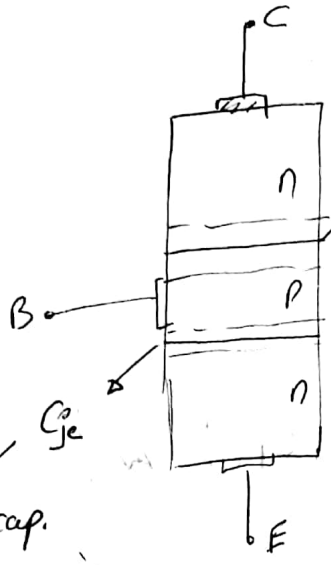
• Ignore r_b, r_e, r_μ, r_c completely for HF analysis

C_{CB} – Collector-bulk capacitance

↓ This cap. appears only in BJT that are integrated in a wafer.

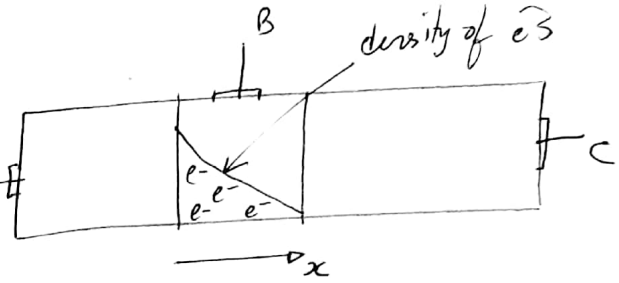
• High-freq model of Bipolar transistor :-

p-n J^n ⇒ Depl rg^n ⇒ cap
↳ J^n cap.

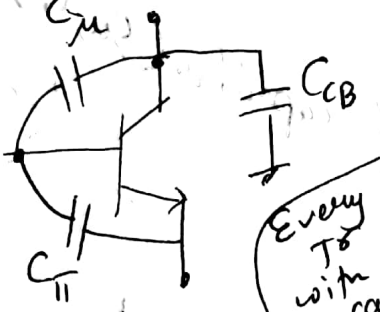


Junction cap. due to dep. region of B-E J^n.

BJT in f/w-active region



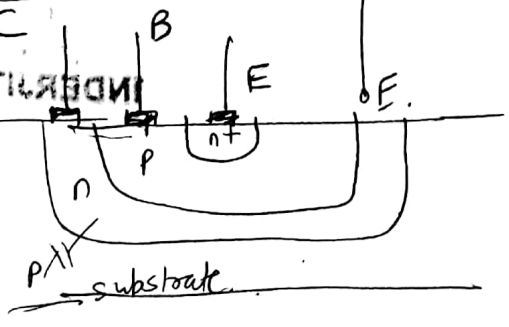
- Movement of e$^-$s inside the base area is by diffusion.
  - need a gradient of conc^n of e$^-$s
- To turn on the Bipolar device
  - we have stored some e$^-$s in base region



Every bipolar To comes with 3 capacitors

$C_{jc} \approx C_\mu$ ↳ This can be modelled by a capacitance.

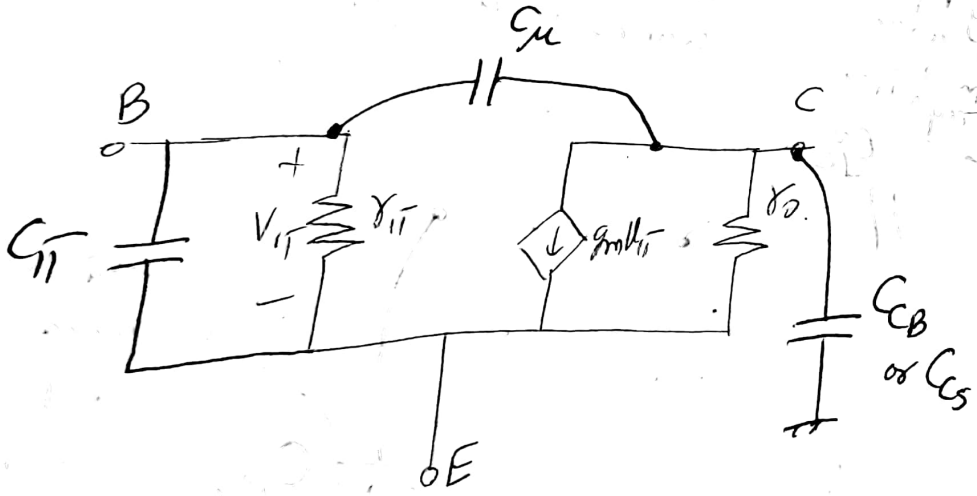
Structure of BJT built in IC form



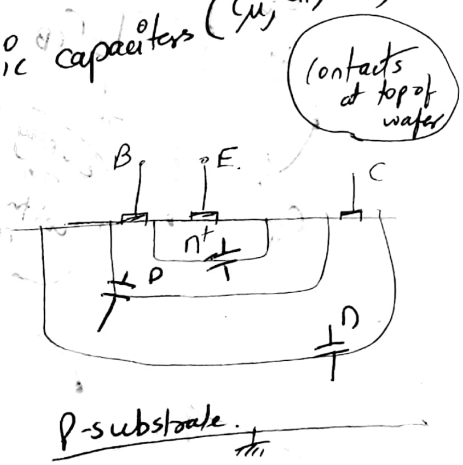
C to substrate R.B J^n of np.
↳ R.B

INDERJIT SINGH

② Bipolar Transistor Caps
(HF model)



intrinsic capacitors (C_μ, C_π, C_{CD})

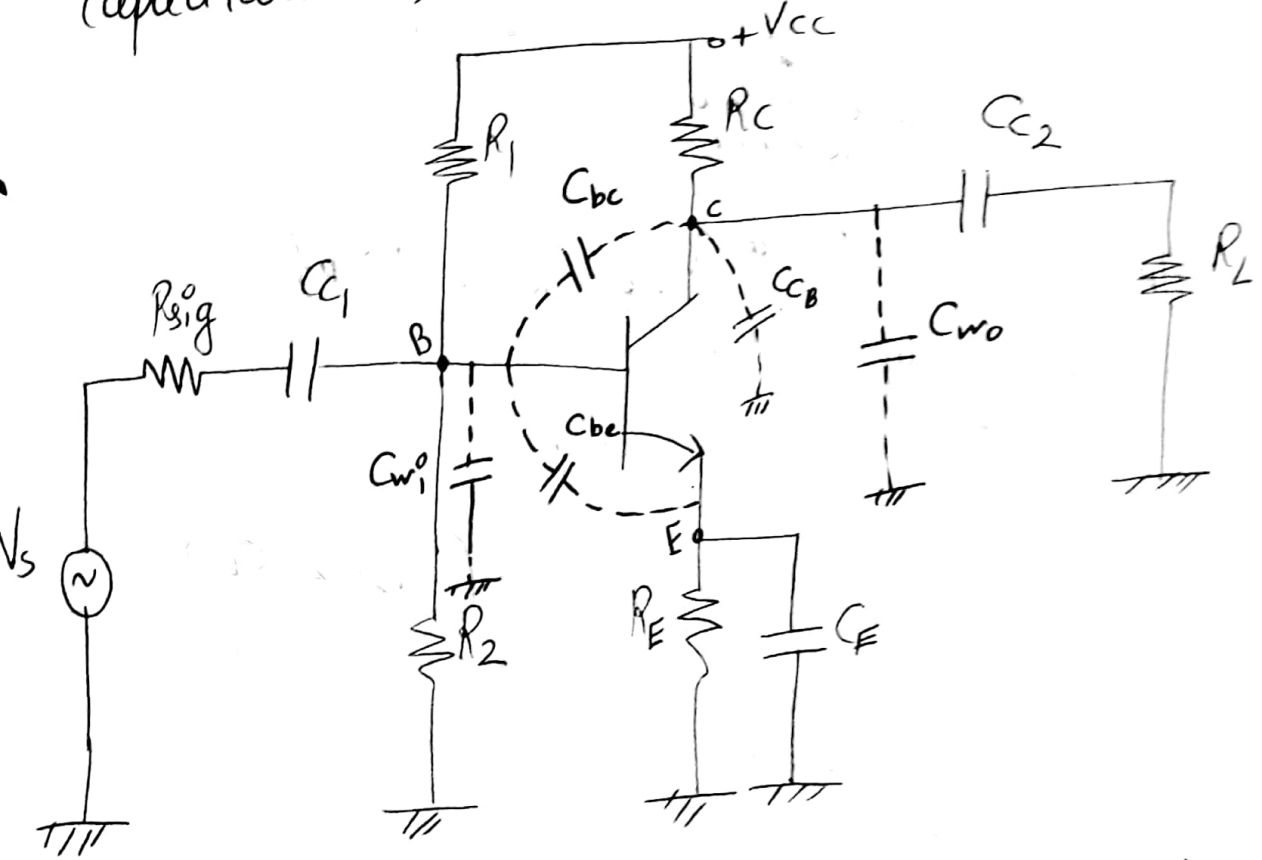


general structure of bjt in integrated circuits.
(not discrete)
modern bjt

INDERJIT SINGH

High-Frequency response of BJT amplifier:-

The gain of a bipolar amplifier falls at higher frequencies due to inter-electrode (parasitic) capacitance of transistor and wiring capacitances. as shown below:-



C_{bc} or C_μ } → Parasitic capacitance or stray capacitances

C_{be} or C_π

C_{wi}, C_{wo} } → wiring capacitances. (introduced due to wires)

C_{wi} → I/p wiring capacitance

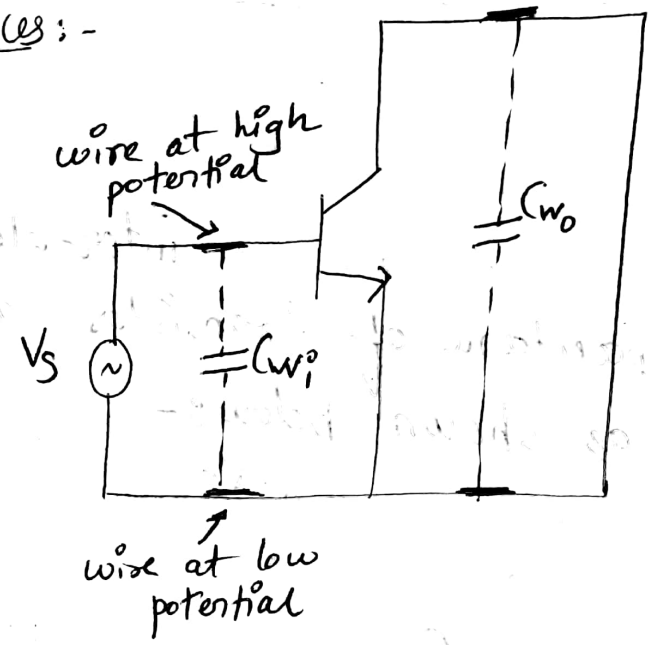
C_{wo} → o/p wiring capacitance.

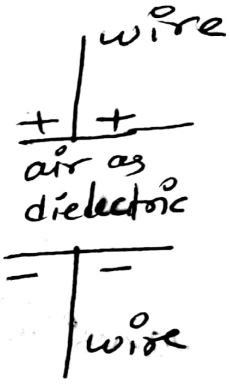
$C_\mu, C_\pi, C_{wi}, C_{wo}$ ~ pf

C_{C_1}, C_{C_2}, C_E → Externally connected capacitors ~ μF

Wiring Capacitances:-

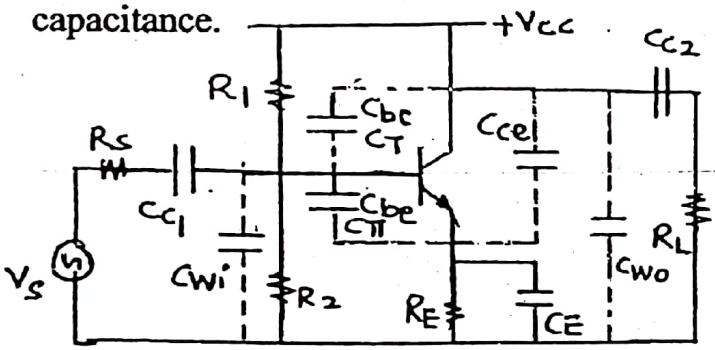
- Wires at I/P & O/P of amplifiers are at different potentials
- Therefore, there exists a capacitance between wires





C_{wi} → i/p wiring capacitance
C_{wo} → o/p wiring capacitance
} → 2 to 10 pf

* Circuit diagram of BJT amplifier with all stray capacitance.



C_{C1}, C_{C2}, C_E → connected capacitors
C_T, C_π, C_{ce}, C_{wi}, C_{wo} → stray, parasitic, fictitious capacitor.
connected caps → in μf.
stray caps → in pf.

STATUS OF CAPACITORS IN DIFFERENT FREQUENCY RANGE

* **DC** → (f = 0) → $X_C = \frac{1}{2\pi f C} = \infty$ → all connected and stray caps are open.

* **LF** → very low frequency (few hertz) → $X_C = \frac{1}{2\pi (Hertz)(\mu f)}$ neither very low nor very high ∴ connected capacitor are considered

→ $X_C = \frac{1}{2\pi (Hertz)(pf)}$ = very high ∴ at LF stray capacitors are open.

* MF → Mid frequency (few 100's of KHz)

→ $X_C = \frac{1}{2\pi (100\times10^3\, Hz)(\mu f)}$ = very low

stray/parasitic capacitors

∴ connected capacitors are short, $X_C = \frac{1}{2\pi (100\times10^3)(pf)}$ = high

∴ stray capacitors are open.

* HF → high frequency (100's of MHz) → $X_C = \frac{1}{2\pi (MHz)(\mu f)}$ = very low

∴ connected capacitors are shorted, $X_C = \frac{1}{2\pi (MHz)(pf)}$ = high

∴ stray caps are neither short nor open but considered.