# * MOSFET I-V Characteristics and device parameters estimation

Principle: A voltage at its gate terminal controls current between its source and drain.

Note: i) Body terminal of an NMOS is connected to gnd
ii) Body terminal of an PMOS is connected to highest voltage in the circuit ie $V_{DD}$.

This is done to minimize any drift in threshold voltage $V_T$.

· Long-channel approximation: - (Nmos)

$$I_D = \frac{K_n}{2}\left[2(V_{GS}-V_T)V_{DS} - V_{DS}^2\right] \quad \text{-- } V_{GS}-V_T > V_{DS}$$

(Linear region)

$$I_D = \frac{K_n}{2}\left[V_{GS}-V_T\right]^2 \quad \text{-- } V_{GS}-V_T < V_{DS}$$

(Saturation region)

$V_{Tn}$ of Nmos is positive

$V_{Tp}$ of Pmos is negative.

· $K_n = \mu_n C_{ox}\left(\frac{W}{L}\right)$

## Problem Statement:

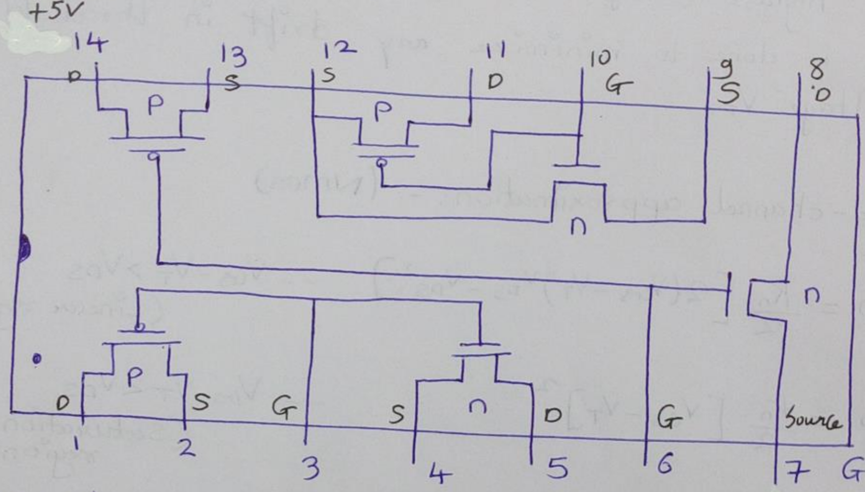
In this experiment, we will do the following for an NMOS transistor: -

* Measure threshold voltage $V_{TN}$
* Measure o/p DC characteristics : $I_D$ Vs $V_{DS}$
* Measure $I_D$ Vs $V_{GS}$ characteristics in saturation region

* Measure small signal transconductance (gm)

Components required : CD4007 MOSFET IC, 5.6V Zener, Resistor → 680Ω, 100Ω, 5K pot, 1KΩ
Capacitor → 10μF, multimeter, Function generator, CRO.

CD 4007: (PIN OUT)



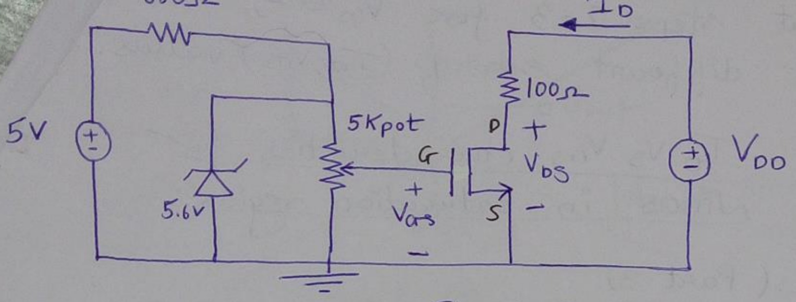

7 → gnd
14 → +5V

(body terminal of all Nmos T^r are tied together)

# Analysis (PART 1): $V_T$ of NMOS

⇒ Threshold voltage ($V_T$) can be found by biasing NMOS in Linear region and varying $V_{gs}$ in small steps and noting Linear change in $I_D$
(Refer circuit ⓐ)

Zener-diode is used to prevent gate voltage from going above 5.6V ⇒ which may cause device oxide to break down.




Circuit ⓐ

Procedure (Part A):

1) Wire up the above circuit ⓐ. Adjust $V_{DD}$ such that $V_{DS} \approx$ 200mV. (Keep monitoring $V_{DS}$ throughout this part — it should be kept constant at 200mV)

2) Vary $V_{GS}$ by means of 5K pot and note $I_D$. Take ($I_D$, $V_{GS}$) readings till $V_{GS} = 5V$

Note: Do not dismantle the ckt ⓐ, you will be using it for part B as well.

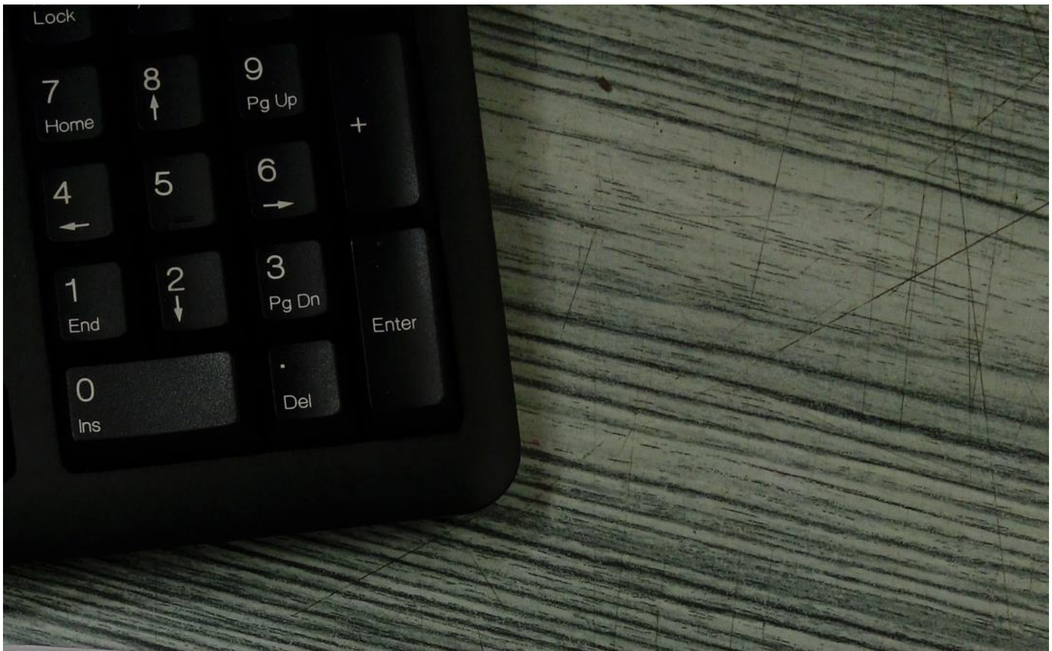
PART 2: $I_D - V_{DS}$ characteristics $|_{\text{at } V_{GS} \text{ constant}}$

Procedure: (Part B)

1) Wire up the circuit ⓐ.

2) Adjust $V_{GS} = 1.5$ V and monitor it to ensure that it stay's constant.

3) Vary $V_{DS}$ in small steps from 0 to 5V and note $I_D$.



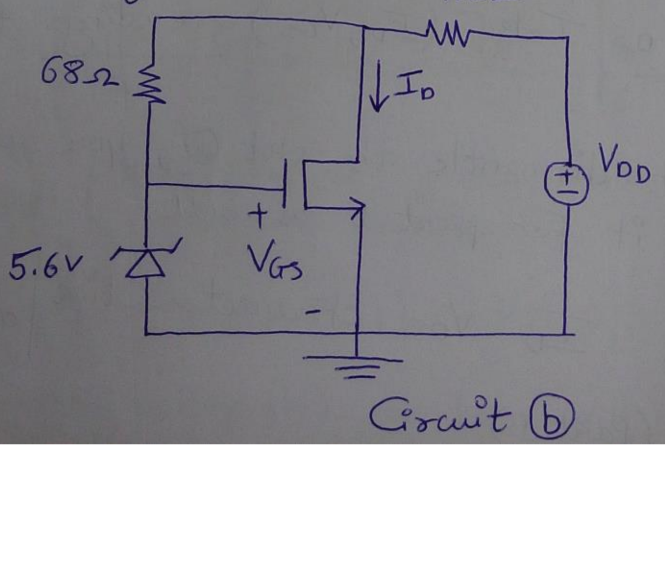
4) Repeat steps 2-3 for $V_{GS} = 2, 2.5$ and 3 V to get different sets of ($I_D$, $V_{DS}$) values.

PART3: $I_D$ Vs $V_{GS}$ characteristics for NMOS in saturation region

Procedure:( Part 3)

1) Wire up circuit (b). The circuit is designed to make $V_{GS} < V_{DS}$. This ensures that $V_{DS} > V_{GS} - V_{TN}$ ie transistor always remain in saturation.

2) Now vary $V_{GS}$ by varying $V_{DD}$ in small steps from 0 to 5V. Note down the value of $I_D$.



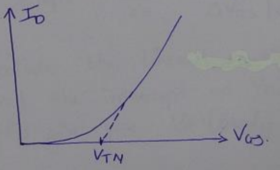

Circuit (b)

## * Obtaining results and Interpreting them:-

PART A :

From $I_D - V_{GS}$ data in part A : -

1) Plot graph of $I_D$ Vs $V_{GS}$ on Linear scale.
2) Extrapolate Linear portion of plot as shown below to find the intercept on $V_{GS}$ axis. This will give $V_{TN}$.

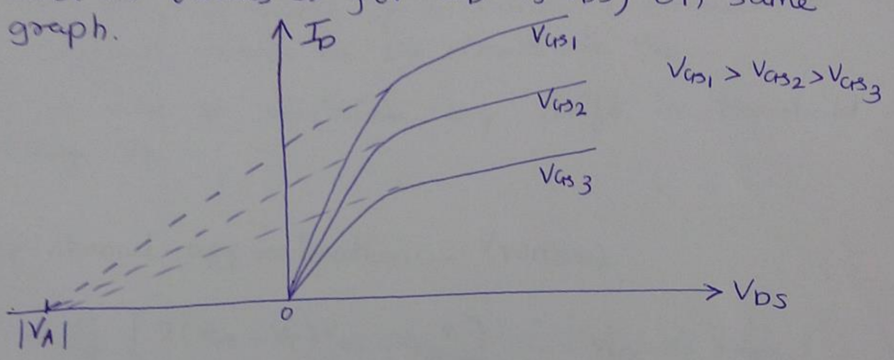



3) Also compute $g_m = \frac{\partial I_D}{\partial V_{GS}}$ . At what value of $V_{GS}$ is $g_m$ maximum?
4) Calculate Linear region resistance $r_o$ and plot it as a function of $V_{GS} - V_{TN}$.

PART B:

From $I_D$-$V_{DS}$ data in Part B:

1) Plot a graph of $I_D$ Vs $V_{DS}$ on a Linear scale. Plot all of these $V_{GS}$ ⇒ different constant values ⇒ for $I_D$ Vs $V_{DS}$) on same graph.




2) From the slope of Linear portion of graph, Find O/P drain-source resistance $r_o$ at $V_{DS} = 5V$ for different value of $V_{GS}$ as,

$$slope = \frac{1}{r_o} = \left.\frac{\Delta I_D}{\Delta V_{DS}}\right|_{V_{GS}}$$

3) Extrapolate the Linear portion of graph to find the intercept on $V_{DS}$ axis. This will give you $V_A$ (Early voltage).

Part C: From $I_D$-$V_{GS}$ characteristics in saturation

1) Plot a graph of $I_D$ Vs $V_{GS}$ on a Linear scale.