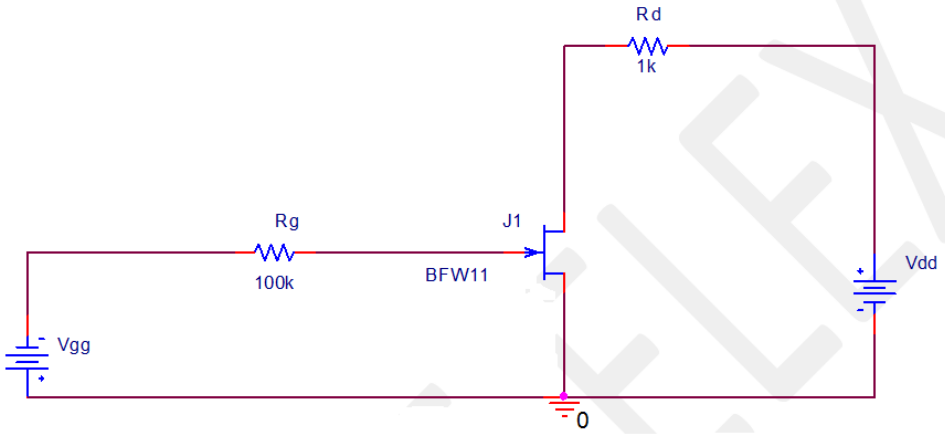
FET CHARACTERISTICS

AIM : - To study the FET characteristics .

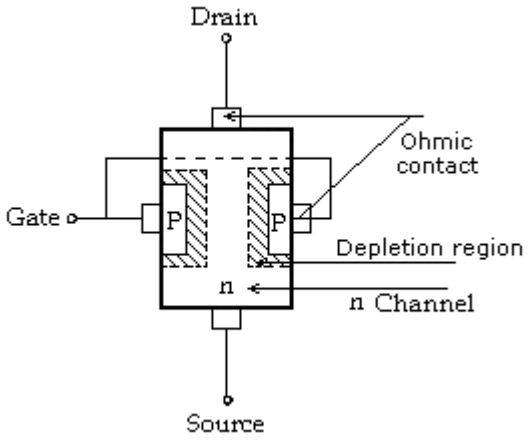
APPARATUS :- FET – BFW 10/11, resistors, 2 – power supply , multimeter.

CIRCUIT DIAGARM :-



THEORY :-

Construction & Char. of JFET:-

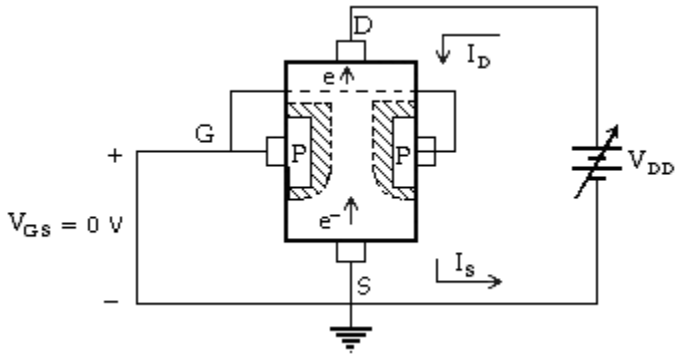


The basic construction of n –channel FET is as shown in figure. The major part of JEET is the channel between embedded P type of material.

The top of the n- channel is connected to an ohmic contact called as ‘Drain’ (D) & Lower end of Channel is called as ‘Source’ (S). The two p types of materials are connected together & to the ‘Gate ‘terminal (G).

Characteristic:-

1. **V_{GS} = 0$_V$, V_{DS} - Some +ve Value:-**



As shown in the figure the gate is directly connected to source to achieve $^{V}_{GS}$ = 0v , this is similar to no bias condition. The instant the voltage V_{DD}(=V_{DS}) is applied , the e^- will drawn to the drain terminal, causing I_D & I_S to flow (i-e. I_D = I_S). Under this condition the flow of charge is limited solely by Resistance of the n channel between drain & source.

It is important to note that the depletion region wider at the top of both p type of material. Since the upper terminal is more R .B. than the lower terminal (source - S).

As voltage V_{DS} is increased from 0 to few volts, the current will increase as determined by ohm's law. if still V_{DS} is increased & approaches a level referred as Vp, the depletion region will widen, causing a noticeable reduction in channel width. The reduced path of conduction causes the resistance to increase. The more the horizontal curve, the higher resistance.

If V_{DS} is increase to a level where it appears that the two depletion region would touch each other, the condition referred as 'pinch –off ' will result . The level of V_{DS} that establish this condition is called as 'pinch off voltage' (V_P). At V_P, I_D should be zero, but practically a small channel still exists & very high density current still flows through the channel.

As V_{DS} is increased beyond V_P the saturation current will flow through the channel (I_{DSS}).

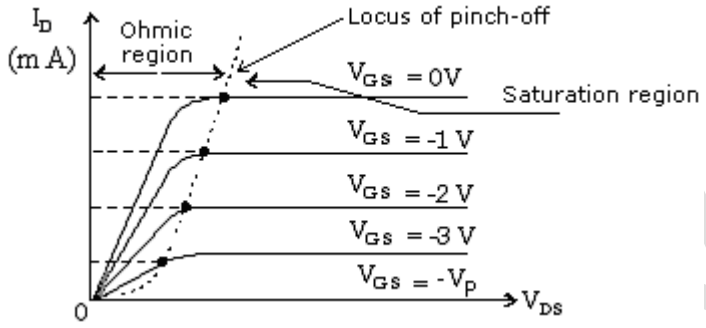
I_{DSS} – Drain to source current with short cut connection from source to Gate.

2. **V_{GS} < 0V:-**

If a –ve bias is applied between gate and source, the effect of the applied –ve bias V_{GS} is to establish depletion region similar to those obtained with V_{GS} = 0V but at lower level of V_{DS}.

As V_{GS} will become more & more –ve biased , the depletion layer pinch off occur at the less & less value of V_{DS} . Eventually, when V_{GS} = - V_P , will be sufficiently –ve to establish a

saturation level , i.e. essentially 0 mA & for all practical purpose the device has been 'turned OFF.'



The region to the right of the pinch – off locus is typically employed in linear amplifiers (Amplifier with min. distortion at applied signal) is commonly referred as the constant current, saturation or linear amplification region.

Voltage controlled region. :-

The region left of pinch – off locus is called as ohmic or voltage controlled region.

In this region the JEET can actually be employed as a variable register whose resistance is controlled by V_{GS}. As V_{GS} becomes more & more –ve, the slope of the curve becomes more & more horizontal, corresponding with an increasing resistance level.

$$rd = \frac{ro}{\left(1 - \frac{V_{GS}}{V_P}\right)^2}$$

Where,

ro – the resistance with V_{GS} = 0V

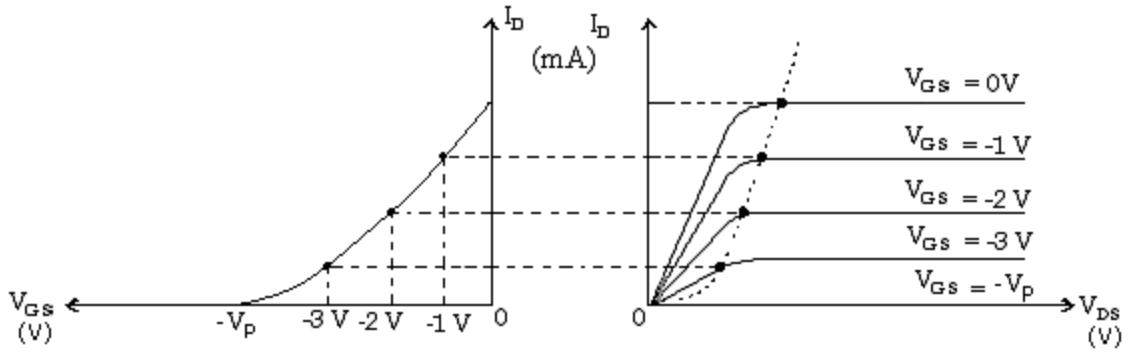
rd – the resistance at particular value of V_{GS}.

Transfer characteristic:-

The relation between I_D & $V_{GS,}$ is given by Shockley's equation.

$$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2$$

The squared term of equation will result in a non – linear relationship between I_D & V_{GS}.



PROCEDURE:-

1. Assemble the circuit as per given diagram properly.
2. Adjust both supply to 0V i.e V_{GS} = 0V & V_{DS} = 0V
3. Note down drain current I_D in mA.
4. By keeping V_{GS} constant to 0V , increase drain to sourse voltage V_{DS} in step of 1V upto 10 volts and measure the current I_D .
5. Now change V_{GS} from 0V to 0.5 ,1V,1.5V,2V,2.5,3 V etc. and repeat the above step no.4 .(VGS voltage should be constant)
6. Now keep the voltage V_{DS} constant at 10 v. Change the V_{GS} in the step of 0.5 upto 4V . Measure current I_D . Tabulate all readings.
7. Plot the characteristics i.e V_{DS} vs I_D and V_{GS} vs I_D .
8. Calculate I_{DSS} ,$V_{P,}$ g_{mo} , r_{ds} from the graphs and verify it from the data sheet.

OBSERVATION TABLE :- Table 1

V_{GS} = 0V		**V_{GS} = 0.5V**		**V_{GS} = 1V**		**V_{GS} = 1.5V …….upto 3V**	
V_{DS} (V)	I_D (mA)	V_{DS} (V)	I_D (mA)	V_{DS} (V)	I_D (mA)	V_{DS} (V)	I_D (mA)
0							
1							
2							
Upto 10							

Table 2 **V_{DS} = 10V**

V_{GS}(V)	**I_D (mA)**
-0.5 V	
-1V	
1.5V upto 5V	

CONCLUSION :-