① Device Characteristics:- (JFET)

18/9/14

- Consider a symmetrical uniformly doped two-sided depletion mode pn JFET.

→ Aim: Derive I-V characteristics for I_{D1}

Total drain current (in a two-sided device) is $I_{D2} = 2I_{D1}$.

- Consider n-channel JFET:

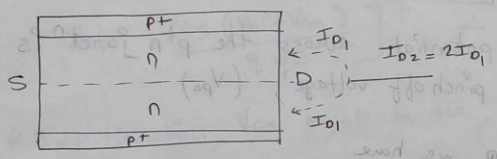
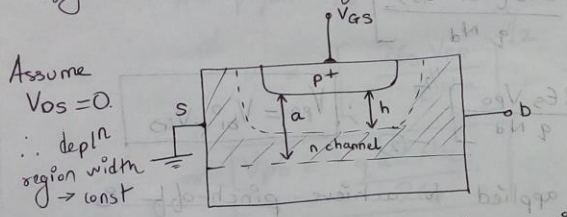


fig. Drain currents of a symmetrical 2-sided nchannel JFET.



Assume $V_{DS} = 0$.
∴ depln region width → const

Case I:
$V_{DS} > 0$

- h – induced depletion region width for one-sided p^+n junction
- a – Metallurgical channel thickness betⁿ p^+ gate region & the substrate.

Extra: Depletion region width for a p-n junction is,

$$W = \sqrt{\frac{2\epsilon_s (V_{bi} + V_R)}{q} \left[\frac{N_a + N_d}{N_a N_d}\right]}$$

For a p^+n device ⇒ $N_a >> N_d$

$N_a + N_d \approx N_a$

$$W = \sqrt{\frac{2\epsilon_s (V_{bi} + V_R)}{q N_d}}$$ --- for p^+n diode.

(2)

If we assume the abrupt depletion approximation, then the space-charge width is,

$$h = \left[\frac{2\varepsilon_s (V_{bi}^\circ - V_{GS})}{q N_d} \right]^{1/2} \quad \text{— (1)}$$

For a rev. bias p+n junction, V_{GS} must be '-ve'.

• At pinch-off, $\boxed{h = a}$

Thus, the total potential across the p+n junct^n is called the 'internal pinch off voltage', (V_{po})

From, a we have

$$a = \left[\frac{2\varepsilon_s (V_{bi}^\circ - V_{GS})}{q N_d} \right]^{1/2}$$

$$a = \left[\frac{2\varepsilon_s V_{po}}{q N_d} \right]^{1/2} \quad \text{— (2)} \qquad ; \boxed{V_{po} = V_{bi}^\circ - V_{GS}}$$

$$V_{po} = \frac{q a^2 N_d}{2\varepsilon_s}$$

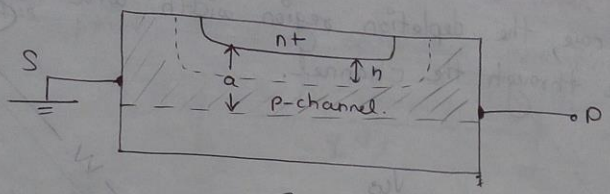
→ V_{GS} that must be applied to achieve ~~pinch-off~~ is described as "pinch-off voltage" / "turn-off vtg" / "threshold vtg". (V_P)

From ① & ②, $V_{bi}^\circ - V_P = V_{po} \Rightarrow \boxed{V_P = V_{bi}^\circ - V_{po}}$ ↳ (a)

The gate to source voltage to achieve ~~pinch-off~~ in an n-channel JFET is '-ve' ∴ thus $V_{po} > V_{bi}^\circ$

* The pinch-off voltage is the gate to source voltage that must be applied to turn the "JFET off".

Similarly, for a p-channel JFET ③



- Induced depletⁿ region for one-sided n^+p junction is

$$h = \left[\frac{2\epsilon_s (V_{bi} + V_{GS})}{q N_a}\right]^{1/2} \quad - ③$$

- For a R.B n^+p junction, V_{GS} must be +ve,

At pinch-off $\boxed{h = a}$,

$$a = \left[\frac{2\epsilon_s V_{po}}{q N_a}\right]^{1/2}$$

or $\boxed{V_{po} = \frac{q a^2 N_a}{2\epsilon_s}}$ ④

From ③ and ④, we get

- Pinch-off voltage is defined as gate to source voltage to achieve the pinch-off condition, so at pinch-off

$$V_{bi} + V_p = V_{po} \quad \text{or} \quad \boxed{V_p = V_{po} - V_{bi}}$$

⇒ Thus, we have determined the pinch-off voltage for both n-channel and p-channel JFETs when the $V_{DS} \approx 0$

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Case ②: Both V_{GS} and V_{DS} applied.

→ In this case, the depletion region width will vary with the distance through the channel.

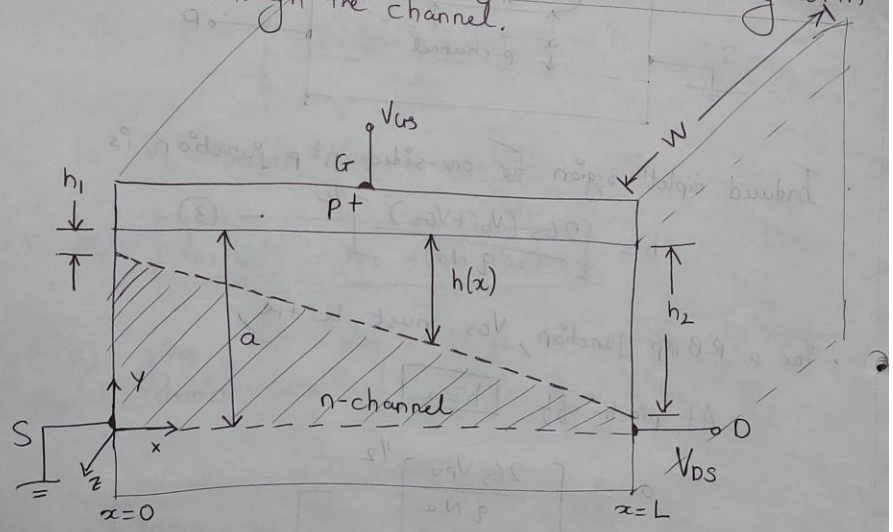

fig: Simplified geometry of an n-channel pn junction FET.

- Depletion width at source end $= h_1$ → is a function of V_{bi} and V_{GS}.

- Depletion width at drain end $= h_2$ → is a function of V_{DS}, V_{GS} and V_{bi}.

$$h_2 = \left[\frac{2 \epsilon_s (V_{bi} + V_{DS} - V_{GS})}{q N_d} \right]^{1/2} \quad — (5)$$

$+V_{GS}$ → ∵ V_{DS}, '+ve' applied ; $-V_{GS}$ → ∵ V_{GS}; '-ve' applied.

Pinchoff at the drain terminal occurs when $\boxed{h_2 = a}$ (5)

→ At this point, we reach saturation condition, ie $V_{DS} = V_{DS(sat)}$

$$\Rightarrow \quad a = \left[\frac{2\varepsilon_s (V_{bi} + V_{DS(sat)} - V_{GS})}{q N_d} \right]^{1/2} \quad - (6)$$

ie $$V_{bi} + V_{DS(sat)} - V_{GS} = \frac{q a^2 N_d}{2\varepsilon_s} = V_{po}$$

ie $$\boxed{V_{DS(sat)} = V_{po} - (V_{bi} - V_{GS})} \quad - (7)$$

Eq^n (7) gives the V_{DS} voltage to cause pinchoff at the drain terminal. (V_{DS} ↓ses with ↑sing Rev bias V_{gs})

ie $$V_{D(sat)} = V_{GS} - (V_{bi} - V_{po})$$

$$\boxed{V_{D(sat)} = V_{GS} - V_p} \quad - (8) \quad \text{from (a)}$$

Similarly, in a p-channel JFET, at saturation,

$$\boxed{V_{SD(sat)} = V_{po} - (V_{bi} + V_{GS})}$$

where, now Source is +ve w.r.t the drain.

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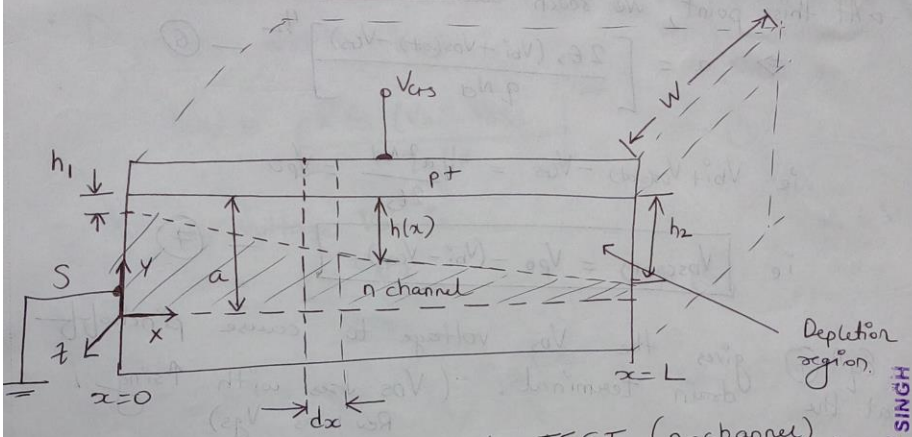
— x —

* "Ideal dc I-V Relationship":

Depletion mode n-channel JFET



fig(1a): Structure of JFET (n-channel).

- Consider a differential incremental strip of length 'dx' across the channel.
  (We are moving this strip from S to D, such that it covers the total current).

- Differential volume in the channel = $W[a - h(x)]dx$ — (1)
  (width × height × length)

- Resistance of the differential volume = $\frac{\rho \cdot d}{A} \simeq \frac{\rho\, dx}{W[a-h(x)]}$ — (2)

- Conductivity (σ) = $\frac{W[a-h(x)]}{\rho\, dx}$

$\sigma = \frac{1}{R}$ → resistance.

- $I_D = \frac{W[a - h(x)]}{\rho\, dx}\, dV_x$ — (3)

(Considering differential voltage change as dV_x).

- Depletion width $h(x)$ is

$$h(x) = \left[\frac{2\varepsilon_s (V_{bi}^\circ - V_{Gx})}{q N_d}\right]^{1/2} \quad — (4)$$

V_{Gx} → gate to 'x' distance voltage.

- Pinch-off voltage V_p is

$$V_p = \frac{q a^2 N_d}{2\varepsilon_s} \quad — (5)$$

ie $$h(x) = a\left(\frac{V_{bi}^\circ - V_{Gx}}{V_p}\right)^{1/2} \quad \text{(From (4) \& (5))},$$

$$\therefore a - h(x) = a\left[1 - \left(\frac{V_{bi}^\circ - V_{Gx}}{V_p}\right)^{1/2}\right]$$

$$a - h(x) = a\left[1 - \left(\frac{V_{bi}^\circ - V_G + V_x}{V_p}\right)^{1/2}\right] \quad — (6)$$

From (3) and (6), we get

$$I_D\, dx = \frac{Wa}{\rho}\left[1 - \left(\frac{V_{bi}^\circ - V_G + V_x}{V_p}\right)^{1/2}\right] dV_x.$$

Total drain current I_D from $x = 0$ to $x = L$
$\equiv$ (V_x will change from 0 to V_D)

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ie $$\int_0^L I_D\,dx = \frac{Wa}{\rho}\int_0^{V_D}\left[1-\left(\frac{V_{bi}^{\circ}+V_x-V_G}{V_p}\right)^{1/2}\right]dV_x \quad (8)$$

ie $$I_D \cdot L = \frac{Wa}{\rho}\left[V_x - \frac{2}{3V_p^{1/2}}\left(V_{bi}^{\circ}+V_x-V_G\right)^{3/2}\right]_0^{V_D}$$

$$I_D = \frac{Wa}{\rho L}\left[V_D - \frac{2}{3V_p^{1/2}}\left(V_{bi}^{\circ}+V_D-V_G\right)^{3/2} - \left\{0 - \frac{2}{3V_p^{1/2}}\left(V_{bi}^{\circ}-V_G+0\right)^{3/2}\right\}\right]$$

$$I_D = \frac{Wa}{\rho L}\left[V_D - \frac{2}{3V_p^{1/2}}\left(V_{bi}^{\circ}-V_G+V_D\right)^{3/2} + \frac{2}{3V_p^{1/2}}\left(V_{bi}^{\circ}-V_G\right)^{3/2}\right] \quad (7)$$

* In linear region, $V_D << V_G$ and $V_D << V_{bi}^{\circ}$, so (by binomial series expansion)

$$I_{D\,linear} \approx \frac{Wa}{\rho L}\left[1-\left(\frac{V_{bi}^{\circ}-V_G}{V_p}\right)\right]V_D$$

$$\boxed{I_{D\,linear} \approx G\left[1-\left(\frac{V_{bi}^{\circ}-V_G}{V_p}\right)\right]V_D} \quad (8)$$

where, $G = \frac{Wa}{\rho L}$ → is the channel conductance.

In saturation region, (9)

$$V_D = V_{Dsat} = V_p + V_G - V_{bi}^\circ = V_G - (V_{bi}^\circ - V_p)$$
$$= V_G - V_T$$

↳ gate threshold voltage.

From eqn (7), saturation current is,

$$I_{Dsat} = G\left[\left(V_p - V_{bi}^\circ + V_G\right) - \frac{2}{3V_p^{1/2}}\left(V_{bi}^\circ - V_G + V_p - V_{bi}^\circ + V_G\right)^{3/2} + \frac{2}{3V_p^{1/2}}\left(V_{bi}^\circ - V_G\right)^{3/2}\right]$$

$$= G\left[V_p - (V_{bi}^\circ - V_G) - \frac{2}{3}V_p^{(3/2-1/2)} + \frac{2}{3V_p^{1/2}}(V_{bi}^\circ - V_G)^{3/2}\right]$$

$$= G\left[V_p - (V_{bi}^\circ - V_G) - \frac{2}{3}V_p + \frac{2}{3}\left(V_{bi}^\circ - V_G\right)^{3/2}\frac{1}{V_p^{1/2}}\right]$$

$$\boxed{I_{Dsat} = G V_p\left[\frac{1}{3} - \frac{V_{bi}^\circ - V_G}{V_p} + \frac{2}{3}\left[\frac{(V_{bi}^\circ - V_G)}{V_p}\right]^{3/2}\right]} \quad (9)$$

Extra! For $V_D >> V_{Dsat}$, the pinch-off starts shifting towards source. While there is a shift in the pinchoff point, potential at pinch-off points will remain constant at V_{Dsat}, so Electric field in drain region remain constant and current I_D thus saturates.

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Experimentally it has been found that,

$$I_{Dsat} \approx I_{DSS}\left[1 - \frac{V_{GS}}{V_P}\right]^2 \quad -(10)$$

(10)

where I_{DSS} is the saturation drain current at $V_G = 0$ & is given by,

$$I_{DSS} = \frac{aWV_P}{3SL}$$

* **Transconductance (g_m):**

It is the transistor gain of a JFET. It indicates the amount of control the gate has on drain current.

$$g_m = \frac{\partial I_{Dsat}}{\partial V_{GS}}$$

Experimental transconductance.

From eqn (10), we can write

$$g_{msat} = -\frac{2}{V_P} I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right) \quad -(11)$$

Since, V_P is '-ve' for n-channel JFET,

g_{msat} will be +ve.

* $$g_{msat\,max} \approx \frac{3I_{DSS}}{V_{P0}}\left[1 - \sqrt{\frac{V_{bi}}{V_{P0}}}\right]$$