01

02/08/14

pn Junction Capacitance:

Two types

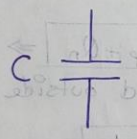
- Diffusion capacitance OR Charge storage capacitance
- Depletion capacitance OR Transition capacitance.

* Diffusion capacitance is dominant under forward-bias conditions, and depletion capacitance is dominant when the junction is reverse biased.

Reference:

In many applications of pn-junctions, the capacitance is a limiting factor in the usefulness of the device; on the other hand, there are important applications in which these capacitance estimation can be useful in circuit applications and in providing important information about the structure of the pn-junction.

Note: For a Parallel Plate Capacitor,



$$C = \frac{\epsilon A}{d}$$

A - Cross-sectional Area between the two plates

d - distance between two plates of capacitor

ϵ - dielectric constant

Also, $C = \frac{Q}{V}$

Q - charge

V - Applied voltage

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02

Diffusion capacitance: (Charge storage capacitance): - C_{diff}

- In a forward bias, a large number of carriers are stored in two sides of the junction ⇒ due to diffusion of carriers across pn junction. ⇒

ie These carriers are stored outside the depletion region ⇒ which gives rise to Diffusion capacitance

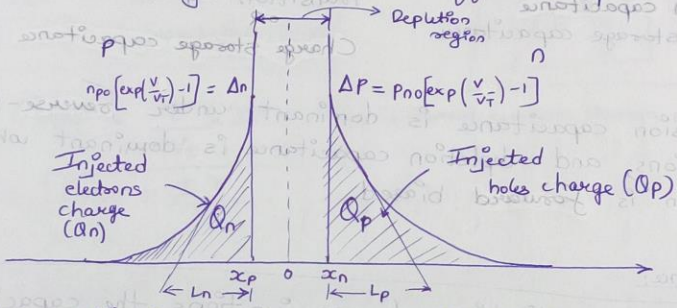

fig a: Minority carrier charge distribution in a pn junction showing the cause of diffusion capacitance in F.B.

∴ The cause of C_{diff} is the injected charge that is stored outside the depletion region in a F.B junction. ie due to injected e⁻s from n side to p side and due to injected holes from p side to n-side. represented by C_{diffn} and C_{diffp} respectively.] C_{diff}

- $C_{diff} = \frac{dQ}{dV}$ —① ; where $\boxed{Q = Q_p + Q_n}$ ⇒ injected charge stored outside depletion region

where, $\boxed{Q_p = q\,\Delta p\, L_p A}$; $\boxed{Q_n = q\,\Delta n\, L_n A}$

Q_p and Q_n → charges in neutral n and p regions of pn junction diode.

From ①, $C_{diff} = \frac{dQ}{dv} = \frac{\tau . dQ}{\tau . dv} = \frac{\tau\, dI}{dv} = \frac{\tau}{r}$

r – incremental resistance $\Rightarrow$ $r = \frac{dv}{dI}$

τ → minority carrier lifetime.

$\Rightarrow \frac{dQ}{\tau dv} \Rightarrow \frac{dI}{dv}$ How?

$I \times t = Q$ $\Rightarrow$ ie (current × time = charge)

Reference

$I = I_0 (e^{(V/V_T)} - 1)$ – ④

$\frac{dI}{dv} \simeq \frac{I_0 e^{V/V_T}}{V_T}$

$\frac{1}{r} \simeq \frac{I}{V_T}$

$r \simeq \frac{V_t}{I}$ becoz $I >> I_0$, neglect (-1) in (a)

Now, $C_{diff} = \frac{\tau}{V_t} \times I$ (I → Forward current through pn junction)

ie $C_{diff} \simeq \frac{I\tau}{V_t}$ – ②

$\Rightarrow$ With ↑se in forward bias $\Rightarrow$ injected charge in both side of junction ↑ses. Therefore, C_{diff} ↑ses.

For Reverse bias, $C_{diff} \to 0$ → (Becoz, under R.B $\Delta p \simeq -p_{no}$, $\Delta n \simeq -n_{po}$)

Depletion capacitances: (Junction Capacitances) : (C_j or (C_{dep})

The origin of these capacitances comes from presence's of uncovered +ve and -ve charges on both side of the junction. (as shown in fig b).

Let us understand this with an incremental picture. ie Applied Reverse bias 'V_R', so if on there is an incremental in V_R ie dV_R $\Rightarrow$ Depletion width ↑ses from W to dW. in a pn junction.

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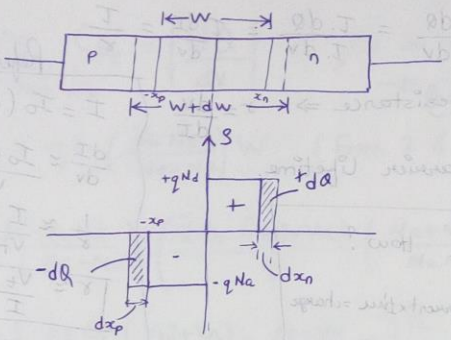

(↑se in -ve charge ≡ ↓se in +ve charge)

fig b: Incremental picture of charges of charges at the edges of a depletion layer. for a uniformly doped pn junction.

⇒ Figure b shows charge densities in the depletion region for applied R.B of V_R and $V_R + dV_R$.

• An increment in reverse-bias dV_R will uncover additional +ve charges in n region and additional -ve charges in the p-region.

Now, $W = \left[\frac{2\varepsilon_s (V_{bi}+V_R)}{q}\left(\frac{N_a+N_d}{N_a N_d}\right)\right]^{1/2}$ (--- For R.B) — ①

↓ Depletion region width.

⇒ Since uncompensated charge Q on each side of the junction varies with W, ⇒ variations in V_R ⇒ variation in charge as required for a capacitor. [$C = |dQ/dV|$]

Now, $|Q| = qA x_n N_d = qA x_p N_a$ — ②

Now, $x_n = \left(\frac{N_a}{N_a+N_d}\right)W$ and $x_p = \left(\frac{N_d}{N_a+N_d}\right)W$ — ③

$\therefore$ Now, $C_{dep} = \left| \frac{dQ}{dV} \right|$; $V \Rightarrow V_{bi}+V_R$ $\Rightarrow$ → (4a)

(charge on each side)

because the voltage that varies the charge in depletion region is the barrier height i.e $(V_{bi}+V_R)$

Now, $|Q| = qA.\left(\frac{N_d N_a}{N_d+N_a}\right) W$ (From 2 & 3)

$$|Q| = qA\left(\frac{N_a N_d}{N_a+N_d}\right)\left[\frac{2\epsilon_s (V_{bi}+V_R)}{q}\left(\frac{N_a+N_d}{N_a N_d}\right)\right]^{1/2}$$

$$|Q| = A\left[2q\epsilon_s (V_{bi}+V_R) \times \frac{N_a N_d}{N_a+N_d}\right]^{1/2} \quad — (4b)$$

Eq^n (4b), tells us that charge Q on each side of depletion region varies nonlinearly with applied voltage.

Now, $C_{dep} = \left| \frac{dQ}{d(V_{bi}+V_R)} \right|$ (From 4a),

$$\therefore C_{dep} = \frac{A}{2}\left[\frac{2q\epsilon_s}{(V_{bi}+V_R)} \frac{N_a N_d}{N_a+N_d}\right]^{1/2} \quad — (5)$$

Reference: C_j or C_{dep} is a voltage-variable capacitance, since $C_j \propto (V_{bi}+V_R)^{-1/2}$

There are several important application's for variable capacitors, including use in tuned circuits.

- The pn-junction device which makes use of the voltage-variable property of C_j is called "Varactor diode".

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Now, from ⑤, we get

$$C_{dep} = \epsilon_s A \left[\frac{q}{2\epsilon_s (V_{bi}+V_R)} \frac{N_a N_d}{N_a+N_a} \right]^{1/2}$$

From ①, $W = \left[\frac{2\epsilon_s (V_{bi}+V_R)}{q} \left(\frac{N_a+N_d}{N_a N_d} \right) \right]^{1/2}$

$$\therefore \boxed{C_{dep} = \frac{\epsilon_s A}{W}} \quad - ⑥$$

This eqn resembles parallel plate capacitor i.e $\boxed{C = \frac{\epsilon A}{d}}$

In Reverse Bias ↓ — pn junction

$C_{dep} = \frac{\epsilon A}{W}$

So, a R.B diode is almost like a pure capacitor, & its value vary with vtg (V_R)

V_R - R.B voltage

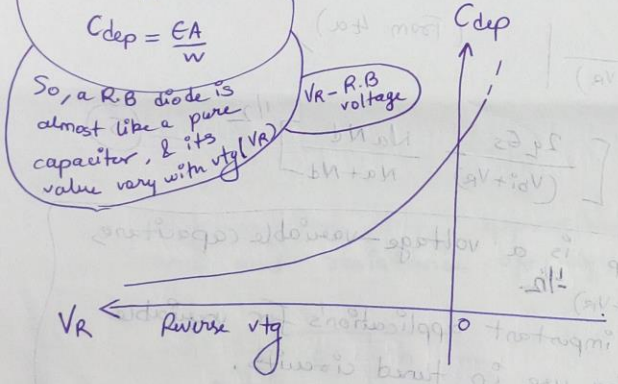


fig: Variation of C_{dep} with reverse bias.

From ⑥ since W depends on reverse bias voltage.

- C_{dep} is also a function of R.B voltage of the pn junction.

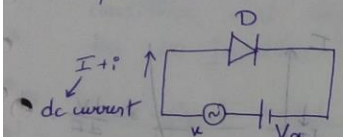
$\therefore$ V_R ↑ses, C_{dep} ↓ses.

07R

Small-signal model of the pn junction :-

→ Equivalent circuit of diode under small-signal conditions.

• When semiconductor devices with pn junctions are used in Linear amplifier circuits, for eg, small ac signals are superimposed on the dc currents and voltages, so that the small-signal characteristics of pn junction become important.



Va - Applied F.B
D - pn junction diode

$v = V_m \sin \omega t$ → mag^n of ac voltage is small

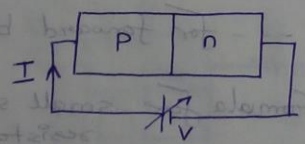
$V_m << V_t$ → Thermal voltage

$i = I_m \sin(\omega t + \theta)$ ← small-s/g current.

• Quasi-static approach (small-signal model):

↳ We will try to derive formulae for ac conditions from dc (static) characteristics.

↳ It gives you only approximate estimate of capacitance and resistance of equivalent circuit.



$V \rightarrow I$

$V + dV \rightarrow I + dI$

charge Q stored for V

$V \rightarrow Q$

$V + dV \rightarrow Q + dQ$

• When current changes from I to I+dI, charges Q inside the device also will change ie Q+dQ.

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- In quasi-static small-signal model, we are making a change in voltage and we are estimating the changes in current and charges, but we give sufficient time for effects of charge to stabilize.

$$r = \frac{dV}{dI}$$; $$C = \left|\frac{dQ}{dV}\right|$$

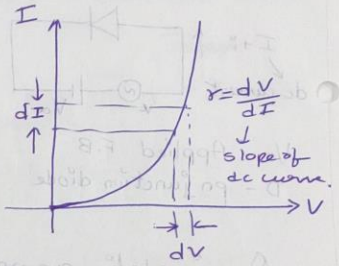
small signal incremental resistance. (or Diffusion resistance)

C → capacitance

→ It represents either +ve or -ve component.

→ Ideal-diode equation:

$$I = I_0\left[\exp\left(\frac{V_a}{V_t}\right) - 1\right] \quad -(1)$$



Differentiate (1) w.r.t voltage V_a

$$\frac{dI}{dV} \approx \frac{I_0 \exp\left(\frac{V_a}{V_t}\right)}{V_t}$$

ie $$\frac{1}{r_d} \approx \frac{I}{V_t}$$ (neglect (-1) in (1))

∴ Now for F.B, $I > I_0$

∴ $$\boxed{r_d \approx \frac{V_t}{I}}$$ ---- for forward bias.

↳ Formula for small signal resistance.

∴ r_d ↓ses as I ↑ses. and r_d ↑ses as I ↓ses.

The incremental resistance is also known as the 'diffusion resistance.'

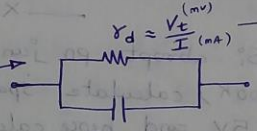
For reverse bias, $I_R = -I_0$

$\therefore$ $r_d \to \infty$ for ideal diode.

But in real diode, $r_d \neq \infty$, becoz I_R ↑ses with V_R.
So, we have finite non-zero conductance $\left(\frac{dI}{dV}\right)$
$\therefore$ r_d will be in order of (> 100 KΩ) - for R.B.

- Diffusion capacitance (C_{diff}) is dominant under forward-bias conditions, and depletion capacitance (C_{dep}) is dominant when the pn junction is reverse-biased.

- Small-signal model for F.B pn junction:

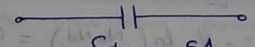


$r_d \approx \frac{V_t\,(mV)}{I\,(mA)}$ → (few ohms)

$C_{diff} \approx \frac{I\tau}{V_t}$ → (~nf)

Why r_d and C_{diff} are in parallel?
Ans: Voltage V is responsible for I and charge Q is the same. Since r_d and C_{diff} are due to common vltg V i.e vltg across r_d and C_{diff} is same.

- Small-signal model for R.B pn junction:



$C_{dep} \approx \frac{\epsilon A}{W}$ → (~pf)

(For R.B we haven't shown r & C_{diff} becoz they are neglible). (r: v.v. high; C_{diff}: negligible)

- Complete small-signal model of pn junction: fig (d)

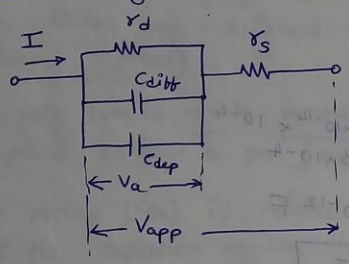


fig (d) pn junction diode equivalent circuit

- In order to complete the small signal model, we need to add C_{dep} which will be in parallel with r_d and C_{diff}.

• To last element we add, to complete the small-signal equivalent circuit, is a series resistance (r_s). (The neutral n and p regions have finite resistances so the actual pn junction will include R_s).

∴ In fig (d), the voltage across the actual junction is V_a and the total voltage applied to pn junction is given by V_{app}.

ie $\boxed{V_{app} = V_a + I r_s}$

—x—

1. For a Si abrupt pn junction, $N_a = 10^{16}/cm^3$ and $N_d = 10^{15}/cm^3$ at $T = 300K$, calculate space-charge → width W at a $V_R = 5V$ and hence calculate depletion capacitances. for junction area $A = 10^{-4} cm^{-2}$

Soln: $W = \left[\frac{2\epsilon_s (V_{bi} + V_R)}{q}\left[\frac{N_a + N_d}{N_a N_d}\right]\right]^{1/2}$

But, $V_{bi} = V_T \ln\left(\frac{N_a N_d}{n_i^2}\right) = 0.0259 \ln\left(\frac{10^{16} \times 10^{15}}{(1.5 \times 10^{10})^2}\right) = 0.635V$

$\therefore W = \left[\frac{(2 \times 11.7 \times 8.85 \times 10^{-14})(0.635 + 5)}{1.6 \times 10^{-19}}\left(\frac{10^{16} + 10^{15}}{(10^{16})(10^{15})}\right)\right]$

$W = 2.83 \times 10^{-4} cm \approx 2.83 \mu m$

Now, $C_{dep} = \frac{\epsilon A}{W}$

$= \frac{11.7 \times 8.854 \times 10^{-14} \times 10^{-4}}{2.83 \times 10^{-4}}$

$0.366 \times 10^{-12} F$

$\boxed{C_{dep} = 0.366 pF}$

—x—