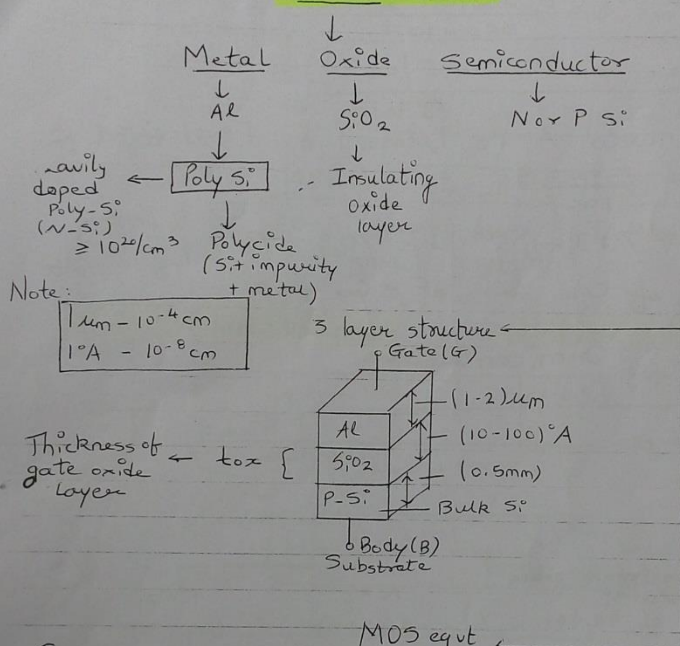
Physics of MOS device

- MOSFET is the fundamental building block of MOS & CMOS digital ICs.
- Compared to BJT, the MOS T^r occupies a relatively smaller Si area, and its fabrication used to involve fewer processing steps.

MOS device



MOS equt

{MOS structure forms a capacitor with gate & substrate as 2 terminal & oxide layer as dielectric.} ← MOS capacitor eg DRAM (MOSCAP)

C_{ox} → Gate oxide Capacitance

Unit: Cap/unit area F/cm^2

$$C = \frac{\epsilon A}{d} \rightarrow \frac{C}{A} = \frac{\epsilon}{d}$$

$$\therefore \boxed{C_{ox} = \frac{\epsilon_{ox}}{t_{ox}}} \quad F/cm^2$$

where, $\epsilon_{ox} = \epsilon_0 \epsilon_r$ F/cm.

ϵ_0 - Dielectric constant of vacuum = 8.854×10^{-14} F/cm

ϵ_r → 3.97

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$$\boxed{\epsilon_{ox} = 3.97 \times \epsilon_0}$$ → Dielectric const of SiO_2.

Q. If $t_{ox} = 500 \text{Å}$. Find C_{ox}

Soln: $C_{ox} = \frac{\epsilon_{ox}}{t_{ox}} = \frac{\epsilon_0 \epsilon_r}{t_{ox}}$

$C_{ox} = \frac{8.854 \times 10^{-14} \times 3.97}{500 \times 10^{-8}} = 7.08 \times 10^{-8}$

$$\boxed{C_{ox} = 70.3 \ nF/cm^2}$$

Q. If Plate area A is $1\mu m \times 1\mu m$, Find total C.

⇒ $C_{ox} = \frac{\epsilon_{ox}}{t_{ox}} A. = 70.3 \times 10^{-9} \times 10^{-8}$

$C_{ox} = 703 \times 10^{-18} = 703 \ aF$

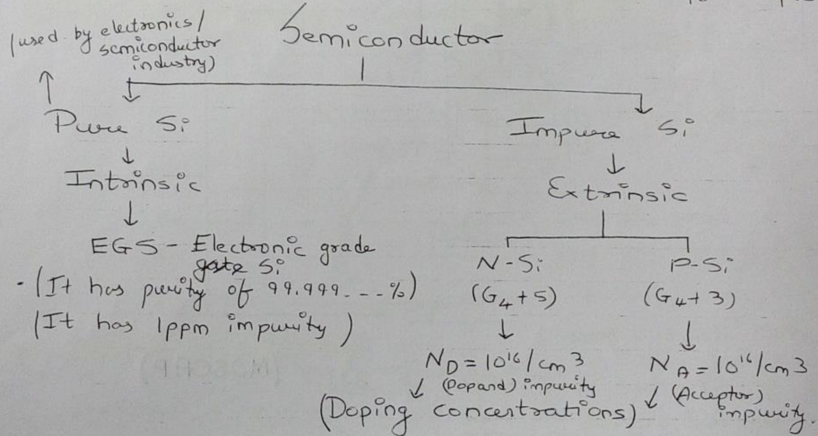
↓

Range of C_{ox} → $zF \leq C_{ox} \leq fF$

10^{-15} – f

10^{-18} – atto (a)

10^{-21} – zepto



Since, equilibrium concentration of mobile carriers in a Semiconductor always obeys Law of Mass Action ie

$$\boxed{n \times p = n_i^2}$$

↓ mobile carrier concn of e^- & holes

where,

n – e^- concn in C.B

p – hole concn in V.B

n_i – intrinsic carrier concn of Si at T=300

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$n_i = 1.45 \times 10^{10}$ /cm³
$n_i^2 = 2.1 \times 10^{20}$ /cm⁶

{At t = 0°C, Si is insulator}

- Order of leakage current in Si → 10^{-9}A, Ge → 10^{-6}A.

Insulator :- No free e⁻s
{Conductor :- All free e⁻s
{Metal :- Au free e⁻s
Semi-cond :- less no of free e⁻s

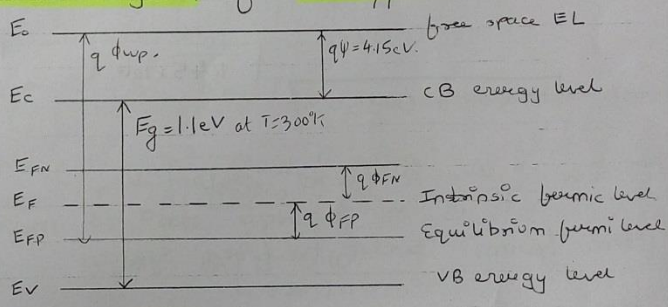
- Energy band diagm :
  - C.B
  - V.B
  - Forbidden gap
  - Fermi level

It indicates the probability of occupancy of C.B which is

$$P(E) = \frac{1}{1 + e^{[(E-E_F)/KT]}}$$

where, E_F - Fermi energy level, T - temp
K - Boltzman's constant.

- Energy band diagram of a P-type Si



ψ - Electron affinity (V) :-
It is energy difference betⁿ free space & CB.
Eg - Band gap energy. betⁿ CB & VB for Si is 1.1eV.

ϕ_F - Fermi Potential (V)
- ϕ_{FP} (-ve)
- ϕ_{FN} (+ve)

For P-type Si

$$\phi_{FP} = \frac{KT}{q} \ln\left(\frac{n_i}{N_A}\right) \text{ Volts}$$

$$\phi_F = \frac{E_{F_{N/P}} - E_i}{q}$$

(Fermi level)

For N-type Si

$$\phi_{FN} = \frac{KT}{q} \ln\left(\frac{N_D}{n_i}\right) \text{ Volts}$$

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$$\frac{KT}{q} = \frac{1.38 \times 10^{-23} J/K \times T}{1.6 \times 10^{-19}} = \frac{T}{11,600}$$

$$\boxed{\frac{KT}{q}} = 0.026V \quad \text{at } T = 300°K.$$

$q \rightarrow$ unit e^- charge

↘ Volt equt of temp.
(Thermal vtg)

Q. For a P-Si, $N_A = 10^{16}/cm^3$, find ϕ_{FP}

=> $\phi_{FP} = \frac{KT}{q} \ln\left(\frac{n_i}{N_A}\right)$

$= 0.026 \ln\left(\frac{1.45 \times 10^{10}}{10^{16}}\right)$

$$\boxed{\phi_{FP} = -0.35V}$$

Q. For an N-Si, $N_D = 10^{16}/cm^3$, find ϕ_{FN}

=> $\phi_{FN} = \frac{KT}{q} \ln\left(\frac{N_D}{n_i}\right)$

$= 0.026 \ln\left(\frac{10^{16}}{1.45 \times 10^{10}}\right)$

$$\boxed{\phi_{FN} = 0.35V}$$

→ ϕ_w - Work functn potential

It is min energy reqd to move a e^- from fermi level to free space.

Here, $\phi_{wp} = \varphi + \frac{1.1}{2} + |\phi_{FP}|$

$= 4.15 + 0.55 + 0.35$ say

$$\boxed{\phi_{wp} = 5.05 V}$$

=> $\phi_{wN} = \varphi + \frac{1.1}{2} - |\phi_{FN}|$

$= 4.15 + 0.55 - 0.35$

$$\boxed{\phi_{wN} = 4.35 V}$$

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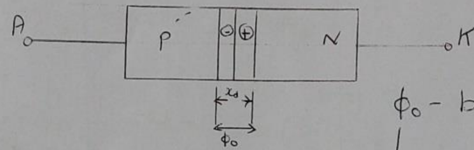
• When two materials of diff work funct^n are joint together, there exists a potential diff at point of contact.

eg $\phi_w = \phi_{wp} - \phi_{wN} = 5.05 - 4.35 = 0.7V$

PN - J^n diode → barrier potential is 0.7V.

Note:- In a P-N J^n diode,



ϕ_o - barrier / J^n / contact potential.

It is due to work funct^n diff bet^n P & N Si.

$\phi_o = \phi_{FN} - \phi_{FP}$

$$\phi_o = \frac{KT}{q} \ln\left[\frac{N_A N_D}{n_i^2}\right] \quad \text{Volts}$$

$\therefore \quad \phi_o = f(N_A, N_D, T)$.

Q. If $N_A = 10^{16} /cm^2$, $N_D = 10^{18} /cm^2$; find ϕ_o.

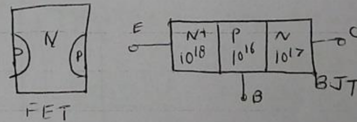
$\Rightarrow \quad \phi_o = \frac{KT}{q} \ln\left[\frac{N_A N_D}{n_i^2}\right]$

$= 0.026 \ln\left[\frac{10^{16} \times 10^{18}}{2.1 \times 10^{20}}\right]$

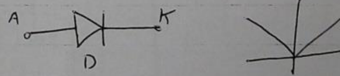
$\phi_o = 0.818$ Volts

* Types of Junctions:-

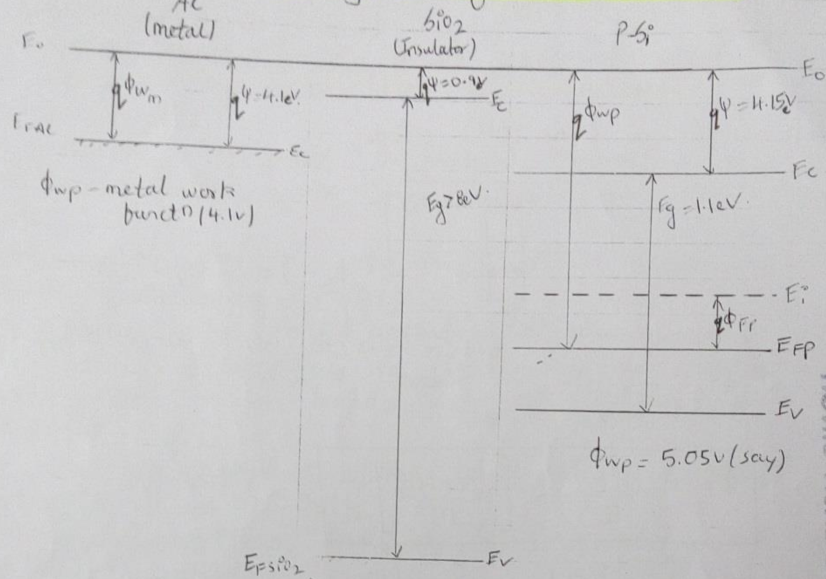
1. Step / abrupt J^n:-
   - Diff doping conc^n
   - eg EB J^n, BJT, FET



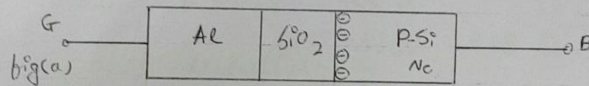
2. Graded J^n:-
   - Same doping conc^n
   - eg Diode.

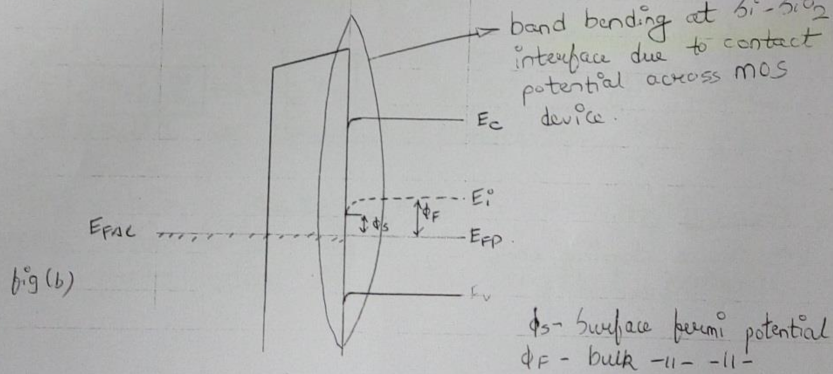


Energy band diagram of MOS element.



- Energy band diagram of MOS device :- mos capacitor.
  - All 3 fermi levels will align as a straight line
  - The device becomes electrically neutral.





ϕ_s - Surface fermi potential
ϕ_F - bulk -"- -"-

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→ Now we consider that 3 components of ideal MOS system are brought into physical contact. as shown in fig(a).

→ The Fermi levels of all three materials must line up, as they form the MOS capacitor as shown in fig(a).

→ Because of work-functⁿ difference between metal (Al) and semiconductor, a vtg drop occurs across MOS device

→ Part of this built-in vtg drop occurs across the insulating oxide layer (SiO_2).

∴ The rest of vtg drop (potential difference) occurs at (P-Si) - SiO_2 interface ie Silicon-oxide interface, forcing the energy bands of Si to bend in this region.

→ The resulting combined energy band diagⁿ of MOS system is shown in fig (b).

Note:- Equilibrium Fermi levels of (Si) & metal gate are at same potential.

→ The bulk Fermi level is not significantly affected by band bending, whereas the surface Fermi level moves closer to intrinsic Fermi level.

→ The Fermi potential at the surface ie 'surface potential (ϕ_S)', is smaller in magnitude than bulk Fermi Potential (ϕ_F).

Q. Why band bending in MOSCAP:

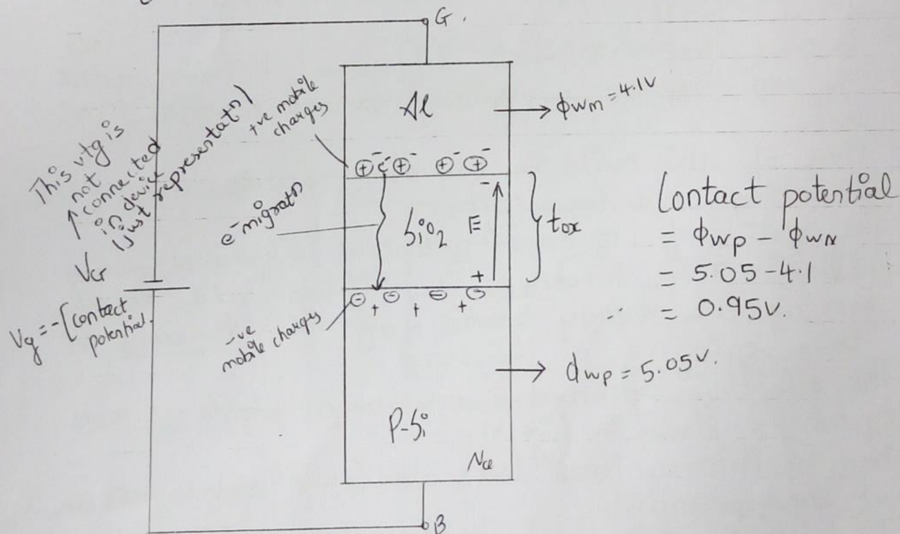
⇒

1. When a MOS device is formed, the work functⁿ diff betⁿ the P-Si & Al metal will create a contact potential across a MOS device

The major part of this potential across the SiO_2 layer.

2. The field due to the contact potential

will pull the e⁻s from Al metal, due to e⁻ migration from Al to P-Si, the surface concentration of charges in P-Si at $Si-SiO_2$ interface will decrease.



Contact potential
$= \phi_{wp} - \phi_{wm}$
$= 5.05 - 4.1$
$= 0.95V$.

3. Hence the surface of P-Si becomes less +ve compared to the bulk Si & hence the surface fermi potential will be less than bulk fermi potential.
4. This phenomenon leads to BAND BENDING at $Si-SiO_2$ interface of a MOS device.