* C-V characteristics of MOSCAP

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- Study of C-V characteristics of MOSCAP gives a great deal of information about the MOS device and oxide-semiconductor interface.

→ Ideal C-V curve :

- We consider small-signal capacitances given by

$$C = \left| \frac{dQ}{dV} \right| \quad \text{ie} \left[\frac{\text{differential change in charge}}{\text{differential change in voltage}} \right]$$

- Assume that there are no trapped charges in oxide and oxide-semiconductor interface.

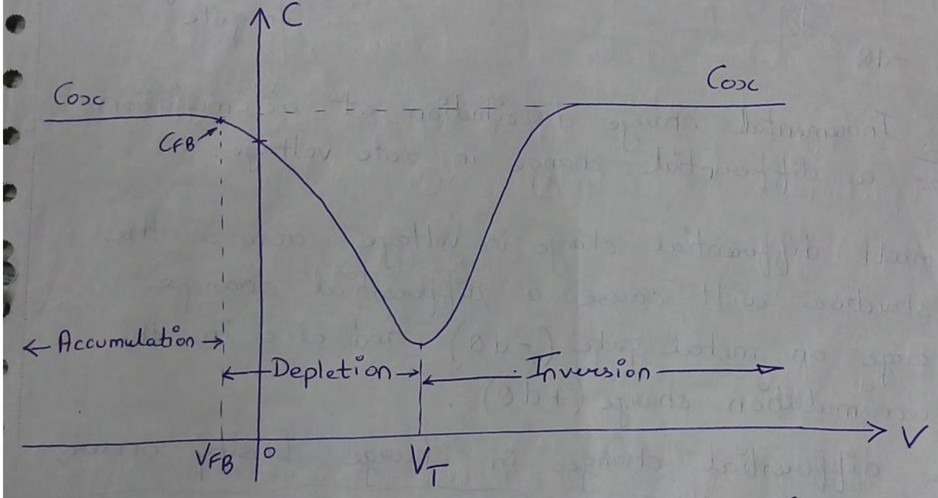


fig (1.a) : Ideal low-frequency C-V curve for a MOSCAP with ptype substrate

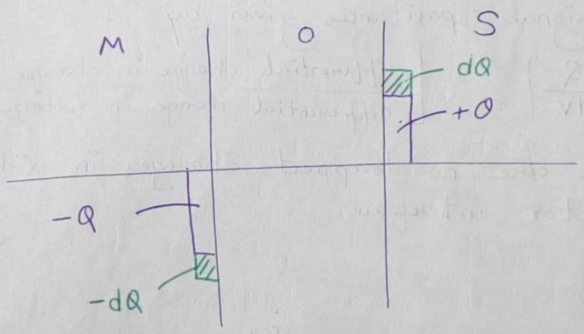
V_{FB} → Flat-band voltage.

V_T → Threshold voltage.

- 3 operating conditions of interest in MOSCAP are,
  a) Accumulation b) Depletion c) Inversion

1) Accumulation :

- When a negative gate voltage is applied, it induces accumulation of holes beneath $Si-SiO_2$ interface.



"Accumulation Case"

+Q ⇒ +ve charge in semiconductor.
- Q ⇒ -ve charge induced in gate

fig (1.b) : Incremental charge distribution at accumulation for a differential change in gate voltage.

- A small differential change in voltage across the MOS structure will cause a differential change in charge on metal gate (-dQ) and also in the hole accumulation charge (+dQ).
- Since differential changes in charge density occurs at the edges of oxide

$$\therefore \boxed{C_{(acc)} = C_{ox} = \frac{\epsilon_{ox}}{t_{ox}}}$$

Thus capacitance's at accumulation is just oxide capacitance.

Similar to a Parallel Plate capacitor, in this case we have a +ve charge in semiconductor and a -ve charge in gate, separated by a oxide.

2) Depletion :

- When a small +ve gate voltage is applied to a MOSCAP, it induces a depletion region in semiconductor.

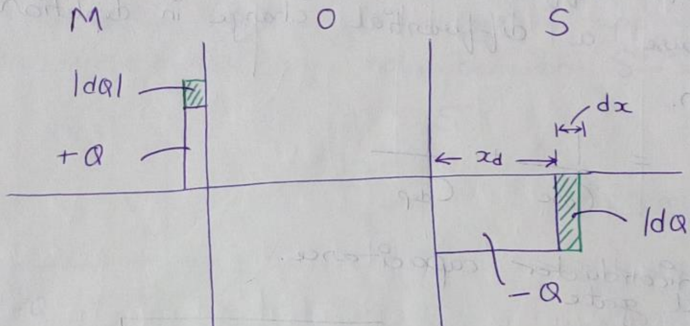


Fig (1.c) Differential charge distribution at depletion for a differential change in gate voltage.

- In depletion region (ie between V_{FB} and V_T), C is falling (why) ?
- When we change voltage, there is a change in charge and that change occurs at 'edge' of depletion layer.

$\Downarrow$

Extra ! !

(These changes are incremental changes)
ie
a) Change in increment +ve charge (dQ) at gate
b) Change in increment -ve charge (dQ) in semiconductor at edge of depletion layer.

- In depletion case, there is oxide capacitances and depletion layer capacitances (which are in series).
- Thus, a small differential change in voltage across C will cause a differential change in depletion layer width.

ie $$\frac{1}{C_s} = \frac{1}{C_{ox}} + \frac{1}{C_{dep}}$$

C_s → ~~Semiconductor~~ Total gate capacitance.

$$C_s = \frac{C_{ox} C_{dep}}{C_{ox} + C_{dep}} \; ; \quad \boxed{C_{ox} = \frac{\epsilon_{ox}}{t_{ox}}}$$

$$\boxed{C_{dep} = \frac{\epsilon_s}{x_d}}$$; x_d → depletion layer width.

ie $$C_s = \frac{C_{ox}}{1 + \frac{C_{ox}}{C_{dep}}} = \frac{\epsilon_{ox}}{t_{ox} + \left(\frac{\epsilon_{ox}}{\epsilon_s}\right) x_d}$$

∴ As x_d ↑ses, total C_s ↓ses.

This explains why Capacitances goes on falling between V_{FB} and V_T (ie depletion case) because distance between incremental charges are changing as show in fig(1.c).

Extra:!!

At maximum depletion width (x_d)

↓

Minimum gate capacitance's

$$\boxed{C_{min} = \frac{\epsilon_{ox}}{t_{ox} + \left(\frac{\epsilon_{ox}}{\epsilon_s}\right) x_{dm}}}$$

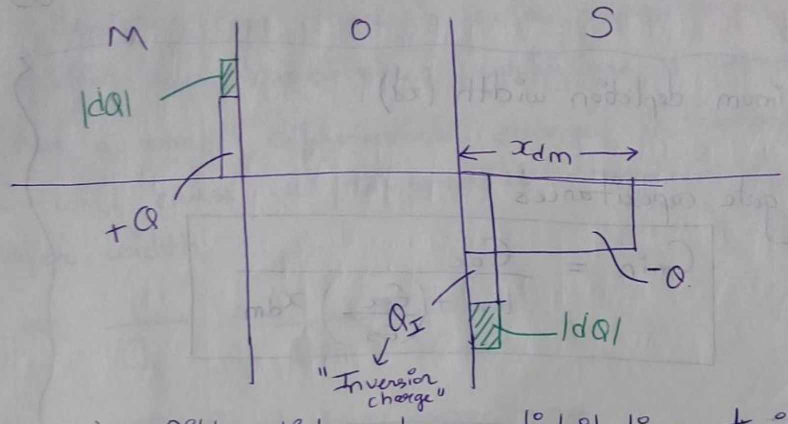
where,

$$x_{dm} = \sqrt{\frac{2\epsilon_s |-2\phi_F|}{q N_A}} = \sqrt{\frac{4\epsilon_s \phi_f}{q N_A}}$$

3) Inversion:

- In ideal case, a small incremental change in gate voltage will cause a differential change in inversion layer charge density
- Space-charge width (x_d) does not ↑se beyond V_T, thus inversion charge corresponds to change in voltage. Thus capacitance is again just oxide capacitance 'Cox'.

$$\boxed{C_{(Inv)} = C_{ox} = \frac{\epsilon_{ox}}{t_{ox}}}$$



fig(1.d) : Differential charge distribution at inversion for a low-frequency differential change in gate voltage

In inversion region, C again rises up to C_{ox} ?

- This means, "incremental charges" are now coming from $Si-SiO_2$ interface. (As depletn layer width reachs max value x_{dm})

{ Beyond V_T, we get more mobile charges appear near $Si-SiO_2$ interface }.

- In case of inversion, the incremental charges are coming from mobile -ve charge's near the interface. as shown in fig.(1.d).

- That explain's qualitatively behavior of C as a function of gate voltage at low frequency.

* Flat band condition occurs between accumulation and depletion conditions:

Thus, capacitance at flat-band condition is,

$$\boxed{C_{FB} = \frac{\epsilon_{ox}}{t_{ox} + \left(\frac{\epsilon_{ox}}{\epsilon_s}\right)\sqrt{\left(\frac{KT}{q}\right)\frac{\epsilon_s}{qNa}}}}$$

Ex: Consider a ptype Si substrate at T=300K doped with $Na = 10^{16}/cm^3$, SiO_2 oxide thickness 550°A and gate is aluminium for a MOSCAP. Find oxide capacitance, minimum gate capacitances and flat-band capacitance.

Sol^n: 1) Gate oxide capacitance (C_{ox}):

$$C_{ox} = \frac{\epsilon_{ox}}{t_{ox}} = \frac{3.97 \times 8.854 \times 10^{-14}}{550 \times 10^{-8}}$$

$$\boxed{C_{ox} = 6.39 \times 10^{-8} \ F/cm^2}$$

2) Minimum gate capacitance (C_{min}):

$$C_{min} = \frac{\epsilon_{ox}}{t_{ox} + \left(\frac{\epsilon_{ox}}{\epsilon_s}\right) x_{dm}}$$

Now, $x_{dm} = \sqrt{\frac{2\epsilon_s |-2\phi_{Fp}|}{qN_a}}$

$\phi_{Fp} = \frac{KT}{q} \ln\left[\frac{N_a}{n_i}\right]$ $\qquad \frac{KT}{q} = V_T = 0.0259$

$= 0.0259 \ln\left[\frac{10^{16}}{1.5\times10^{10}}\right]$

$\phi_{Fp} = 0.3473$ V

ie $x_{dm} = \sqrt{\frac{2\times 11.7\times 8.854\times10^{-14}\times 2\times0.3473}{1.6\times10^{-19}\times10^{16}}}$

$x_{dm} = 30\times10^{-6}$ cm

ie $C_{min} = \frac{\epsilon_{ox}}{t_{ox} + \left(\frac{\epsilon_{ox}}{\epsilon_s}\right)x_{dm}}$

$= \frac{3.97\times8.854\times10^{-14}}{550\times10^{-8} + \left(\frac{3.9766}{11.760}\right)\times30\times10^{-6}}$

$\boxed{C_{min} = 2.242\times10^{-8}\ F/cm^2}$

3) Flat-band capacitances (C_{FB}):

$C_{FB} = \frac{\epsilon_{ox}}{t_{ox} + \frac{\epsilon_{ox}}{\epsilon_s}\sqrt{\frac{KT}{q}\left(\frac{\epsilon_s}{qN_a}\right)}} = 5.1\times10^{-8}\ F/cm^2$

$\boxed{C_{FB} = 5.1\times10^{-8}\ F/cm^2}$

* Frequency effects on a MOSCAP C-V curve :

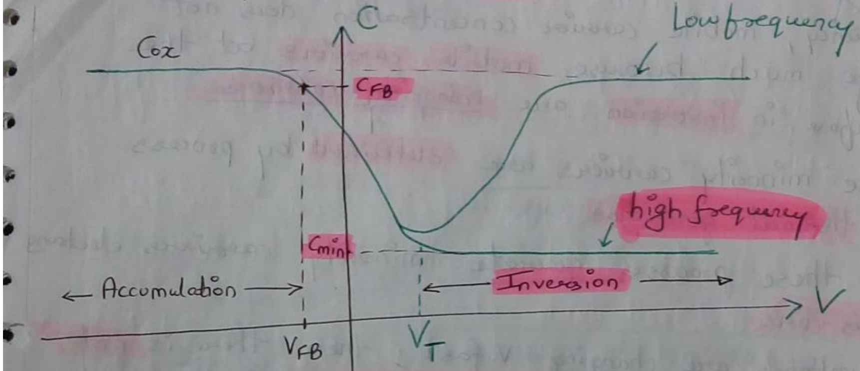


fig (2.a): Low-frequency and high-frequency capacitance versus gate voltage of a MOSCAP with a ptype substrate

- When a MOSCAP is biased in inversion condition, and if frequency is high, then we cannot provide changes in the mobile carrier concentration (ie electrons) at the interface very easily.
- At high frequency, voltage changes rapidly, thus there is no way Q_I (inversion charge) will be able to respond in time ie the electrons have no opportunity to respond.
- Thus, at high frequency, only depletion region differential charge changes, thus capacitances almost remain's constant at Cmin. as shown in fig (2.a).

- The argument that in inversion condition at high frequency, mobile carrier concentration does not change much because mobile carriers at the interface in inversion are minority carriers.
- These minority carriers are obtained by process of thermal generation.
- But these processes generate minority carriers electrons takes time
- If voltage's are changing v. fast, then there is not sufficient time for minority carriers to be generated.
- Therefore, for rapid changes in gate voltage, in inversion case, the differential change in charges cannot come from inversion charge (Q_I), it comes infact from edge of depletion layer charge (Q_D).
- Because, majority carrier charge can be changed quickly in response to change in voltage.
- Thus, at high frequency, incremental charges are coming from depletion charge (since width of depletion layer saturates) beyond V_T, capacitance in inversion almost does not change much and remains constant at Cmin.

That explain's C behavior as a function of voltage at high frequency.

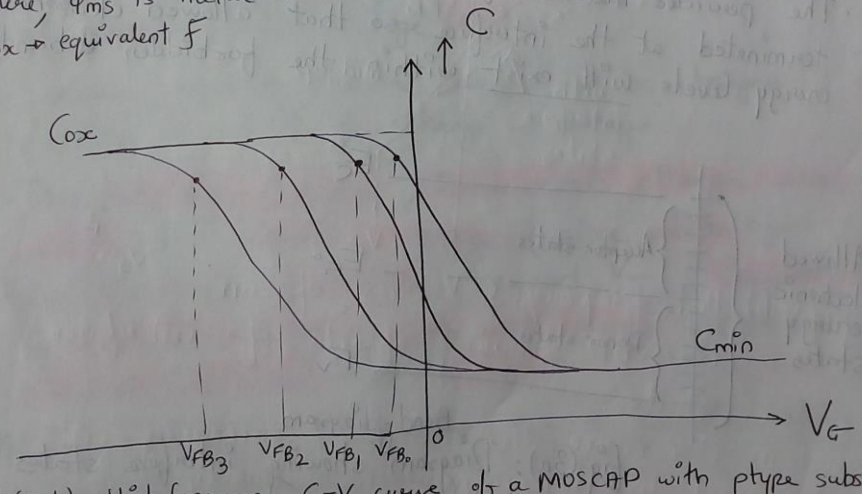
* Fixed oxide and Interface charge effects on C-V characteristics of MOSCAP :

- For ideal C-V curve of MOSCAP, we have assumed an ideal oxide in which there are no fixed change at oxide or $Si-SiO_2$ interface.
- Considering fixed oxide charges and interface charges effect's will change the C-V characteristics.

a). Fixed oxide charge affects flat-band voltage and threshold voltage.

$$\boxed{V_{FB} = \phi_{ms} - \frac{Q_{ox}}{C_{ox}}} \quad — ①$$

where, ϕ_{ms} is metal-semiconductor work function difference.
Q_{ox} → equivalent f



fig(2.b): High frequency C-V curve of a MOSCAP with ptype substrate for several values of effective trapped oxide charge

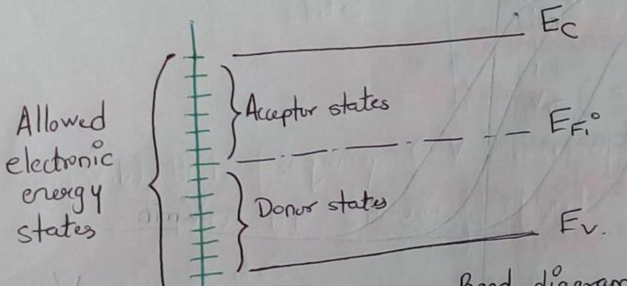
- The flat-band voltage shifts to more negative voltages for a positive fixed oxide charge.
- Since the oxide-charge is not a function of gate voltage, the C-V curves show a parallel shift with oxide charge and the shape of the C-V curves remains the same as the ideal C-V curves.

* The C-V characteristics can be used to determine the equivalent fixed oxide charge. For a given MOS structure, if ϕ_{ms} and C_{ox} are known, the ideal flat-band voltage and flat-band capacitance can be calculated.

b) Effect of interface charges on C-V curve:

Fig (3a) shows the EBD of a semiconductor at Si-SiO$_2$ interface.

- The periodic nature of the semiconductor is abruptly terminated at the interface so that allowed electronic energy levels will exist within the forbidden bandgap.



Band-diagram ⇓

fig (3a): Diagram showing interface states at the oxide-semiconductor interface.

- "These allowed energy states are referred to as "interface states".

- Charge can flow between the semiconductor and interface states, in contrast to the fixed oxide charge.

- The net charge in these interface states is a function of the position of the Fermi-level in the bandgap and hence a function of the gate voltage applied across the MOSCAP.

- Effect of interface states is that the C-V curves now become "smeared out" as shown in fig(3.b). This Figure shows the movement of C-V curve due to interface states.

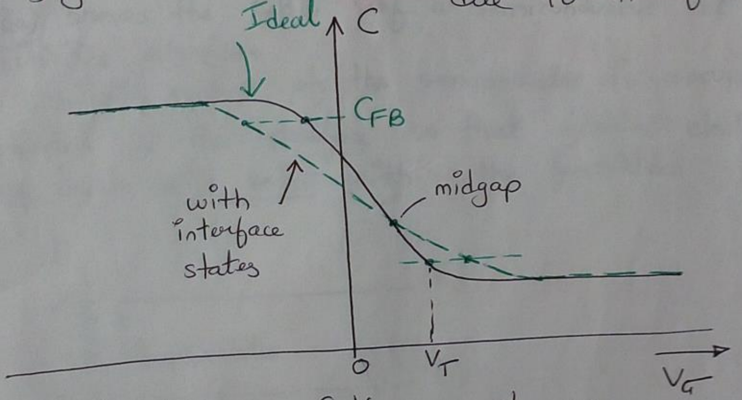


fig (3.b) High-frequency C-V curve of an MOSCAP showing effects of interface states.

- From C-V curve, the amount of smearing out can be used to determine the density of interface states.

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