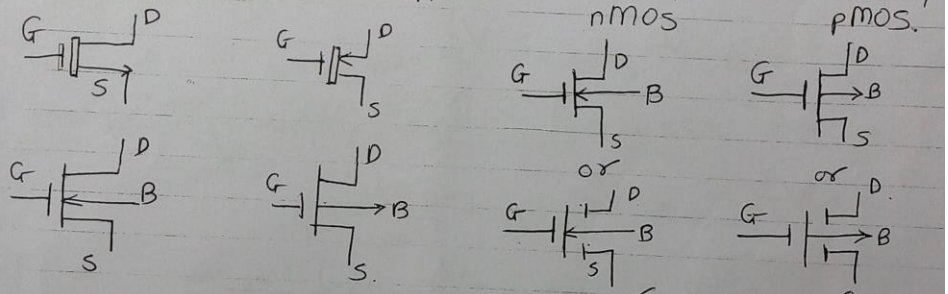
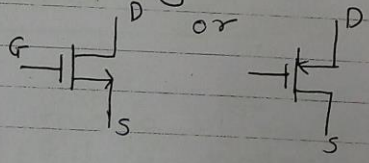
↦ MOSFET Operation:-

MOSFETs

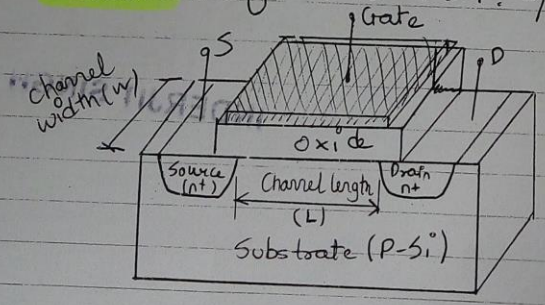
- Depletion MOSFET mode
  - n-Channel MOSFET/nMOS
  - p-channel MOSFET/pMOS
- Enhancement mode MOSFET
  - n-channel MOSFET/ nMOS
  - p-chan ; MOSFET/ pMOS.



Symbols.



↦ Schematic of MOSFET:-/MOS Tr



From the schematic of MOSFET/MOS Tr
- → The source & drain regions are heavily doped
- → The distance betn source & drain diffusion region is called the channel length 'L'.
- → Similarly, the lateral extent of the channel (inside the semiconductor) is known as channel width W.
- → The thickness of oxide layer is taken as t_{ox}.

∴ L, W and t_{ox} are important parameter for determining the electrical behaviour of MOSFETs.

The gate material is usually Poly Si or Al and the length of the gate is almost equal to channel length L.

MOS Tr

Depletion MOS Tr — "normally on" device
↓
At zero gate vtg, & a fixed drain voltage, the current is a maximum, & then ↓ses with applied gate potential.

Enhancement MOS Tr — "normally off" device
↓
Exhibits no current at zero gate vtg & the magnitude of o/p current ↑ses with ↑ses in the magnitude of gate potential.

→ CMOS technology only supports Enhancement-type MOS :-

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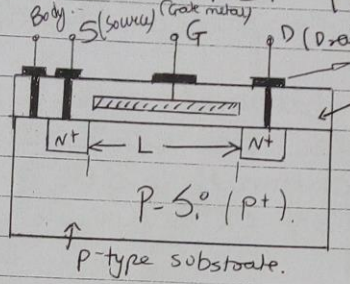
- Enhancement Mode MOSFET:-

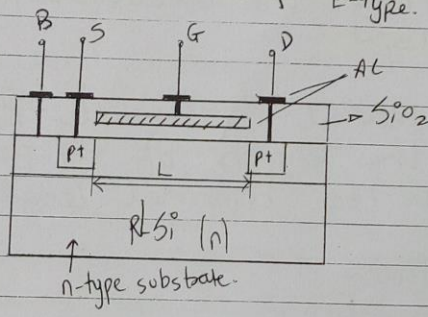
1. p-channel MOSFET (PMOS):-



- It is because of SiO_2 layer, MOSFET have a high I/p resistance.

2. p-channel MOSFET (PMOS)

E-type.



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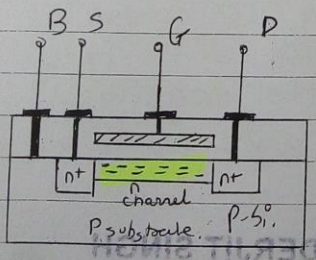
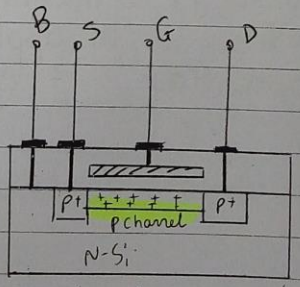
- Depletion Mode MOSFETs:-

If a narrow n-channel or p-channel is embedded into the substrate betn source & drain at time of fabrication, structure is known as Depletion ~~region~~ type MOSFET



n-channel MOSFET (NMOS D-type)



p-channel MOSFET (PMOS D-type)

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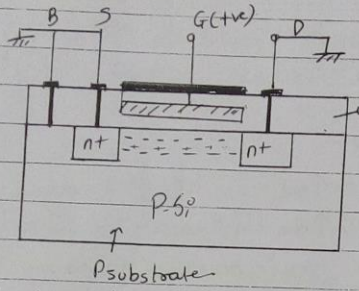
nMOS Tr with source & drain grounded:-



- To study the electrical behaviour of NMOS device, external bias are applied.
- $V_{SB} = 0$ (Initially)
- If a +ve is applied to the gate, an E-field is established which is directed ⊥rly through oxide.
- This field will induce -ve charges (minority carriers in P-Si) near surface.
- Since, P-Si contain very few e⁻s, the surface charges are the e⁻s obtnd from the source and drain & thus an inversion layer is formed.

  This inversion layer is formed only when certain gate voltage is applied.

  This value of gate voltage at which inversion of Si-SiO_2 surface takes place is known as threshold voltage V_T.
- As gate voltage (V_{GS}) ↑ses beyond V_T, the charges in inversion layer ↑se and the channel conductivity ↑ses.
- When a +ve potential is applied betn the drain & the source (V_{DS}), a current is produced in the channel betn source & drain.

  Thus, we see that the drain current is enhanced by the gate voltage & so the device is known as Enhancement type MOSFET.

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- When V_{DS} vtg is ↑sed further keeping V_{GS} constant ($V_{GS} > V_T$). Three cases occur depending on the value of V_{DS}.

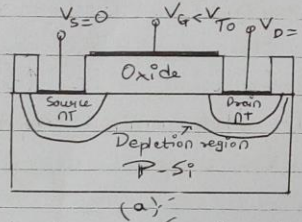
1. At $V_{DS} < V_{GS} - V_T$ an ↑se in V_{DS} causes the drain current I_D to ↑se linearly & the MOSFET behaves as resistance (Linear region)

2. At $V_{DS} = V_{GS} - V_T$, drop across the channel ↑ses in magnitude & hence the vtg across the oxide at drain side of channel ↓ses. As the potential difference is lowered, the field across the drain end of the oxide is reduced.
   So the no of inversion charges in this region is also reduced and at a point where $V_{DS} = V_{GS} - V_T$, the channel is said to be pinched off (devoid of charges at drain end of the channel)
   This results in a slow ↑se of I_D with ↑se in V_{DS}.)

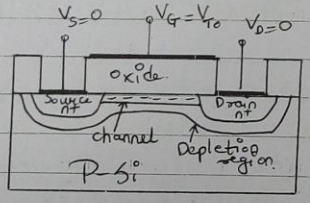
3. At $V_{DS} > V_{GS} - V_T$; a further ↑se in V_{DS} produces no change in drain current and the current saturation occur.
   This is the saturation region of device operation.

MOSFET Operation:-

We have seen that MOSFET consists of a MOS capacitor (P-Si gate, SiO_2 as dielectric P-Si); The carriers ie electrons in nMOST, enter the structure through Source (S) & leave through the drain (D) and are controlled by gate voltage.

a) 

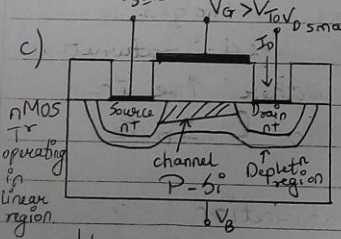
→ When a small +ve gate vtg ($0<V_{GS}<V_{TO}$) is applied, the gated region betn Source & the drain is depleted; ie holes get depleted from Semiconductor surface, & a depletion is formed.; ie no carrier flow can be observed in the channel. ie no channel exist and drain current is zero.

b) 

→ Here, when gate vtg V_G is ↑sed to a value V_{TO}, then surface inversion occurs. This results in formation of a channel betn Source & drain. Again no current flows as drain bias is kept at a zero potential.

* How? [One inversion layer is established on the surface, an n-type conducting channel forms betn S & D, which is capable of carrying the drain current]

[At $V_{DS}=0$, thermal equilibrium exists in inverted channel region & $I_D=0$].

c) 

nMOS Tr operating in linear region

→ As drain bias is ↑sed in small +ve value, current conduction takes place. ie. if small $V_{DS}>0$ is applied, a drain current I_D proportional to V_{DS} will flow from the S to D through the conducting channel.

• The inversion layer ie the channel, forms a continuous current path from the S to the D. This operation mode is called the 'Linear region'.

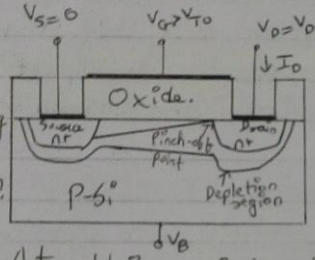
• Thus, in linear region operation, the channel region acts as a voltage-controlled resistor.

→ See that the vtg drop in the channel at Source-gate side is constant & at gate-drain side has changed due to application of drain bias (V_{DS} ↑ed)

• This results in the ↓se in no of carriers from the channel at gate-drain side & hence the shape of the channel & the depletion region also gets changed.

• Note that as the drain voltage is ↑ed, the inversion layer charge & the channel depth at Drain-end start to ↓se.

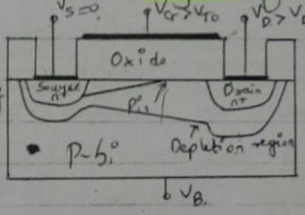
d) nMOS operating at the edge of saturatn.



• Keeping gate vtg constant, when $V_{DS} = V_{DSsat}$; the inversion charge at the drain end is reduced to zero, which is called pinch-off point.

At this point, the nMOSFET is said to be operating at the edge of saturation.

c) nMOS operating beyond saturatn



• Beyond the pinch-off pt; for $V_{DS} > V_{DSat}$; the channel near the drain vanishes & a depletion region is formed and it grows towards the source with ↑sing drain voltages.

This operation mode of nMOSFET is called 'saturation region', or saturation mode as further ↑se in drain voltage does not ↑se the I_D & I_D is said to saturate.

→ For a MOSFET, operating in saturation region, effective channel length is reduced as the inversion layer near drain vanishes, while channel-end voltage remains essentially constant ie V_{DSat}.

Note that the pinched-off (depleted) section of the channel absorbs most of the excess vtg drop ($V_{DS}-V_{DSat}$) & a high-field region forms betn channel-end & drain boundary. Thus, no channel exists in this region (betn channel end & drain) the e⁻s entering the shortened channel from the source are steered by this high electric field into the drain & drain current ↑ses but very slowly.

Also, the e⁻s arriving from the source to the channel-end are injected into drain-depletion region & are accelerated towards the drain in this high electric field.

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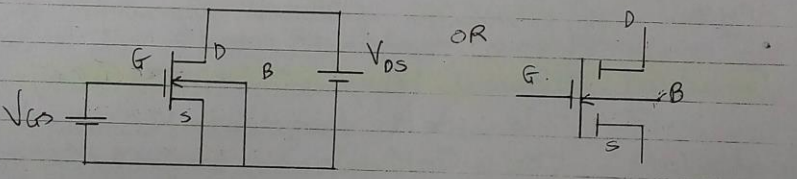
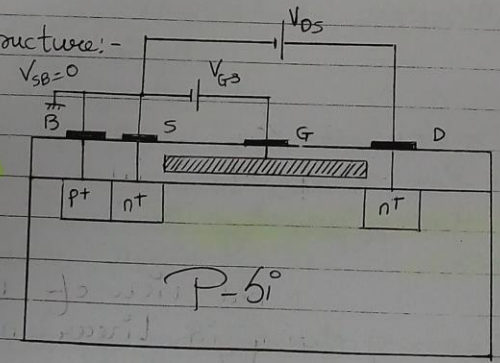
⇨ Working Analysis and Characteristics of NMOS E-Tr :-

↦ N-MOS Tr biasing



• Structure :-



• To study electrical behaviour of nMOS, external bias are applied
• Source & substrate are at gnd potential.

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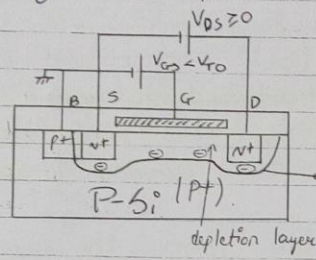
Case ①:-

If $V_{GS} < V_{TO}$ & $V_{DS} \geq 0$.

{ Cut-off region
$I_D \approx 0$ }



- Application of +ve gate vtg will create a depletion layer beneath the gate.
- Since there is no conducting path betn Drain & source ; $I_D = 0$
- The device is said to be in cut-off state.
- $I_D = 0$ because potential barrier due to depln charge density Q_{BO} C/cm² prevents the free e⁻ from entering into the depletion layer.

(To reduce no of steps, several approximatns to be made to simplify the problem)

- Gradual Channel Approximation (GCA):

GCA is used for establishing or to calculate the C-V characteristics of MOSFET.

→ Note, GCA has its limitations, esp for small-geometry MOSFETs.

⇨ Case ②:-

If $V_{GS} \geq V_{TO}$

; $0 \leq V_{DS} \leq V_{GS} - V_{TO}$

NMOS T^r operating in

→ Linear region.

- Consider the cross-sectional view of n-channel MOSFET or nMOS operating in Linear mode. Here, Source & substrate terminals are gnded. i.e $V_{SB} = 0$.

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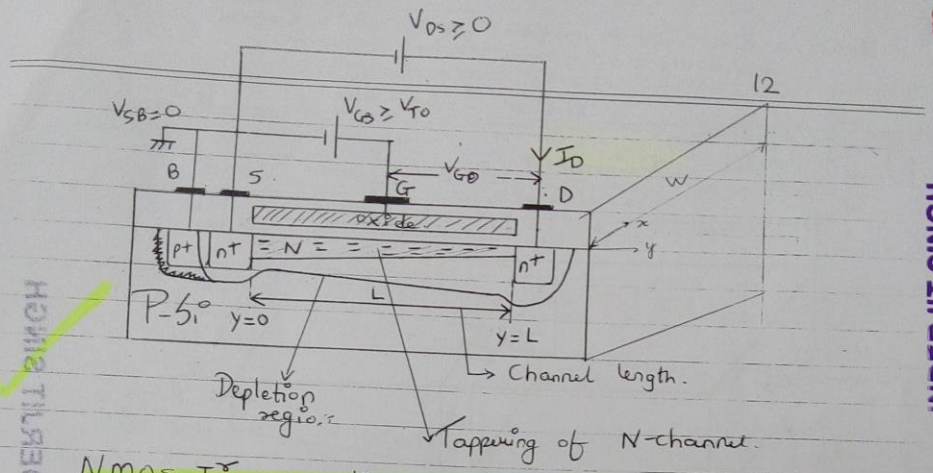

NMOS T^r operating in linear region.

∴ If $V_{GS} \geq V_{TO}$, an N-channel is induced betn drain & Source due to Surface inversion. ∴ there exists a conducting part betn Drain & Source.

- If $V_{DS}=0$, $I_D=0$, due to thermal equilibrium.
- If V_{DS} ↑ses, I_D ↑ses linearly with V_{DS}.
- If V_{GS} ↑ses, N channel conductivity ↑ses & hence I_D ↑ses. Therefore, in this region I_D is a function of external parameters V_{DS} & V_{GS}.
- $V_{GS} > V_{TO}$ since to create a conducting inversion layer betn Source & drain. ie $I_D = f(V_{GS}, V_{DS})$ This is linear region of device

⇨ Shape of N-channel:

From diagm,

$$V_{GD} = V_{GS} - V_{DS}$$

If V_{DS} ↑ses, V_{GD} ↓ses.

Hence, there is a tapering of N-channel towards Drain-side.

Note:- Surface potential at D-side is less than Surface potential S-side, thus N-channel thickness is a functn of Surface potential.

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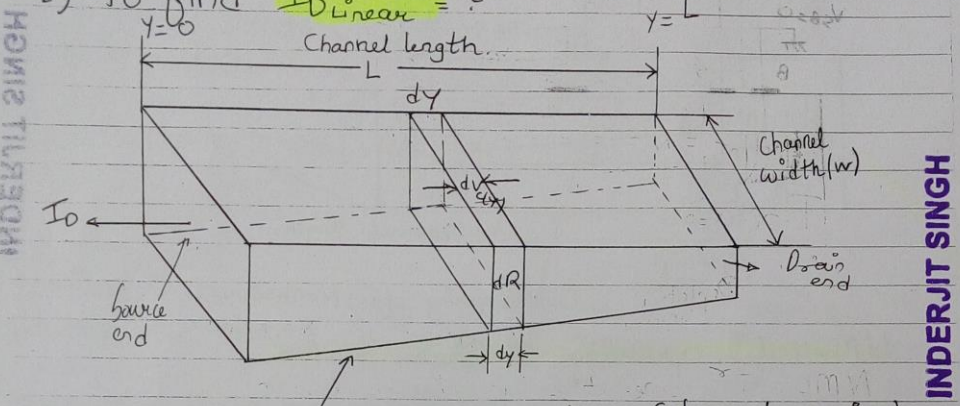
Here, x-directn ⊥r to surface, y-directn ∥el to surface
Channel vtg w.r.t source $= V_c(y)$.

b) To find $I_{D\,Linear} = ?$



Simplified Geometry of Surface inversion layer

- The channel voltage w.r.t source is $V_c(y)$
  Now assume that the threshold voltage V_{TO} is constant along entire channel region betn $y=0$ & $y=L$.
  {In reality, V_{TO} changes along the channel since channel vtg is not constant},

Let L - channel length
W - channel width.

Boundary condns for channel voltage V_c are

$$V_c(y=0) = 0$$
$$V_c(y=L) = V_{DS}$$

It is also assumed that entire channel region betn S & D is inverted ie,

$$V_{GS} \geq V_{TO}$$
$$V_{GD} = V_{GS} - V_{DS} \geq V_{TO}.$$

→ The channel current (drain current) I_D is due to e⁻s in channel region travelling from source to drain.

$$R = \frac{L}{\sigma A}$$

Let $Q_I(y)$ be the total mobile e^- charge in the surface inversion layer.

This charge can be expressed as a fn of V_{GS} & of channel vtg $V_c(y)$ as follows:-

$$Q_I(y) = -C_{ox}\left[\underbrace{(V_{GS} - V_{TO})}_{\text{due to excess gate vtg.}} - V_c(y)\right] \quad C/cm^2 \quad \rightarrow (A)$$

Consider an elementary resistance dR having length dy as shown in channel region.

Assuming that all mobile e-s in the inversion layer have a const surface mobility μ_n; the incremental resistance is

By defn,

$$dR = \frac{dy}{\sigma\, dA}$$

$$dR = \frac{-dy}{W.\mu_n Q_I(y)} \quad — (1)$$

where, $\mu_n = e^-$ mobility $\quad cm^2/V\text{-sec}.$
$(680\ cm^2/V\text{-se})$
$\rightarrow$ (e^- mobility is fun^n of geometry of device)

Here, I_D flows betn S & D region in y- direction.
Thus, I_D causes a p.d across dR.

$$\therefore\ dV_c(y) = I_D\, dR.$$

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$$dV_{c(y)} = -\frac{I_D\,dy}{W\mu_n Q_{I(y)}} \qquad \text{From } (1)$$

$$I_D\,dy = -W\mu_n Q_{I(y)}\,dV_{c(y)}$$

$$I_D\,dy = -W\mu_n C_{ox}\left[(V_{GS}-V_{TO}) - V_{c(y)}\right]dV_{c(y)}$$

From (A).

Integrate over the limits $y=0$ to $y=L$

$$\int_0^L I_D\,dy = W\mu_n C_{ox}\int_0^{V_{DS}}\left[(V_{GS}-V_{TO}) - V_{c(y)}\right]dV_{c(y)}$$

$$I_D \cdot L = W\mu_n \cdot C_{ox}\left[(V_{GS}-V_{TO})V_{DS} - \frac{V_{DS}^2}{2}\right]$$

$$I_D = \mu_n \cdot C_{ox}\left(\frac{W}{L}\right)\left[(V_{GS}-V_{TO})V_{DS} - \frac{V_{DS}^2}{2}\right]$$

$$I_D = K_n\left[(V_{GS}-V_{TO})V_{DS} - \frac{V_{DS}^2}{2}\right]$$

↳ let $\boxed{K_n' = \mu_n C_{ox}}$ (A/V^2)

↳ process transconductance parameter.

& $\mu_n C_{ox}\left(\frac{W}{L}\right) = K_n'\left(\frac{W}{L}\right) = K_n$

↳ Device gain

$$\therefore I_D = K_n\left[(V_{GS}-V_{TO})V_{DS} - \frac{V_{DS}^2}{2}\right]$$

$$\therefore \boxed{I_{D\,linear} = \frac{K_n}{2}\left[2(V_{GS}-V_{TO})V_{DS} - V_{DS}^2\right]}$$

↳ Valid only for Linear region

Thus, $I_D = f(V_{GS}, V_{DS})$

→ The ratio $\left(\frac{W}{L}\right)$ is one of most imp design parameters in MOS digital ckt design & is called as Aspect Ratio.

$$I_{D\,Linear} = \frac{K_n}{2}\left[2(V_{GS}-V_{TO})V_{DS} - V_{DS}^2\right] \rightarrow \text{✡ eq}^n$$

$K_n = K_n'\left(\frac{W}{L}\right) \rightarrow$ Device gain.

($K_n' \rightarrow \mu_n C_{ox}$)

→ Practical use of ✡ eq^n:-

* Tabulate

Let $K_n = 100\ \mu A/V^2$

$V_{TO} = 1V$

Reference

$V_{GS} = 3V$		$V_{GS} = 4V$		$V_{GS} = 5V$	
V_{DS}	I_D	V_{DS}	I_D	V_{DS}	I_D
0		0		0	
1		1		1	
2		2		2	
3		3		3	

· Plot graph of I_D Vs V_{DS}