Channel Length modulation

Same

Channel Length Modulation or Derivation for I_{Dsat} (NMOS)

Next, we will examine the mechanisms of channel pinch-off and current flow in saturation mode in more detail. Consider the inversion layer charge Q_I that represents the total mobile electron charge on the surface, given by (3.27). The inversion layer charge at the source end of the channel is

$$Q_I(y=0) = -C_{ox} \cdot (V_{GS} - V_{T0}) \tag{3.39}$$

and the inversion layer charge at the drain end of the channel is

$$Q_I(y=L) = -C_{ox} \cdot (V_{GS} - V_{T0} - V_{DS}) \tag{3.40}$$

Note that at the edge of saturation, i.e., when the drain-to-source voltage reaches V_{DSAT},

$$V_{DS} = V_{DSAT} = V_{GS} - V_{T0} \tag{3.41}$$

the inversion layer charge at the drain end becomes zero, according to (3.40). In reality, the channel charge does not become exactly equal to zero (remember that the GCA is just a simple approximation of the actual conditions in the channel), but it indeed becomes very small.

$$Q_I(y=L) = 0 \tag{3.42}$$

Thus, we can state that under the bias condition given in (3.41), the channel is *pinched-off* at the drain end, i.e., at $y = L$. The onset of the saturation mode operation in the MOSFET is signified by this pinch-off event. If the drain-to-source voltage V_{DS} is increased even further beyond the saturation edge so that $V_{DS} > V_{DSAT}$, an even larger portion of the channel becomes pinched-off.

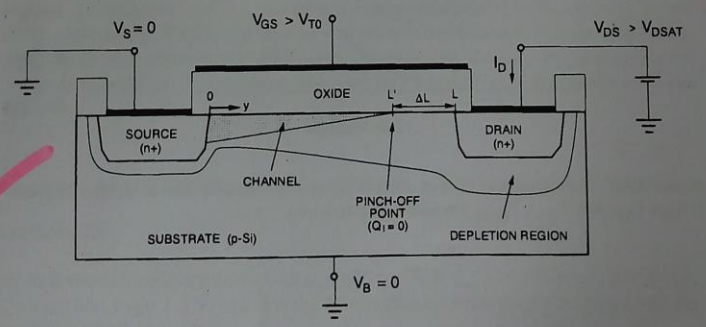


Figure 3.19. Channel length modulation in an n-channel MOSFET operation in saturation mode.

Consequently, the *effective channel length* (the length of the inversion layer where GCA is still valid) is reduced to

$$L' = L - \Delta L \tag{3.43}$$

where ΔL is the length of the channel segment with $Q_I = 0$ (Fig. 3.19). Hence, the pinch-off point moves from the drain end of the channel toward the source with increasing drain-to-source voltages. The remaining portion of the channel between the pinch-off point and the drain will be in depletion mode. Since $Q_I(y) = 0$ for $L' < y < L$, the channel voltage at the pinch-off point remains equal to V_{DSAT}, i.e.,

$$V_c(y = L') = V_{DSAT} \tag{3.44}$$

The electrons traveling from the source toward the drain traverse the inverted channel segment of length L', and then they are injected into the depletion region of length ΔL that separates the pinch-off point from the drain edge. As seen in Fig. 3.19, we can represent the inverted portion of the surface by a shortened channel, with a channel-end voltage of V_{DSAT}. The gradual channel approximation is valid in this region; thus, the channel current can be found using (3.38).

$$I_D(sat) = \frac{\mu_n \cdot C_{ox}}{2} \cdot \frac{W}{L'} \cdot (V_{GS} - V_{T0})^2 \tag{3.45}$$

Note that this current equation corresponds to a MOSFET with effective channel length L', operating in saturation. Thus, (3.45) accounts for the actual shortening of the channel, also called *channel length modulation*. Since $L' < L$, the saturation current calculated by using (3.45) will be larger than that found by using (3.38) under the same bias conditions. As L' decreases with increasing V_{DS}, the saturation mode current $I_D(sat)$ will also increase with V_{DS}. By approximating the effective channel length $L' = L - \Delta L$ as a function of the drain bias voltage, we can modify (3.45) to reflect this drain voltage dependence. First, rewrite the saturation current as follows:

$$I_D(sat) = \left(\frac{1}{1 - \frac{\Delta L}{L}} \right) \cdot \frac{\mu_n \cdot C_{ox}}{2} \cdot \frac{W}{L} \cdot (V_{GS} - V_{T0})^2 \tag{3.46}$$

The first term of this saturation current expression accounts for the channel modulation effect, while the rest of this expression is identical to (3.38). It can be shown that the channel length shortening ΔL is actually proportional to the square root of $(V_{DS} - V_{DSAT})$.

$$\Delta L \propto \sqrt{V_{DS} - V_{DSAT}} \tag{3.47}$$

To simplify the analysis even further, we will use the following empirical relation between ΔL and the drain-to-source voltage instead:

$$1 - \frac{\Delta L}{L} \approx 1 - \lambda \cdot V_{DS} \tag{3.48}$$

Here, λ is an empirical model parameter, and is called the *channel length modulation coefficient*. Assuming that $\lambda V_{DS} << 1$, the saturation current given in (3.45) can now be written as:

$$I_D(sat) = \frac{\mu_n \cdot C_{ox}}{2} \cdot \frac{W}{L} \cdot (V_{GS} - V_{T0})^2 \cdot (1 + \lambda \cdot V_{DS}) \tag{3.49}$$

This simple current equation prescribes a linear drain-bias dependence for the saturation current in MOS transistors, determined by the empirical parameter λ. Although this rough approximation does not accurately reflect the physical relationship between the channel length shortening ΔL and the drain bias, (3.49) can be used with sufficient confidence for most first-order hand calculations. The drain current versus drain-to-source voltage characteristics of an n-channel MOSFET, obtained by using (3.32) for the linear region and (3.49) for the saturation region, are shown in Fig. 3.20. The saturation mode current increases linearly with V_{DS} instead of remaining constant. The slope of the current-voltage curve in the saturation region is determined by the channel length modulation coefficient λ.

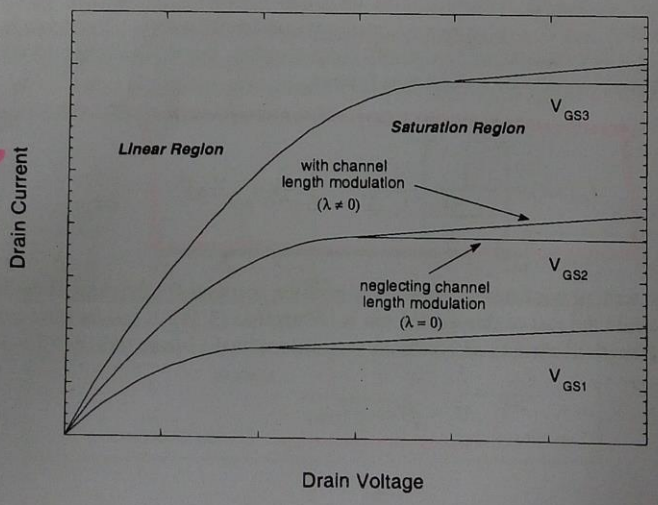


Figure 3.20. Current-voltage characteristics of an n-channel MOS transistor, including the channel length modulation effect.

Substrate Bias Effect

Note that the derivation of linear-mode and saturation-mode current-voltage characteristics in the previous pages has been done under the assumption that the substrate potential is equal to the source potential, i.e., $V_{SB} = 0$. Consequently, the zero-substrate bias threshold voltage V_{TO} has been used in the current equations. In many digital circuit applications, on the other hand, the source potential of an nMOS transistor can be larger than the substrate potential, which results in a positive source-to-substrate voltage $V_{SB} > 0$. In this case, the influence of the nonzero V_{SB} upon the current characteristics must be accounted for. Recall that the general expression (3.23) for the threshold voltage V_T already includes the substrate bias term and, hence, it reflects the influence of the nonzero source-to-substrate voltage upon the device characteristics.

$$V_T(V_{SB}) = V_{TO} + \gamma \cdot \left(\sqrt{|2\phi_F| + V_{SB}} - \sqrt{|2\phi_F|}\right) \tag{3.50}$$

We can simply replace the threshold voltage terms in linear-mode and saturation-mode current equations with the more general $V_T(V_{SB})$ term.

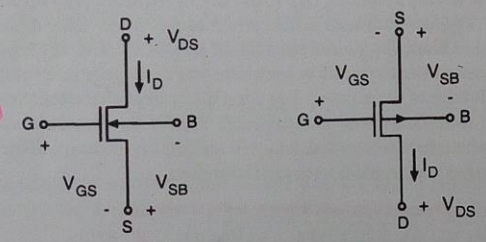
$$I_D(lin) = \frac{\mu_n \cdot C_{ox}}{2} \cdot \frac{W}{L} \cdot \left[2 \cdot \left(V_{GS} - V_T(V_{SB})\right) V_{DS} - V_{DS}^2\right] \tag{3.51}$$

$$I_D(sat) = \frac{\mu_n \cdot C_{ox}}{2} \cdot \frac{W}{L} \cdot \left(V_{GS} - V_T(V_{SB})\right)^2 \cdot (1 + \lambda \cdot V_{DS}) \tag{3.52}$$

In general, we will use only the term V_T instead of $V_T(V_{SB})$ to express the general (substrate-bias dependent) threshold voltage. As already demonstrated in Example 3.3, the substrate-bias effect can significantly change the value of the threshold voltage and, hence, the current capability of the MOSFET. With this modification, we finally arrive at a complete first-order characterization of the drain (channel) current as a nonlinear function of the terminal voltages.

$$I_D = f(V_{GS}, V_{DS}, V_{BS}) \tag{3.53}$$

In the following, we will repeat the current-voltage equations derived under the first-order gradual channel approximation (GCA), both for n-channel and for p-channel MOS transistors. Figure 3.21 shows the polarities of applied terminal voltages and the drain current directions. Note that the threshold voltage V_T and the terminal voltages V_{GS}, V_{DS}, and V_{SB} are all *negative* for the pMOS transistor. The parameter μ_p denotes the surface hole mobility in the pMOSFET.



n-channel MOSFET p-channel MOSFET

Figure 3.21. Terminal voltages and currents of the nMOS and the pMOS transistor.

Current-voltage equations of the n-channel MOSFET :

$$I_D = 0, \quad for \quad V_{GS} < V_T \tag{3.54}$$

$$I_D(lin) = \frac{\mu_n \cdot C_{ox}}{2} \cdot \frac{W}{L} \cdot \left[2 \cdot (V_{GS} - V_T) V_{DS} - V_{DS}^2\right] \quad for \quad V_{GS} \geq V_T \quad and \quad V_{DS} < V_{GS} - V_T \tag{3.55}$$

$$I_D(sat) = \frac{\mu_n \cdot C_{ox}}{2} \cdot \frac{W}{L} \cdot (V_{GS} - V_T)^2 \cdot (1 + \lambda \cdot V_{DS}) \quad for \quad V_{GS} \geq V_T \quad and \quad V_{DS} \geq V_{GS} - V_T \tag{3.56}$$

Current-voltage equations of the p-channel MOSFET :

$$I_D = 0, \quad for \quad V_{GS} > V_T \tag{3.57}$$

$$I_D(lin) = \frac{\mu_p \cdot C_{ox}}{2} \cdot \frac{W}{L} \cdot \left[2 \cdot (V_{GS} - V_T) V_{DS} - V_{DS}^2\right] \quad for \quad V_{GS} \leq V_T \quad and \quad V_{DS} > V_{GS} - V_T \tag{3.58}$$

$$I_D(sat) = \frac{\mu_p \cdot C_{ox}}{2} \cdot \frac{W}{L} \cdot (V_{GS} - V_T)^2 \cdot (1 + \lambda \cdot V_{DS}) \quad for \quad V_{GS} \leq V_T \quad and \quad V_{DS} \leq V_{GS} - V_T \tag{3.59}$$