Shri Vile Parle Kelvani Mandal's
Dwarkadas J. Sanghvi College of Engineering

Department of Electronics Engineering

Academic Year : 2015

MID-TERM TEST II

Subject : Electronic Devices

SE Sem III

Date : 17/10/2015

Marks : 20

Time : 1 hour

1] Q1. is compulsory

2] Attempt any two question's from remaining.

Q1

i) Draw small signal equivalent ckt for a JFET (1m)

ii) Draw EBD of MOSCAP with ptype body under positive gate voltage (1m)

iii) Draw EBD for a metal-ntype semiconductor ($\phi_m < \phi_s$) in thermal equilibrium and forward bias case. (2m)

iv) Draw ideal Low-frequency and high-frequency C-V curve for a MOSCAP with a ptype substrate (2m)

v) What are the types of MOSFETs ? Explain? (2m)

vi) Draw EBD for an n-Ge (narrow bandgap) and P-GaAs (wide-bandgap) heterojunction in thermal equilibrium? (2m)

OR

Q1

a) Calculate threshold voltage V_{TO} for a Poly Si gate N-channel MOSFET. (5m)
Given: Substrate doping is $10^{16}/cm^3$, poly Si gate doping is $2\times10^{20}/cm^3$, gate oxide thickness is 500 Å and no. of fixed oxide charges are $4\times10^{10}/cm^2$

b) Explain the working of N-channel JFET with the help of circuit diagram and its I-V characteristics. (5m)

P.T.O

$\boxed{Q2.}$ Consider a contact between tungsten and ntype Si doped to $N_d = 10^{16}\ cm^{-3}$ at $T = 300K$. (5m)

Find a) Schottky barrier height b) built-in potential barrier c) Max E-field for Zero-applied bias

Given: Metal work function for tungsten is 4.55V

Electron affinity is 4.01V, $N_c = 2.8 \times 10^{19}\ cm^{-3}$.

$\boxed{Q3.}$ Draw EBD of a MOSCAP in thermal-equilibrium for a ptype Si substrate. (5m)

i) How much voltage do we need to apply to make the bands flat.

ii) If a v. high -ve gate vtg is externally applied to this MOSCAP, which condition is achieved

iii) Draw EBD for case (ii).

$\boxed{Q4.}$ Explain the terms straddling, staggered and broken-gap w.r.t heterojunctions. Hence, explain concept of "2DEG" w.r.t ideal EBD of an nN GaAs - ALGaAs hetero-junction in thermal equilibrium. (5m)

$\boxed{Q5.}$ Draw EBD of a metal-ntype semiconductor junction for $\phi_m > \phi_s$. (5m)

a) before contact

b) after contact (in thermal equilibrium)

c) in forward bias

d) in reverse bias

Hence, justify in short why this contact is called a "rectifying contact or junction"

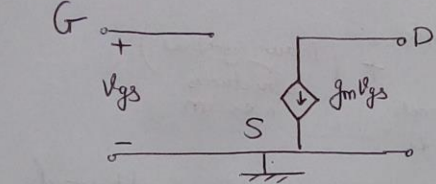
65

———x———

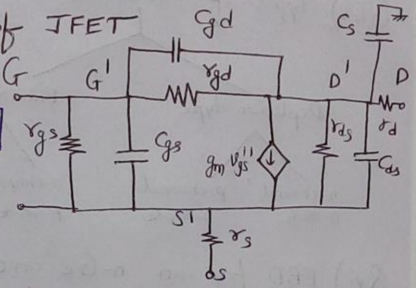
Pg 1

"ED TT2 Solutions"

Q1 i) Small-signal equivalent ckt of JFET

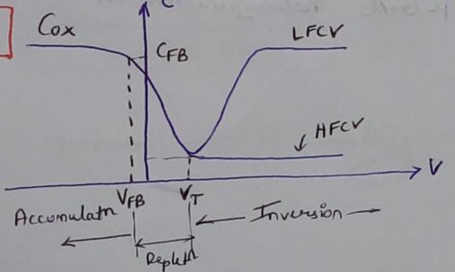


OR



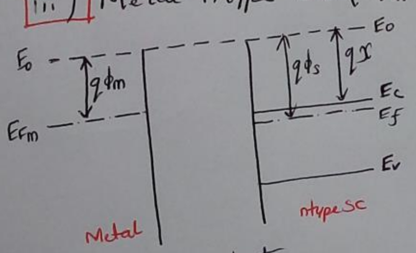
(1M)

iv)



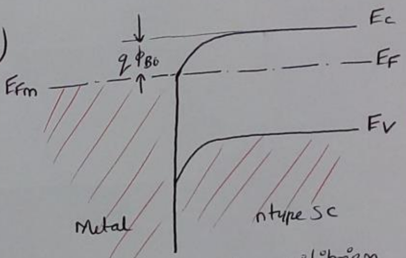
(1m)

iii) Metal-ntype SC ($\phi_m < \phi_s$)



before contact

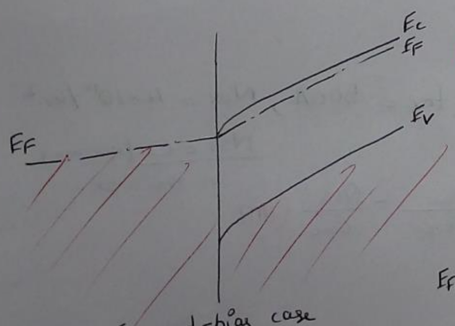
(Not asked in Q)



in thermal equilibrium

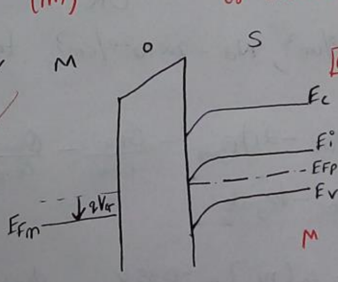
(1m)

ii) EBD of MOSCAP under the gate vtg (can be depletion or inversion) → both are correct!



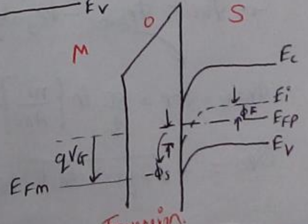
Forward-bias case

(1m)



Depletion

OR



Inversion.

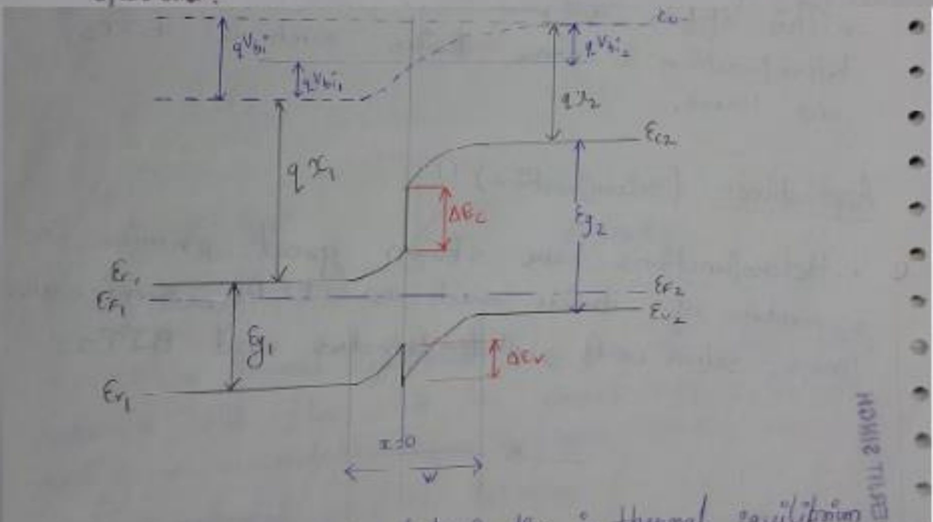
Q1. v) Types of MOSFETs

- Depletion type
  - n-channel D-mode
  - p-channel D-mode
- Enhancement type
  - n-channel E-mode
  - p-channel E-mode

(2m)

+ (Draw symbols or structures in exam)

Q. vi) EBD for an n-Ge and P-GaAs heterojunction in thermal equilibrium:



7.b) EBD of an nP heterojunction in thermal equilibrium

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OR

Q1. a)

$N_a = 10^{16}/cm^3$, $N_d = 2\times10^{20}/cm^3$, $t_{ox} = 500Å$, $N_{ox} = 4\times10^{10}/cm^2$

$\underline{N_{SS} = 0}$ (assume) $\therefore Q_{SS} = 0$

$V_{TO} = ?$

$V_{TO} = \phi_{GC} - 2\phi_{F(sub)} - \frac{Q_{BO}}{C_{ox}} - \frac{Q_{ox}}{C_{ox}} - \frac{Q_{SS}}{C_{ox}}$ (1m)

$\rightarrow \phi_{GC} = \phi_{F(sub)} - \phi_{F gate}$

$\phi_{F(sub)} = \phi_{FP} = \frac{KT}{q}\ln\left[\frac{n_i}{N_A}\right] = \underline{-0.35V}$, $\phi_{F(gate)} = \phi_{FN} = \frac{KT}{q}\ln\left[\frac{N_D}{n_i}\right] = \underline{0.6V}$

$\therefore \phi_{GC} = -0.35 - 0.6 = -0.95\,V$ (1m)

$Q_{BO} = -\sqrt{2q\epsilon_{Si}N_A|-2\phi_{F(sub)}|} = -48.17\times10^{-9}\ C/cm^2$ (1m)

Pg 2

$Q_{ox} = qN_{ox} = 1.6\times10^{-19} \times 4\times10^{10} = 6.4\times10^{-9}$ C/cm² (½ m)

$Q_{SS} = 0$

$C_{ox} = \frac{\epsilon_{ox}}{t_{ox}} = 70.3\times10^{-9}$ F/cm² (½ m)

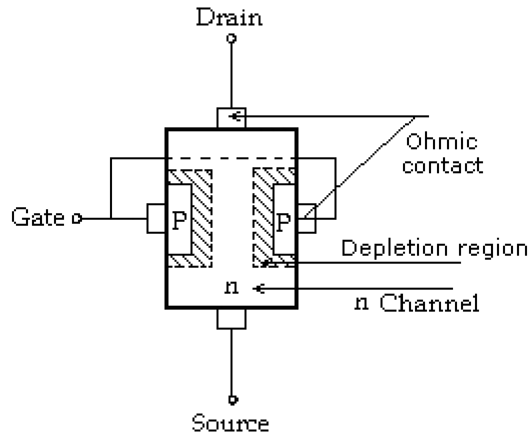
$$V_{TO} = \phi_{GC} - 2\phi_F - \frac{Q_{BO}}{C_{ox}} - \frac{Q_{ox}}{C_{ox}}$$

$$= -0.95 - 2(-0.35) - \left(-\frac{48.17}{70.3}\right) - \frac{6.4}{70.3}$$

$$\boxed{V_{TO} = 0.344 \text{ Volts}}$$ (1m)

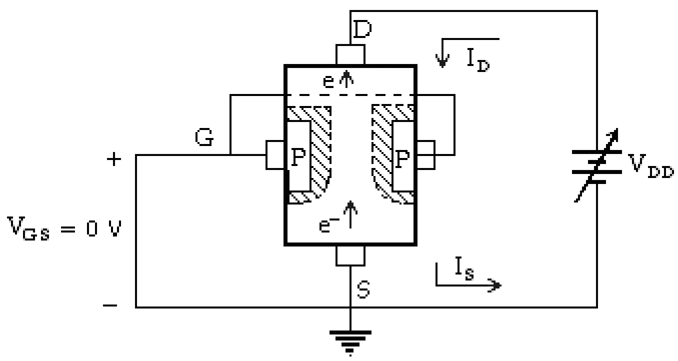
Q1.b) N-channel JFET working :- (5m)

N Channel JFET Working



The basic construction of n –channel FET is as shown in figure

1. <u>V_{GS} = 0_V , V_{DS} - Some +ve Value</u>:-



As shown in the figure the gate is directly connected to source to achieve V_{GS} = 0v , this is similar to no bias condition. The instant the voltage $V_{DD}(=V_{DS})$ is applied , the e^- will drawn to the drain terminal, causing I_D & I_S to flow (i-e. $I_D = I_S$). Under this condition the flow of charge is limited solely by Resistance of the n channel between drain & source.

It is important to note that the depletion region wider at the top of both p type of material. Since the upper terminal is more R .B. than the lower terminal (source - S).

As voltage V_{DS} is increased from 0 to few volts, the current will increase as determined by ohm's law. if still V_{DS} is increased & approaches a level referred as Vp, the depletion region will widen, causing a noticeable reduction in channel width. The reduced path of conduction causes the resistance to increase. The more the horizontal curve, the higher resistance.

If V_{DS} is increase to a level where it appears that the two depletion region would touch each other, the condition referred as 'pinch –off ' will result . The level of V_{DS} that establish this condition is called as 'pinch off voltage' (V_P). At V_P, I_D should be zero, but practically a small channel still exists & very high density current still flows through the channel.

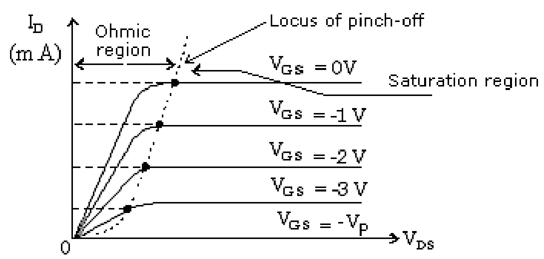
As V_{DS} is increased beyond V_P the saturation current will flow through the channel (I_{DSS}).

I_{DSS} – Drain to source current with short cut connection from source to Gate.

2. V_{GS} < 0V:-

If a –ve bias is applied between gate and source, the effect of the applied –ve bias V_{GS} is to establish depletion region similar to those obtained with V_{GS} = 0V but at lower level of V_{DS}.

As V_{GS} will become more & more –ve biased , the depletion layer pinch off occur at the less & less value of V_{DS} . Eventually, when $V_{GS} = - V_P$, will be sufficiently –ve to establish a saturation level , i.e. essentially 0 mA & for all practical purpose the device has been 'turned OFF.'



The region to the right of the pinch – off locus is typically employed in linear amplifiers (Amplifier with min. distortion at applied signal) is commonly referred as the constant current, saturation or linear amplification region.

Q2. Given: Tungsten – n-type Si contact

$N_d = 10^{16}\ cm^{-3}$, $\phi_m = 4.55V$, $\chi = 4.01V$

$N_c = 2.8\times10^{19}\ cm^{-3}$

→ a) Schottky Barrier htg: (ϕ_{B0})

$$\phi_{B0} = \phi_m - \chi = 4.55 - 4.01 = \underline{0.54V} \quad (1m)$$

b) Built-in potential barrier (V_{bi})

$$\phi_n = \frac{KT}{q}\ln\left(\frac{N_c}{N_d}\right) = 0.206V \quad (1m)$$

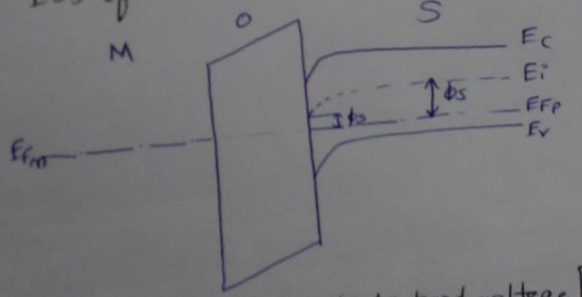
$$V_{bi} = \phi_{B0} - \phi_n = \underline{0.33V} \quad (1m)$$

c) Max E-field:

$$x_n = W = \left[\frac{2\epsilon_s V_{bi}}{qN_d}\right]^{1/2} = 0.207\times10^{-4}\ cm \quad (1m)$$

$$|E_{max}| = \frac{qN_d x_n}{\epsilon_s} = 3.2\times10^{4}\ V/cm \quad (1m)$$

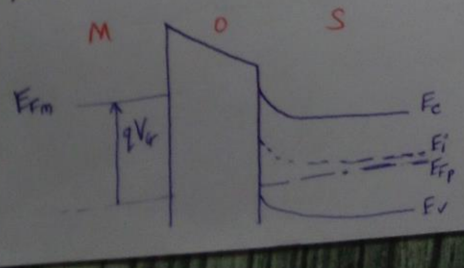
Q3. EBD of a MOSCAP in thermal-equilibrium (p type substrate) (2m)



i) We need to apply flat band voltage $\boxed{V_{FB} = \phi_{GC} - \frac{Q_{ox}}{C_{ox}}}$ (1m) to make bands flat.

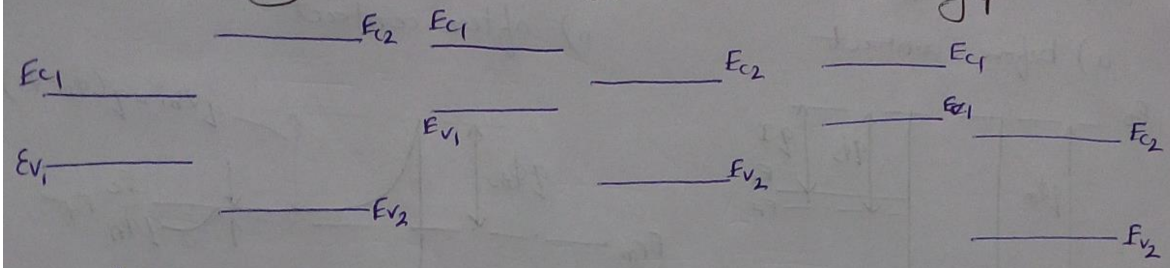
ii) Accumulation cond^n is achieved. (1m)

iii) (1m)



Pg no 3

Q4. Straddling Staggered Broken gap



"2DEG" concept w.r.t EBD of nN GaAs-AlGaAs

a) EBD of an nN GaAs-AlGaAs heterojunction in thermal equilibrium in shown in fig 5.a)

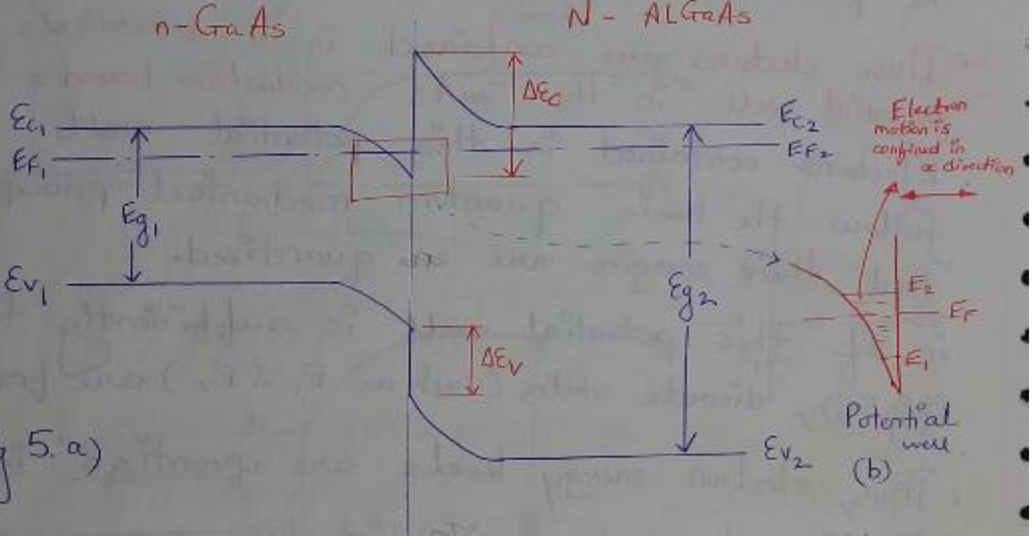


fig 5.a)

To explain an interesting property of an isotype hetero-junction, we will assume that GaAs is lightly doped, whereas AlGaAs is moderately to heavily doped.

To achieve thermal equilibrium, electron flow from the wide-band-gap material into the low-band gap GaAs.

This leads to the formation of an accumulation layer of electrons in the potential well adjacent to the interface. 14

- Thus the discontinuity in the conduction band (C.B) allows electrons to spill over from the AlGaAs into the GaAs, where they become trapped in the potential well.
- These electrons are confined in a narrow potential well in the GaAs conduction band.
- Electrons contained in this potential well follow the basic quantum mechanical principle that their energies are quantized.

ie If this potential well is sufficiently thin (fig 5b), discrete states (such as E_1 & E_2) are formed.

- Thus, electron energy levels are "quantized" in a direction ⊥r to the interface, whereas the electron's are free to move in the other two spatial directions.
- Such a behavior of electrons is referred to as "two-dimensional electron gas" or "2DEG"

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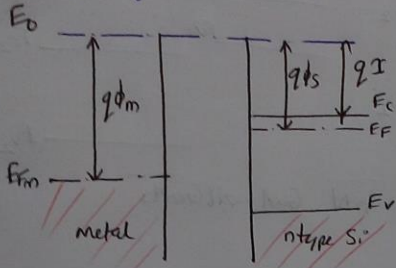
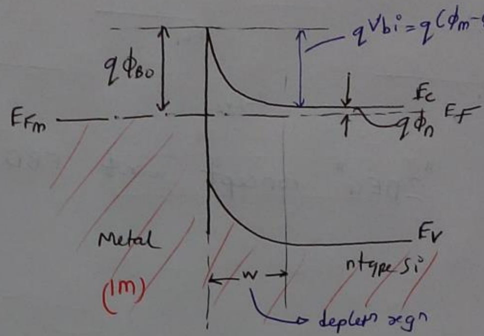
Q5. EBD of Metal-ntype Si contact for $\phi_m > \phi_s$

a) before contact



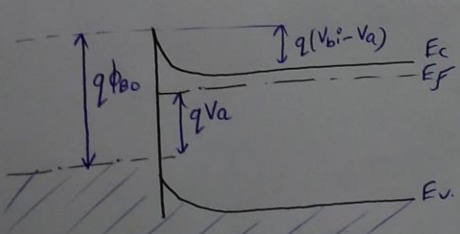
(1m)

b) after contact.



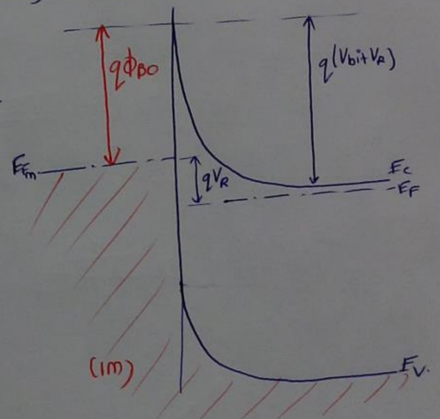
(1m)

c) in forward bias



(1m)

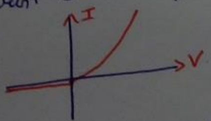
d) in reverse bias



(1m)

Justification: (1m)

- In Forward-bias, barrier seen by $\bar{e}$s in SC is reduced, so maj. carrier $\bar{e}$s flow more easily from SC into the metal.
- In R.B, reverse current is v. small, as barrier is large.



∴ Schottky barrier contact acts like a rectifying contact