D. J. SANGHVI COLLEGE OF ENGINEERING
DEPARTMENT OF ELECTRONICS ENGINEERING
EXC302: ELECTRONIC DEVICES SEM III
QUIZ 2 SET A SOLUTION

N.B. : **[Total Marks: 100]**

1) For every incorrect answer **50% marks** will be deducted.

2) While answering the numericals, writing formula is mandatory.

NAME: ______________________ **SAP ID:** ______________________

Given: $n_i = 1 \times 10^{10}/cm^3$, $\epsilon_s = 10^{-12} F/cm$, $\epsilon_{ox} = 3.97 \times 8.854 \times 10^{-14} F/cm$

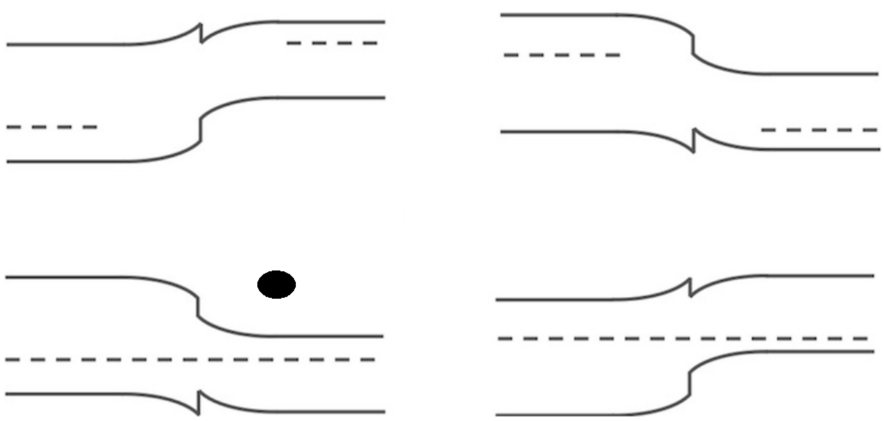
1. Consider a pn junction made from p-type Si (E_g=1.1eV) and n-type Ge (E_g=0.67eV). The conduction band offset ΔE_c=0.2eV (the conduction band steps down as you go from the higher bandgap material to the lower bandgap material).

a) What is the valence band offset ΔE_v ? **[01]**

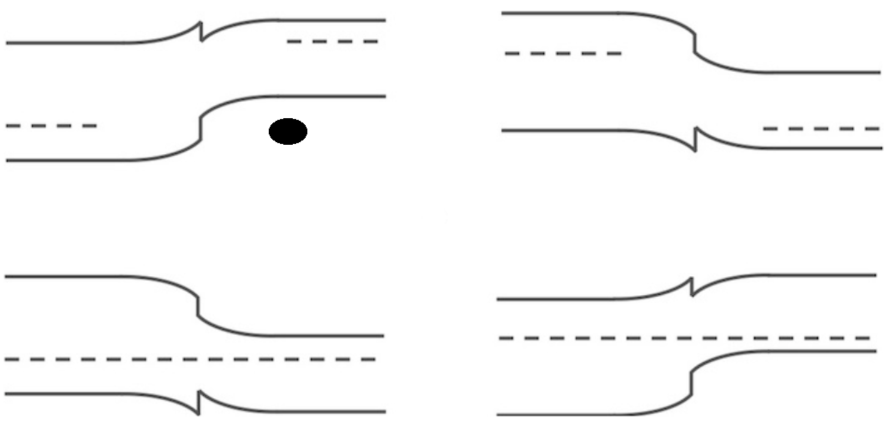
$\Delta E_c + \Delta E_v = 1.1 - 0.67 = 0.43$ eV

$\Delta E_v =$ **0.23 eV**

b) Click on the band structure that represents this device under equilibrium conditions? **[02]**

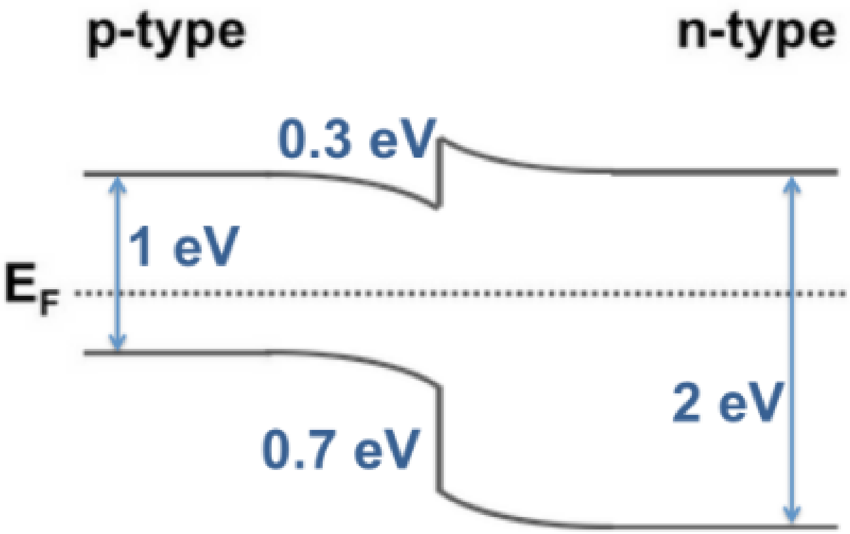


c) Click on the band structure that represents this device under forward bias? **[02]**

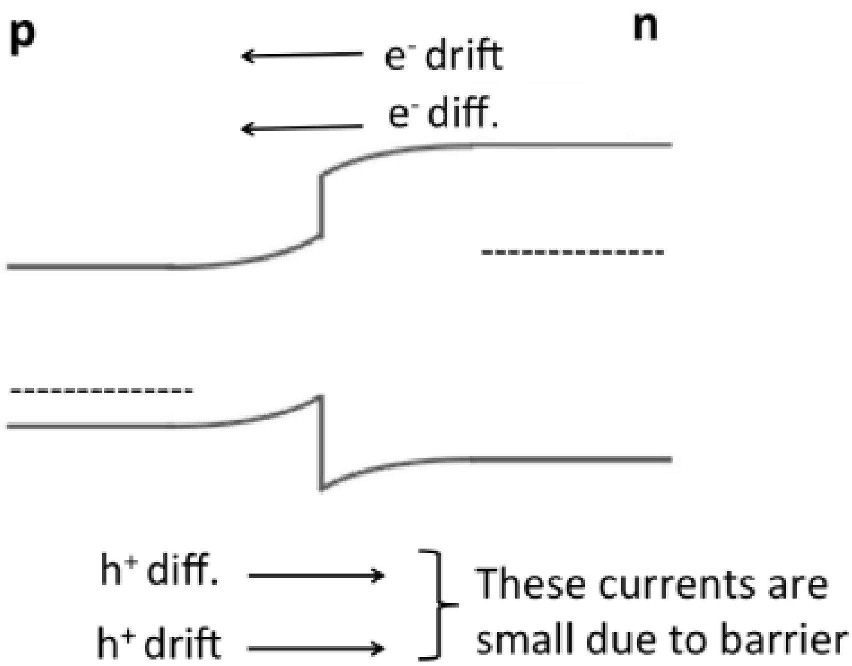


2. A has a band gap of 1eV and B has a band gap of 2eV. The band offset ΔE_c is 0.3eV. Assume that the pn junction is made from p-type A and n-type B.

I) Draw EBD of given pn heterojunction under equilibrium **[04]**



II) Draw EBD of given pn heterojunction under forward-bias **[04]**



III) Which of the following correctly describe the carrier currents across the pn junction's band structure in **forward-bias**.

Electron drift: **[02]**

a) The electrons drift from left to right (from A to B)

b) **The electrons drift from right to left (from B to A)**

c) As compared to a homojunction, the electron drift current is reduced due to the presence of a barrier

Electron diffusion: **[02]**

a) The electrons diffusion from left to right (from A to B)

b) **The electrons diffusion from right to left (from B to A)**

c) As compared to a homojunction, the electron diffusion current is reduced due to the presence of a barrier

Hole drift: **[02]**

a) The holes drift from left to right (from A to B)

b) The holes drift from right to left (from B to A)

c) **As compared to a homojunction, the hole drift current is reduced due to the presence of a barrier**

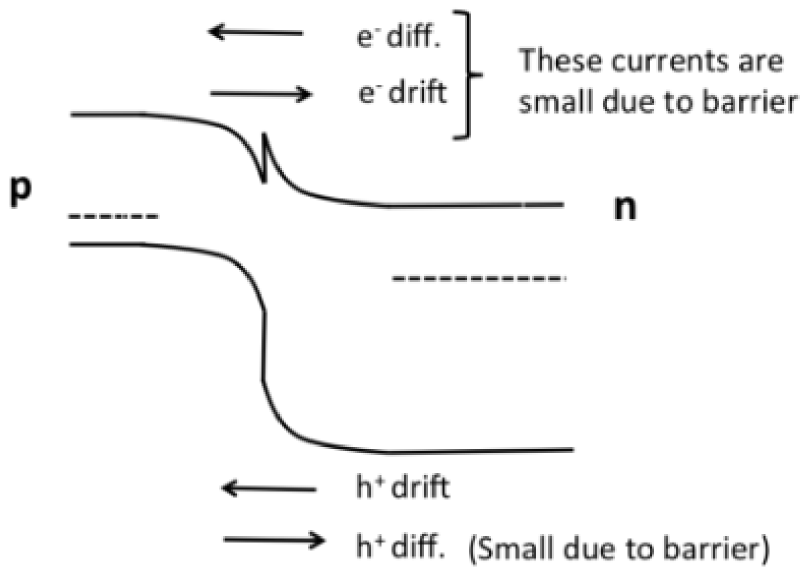
Hole diffusion: **[02]**

a) The holes diffusion from left to right (from A to B)

b) The holes diffusion from right to left (from B to A)

c) **As compared to a homojunction, the hole diffusion current is reduced due to the presence of a barrier**

IV) Draw EBD of given pn heterojunction under reverse-bias **[04]**



V) Which of the following correctly describe the carrier currents across the pn junction's band structure in **reverse-bias**.

Electron drift: **[02]**

a) **The electrons drift from left to right (from A to B)**

b) The electrons drift from right to left (from B to A)

c) **As compared to a homojunction, the electron drift current is reduced due to the presence of a barrier**

Electron diffusion: **[02]**

a) The electrons diffusion from left to right (from A to B)

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Hole diffusion: **[02]**

a) **The holes diffusion from left to right (from A to B)**

b) The holes diffusion from right to left (from B to A)

c) **As compared to a homojunction, the hole diffusion current is reduced due to the presence of a barrier**

3. A MOSCAP is biased so that majority carriers in the semiconductor pile up at the oxide-semiconductor interface is biased in which region **[02]**

   a) **Accumulation**

   b) Flat-band

   c) Inversion

   d) Depletion

4. A MOSCAP is biased so that minority carriers in the semiconductor pile up at the oxide-semiconductor interface is biased in which region **[02]**

   a) Accumulation

   b) Flat-band

   c) **Inversion**

   d) Depletion

5. The quantity ϕ_f is a critical parameter in MOS theory. What happens when the surface potential equals $|2\phi_f|$ **[02]**

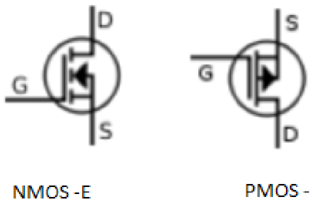
   a) The majority carrier concentration at the surface equals the majority carrier concentration in the bulk

   b) The majority carrier concentration at the surface equals the n_i intrinsic carrier concentration

   c) **The minority carrier concentration at the surface equals the majority carrier concentration in the bulk**

   d) None of the above

6. Draw symbol of Enhancement type NMOS and depletion type PMOS. **[01]**



7. An MOSCAP made using p-type substrate is in the accumulation mode. The dominant charge in the channel is due to presence of **[02]**

   a) **Holes**

   b) Electrons

   c) Positively charged ions

   d) Negatively charged ions

8. For an NMOS enhancement transistor, $K_n = 150\mu A/V^2, V_{TO} = 1.2$V, $V_{DS} = 5$V and $V_{GS} = 3.2$V.

   a) Determine in which operating region given device is operating. **[02]**

   Solution:

   Since $V_{GS} > V_T$ and $V_{DS} > (V_{GS} - V_T)$

   Given device is working in the **saturation** region

   b) Find the drain current I_D **[02]**

   $$I_D = \frac{K_n}{2}(V_{GS} - V_T)^2 = \mathbf{300}\mu A$$

9. In case of E-MOSFET, conduction occurs if and only if **[02]**

   a) $V_{GS} > V_T$ ✓

   b) $V_{GS} = V_T$

   c) $V_{GS} < V_T$

   d) $V_{GS} < 0$

10. For a p-type substrate, $N_A = 10^{16}/cm^3$, find fermi potential ϕ_{fp} **[02]**

$$\phi_{fp} = \frac{kT}{q} ln\left(\frac{n_i}{N_A}\right) = 0.026\, ln\left(\frac{1\times 10^{10}}{1\times 10^{16}}\right) = \textbf{-0.359}\text{ V}$$

11. For a MOSCAP, gate oxide thickness $t_{ox} = 100^o$A. Find gate oxide capacitance C_{ox} **[02]**

$$C_{ox} = \frac{\epsilon_{ox}}{t_{ox}} = \frac{3.97\times 8.854\times 10^{-14}}{100\times 10^{-8}} = \mathbf{351}\times 10^{-9}\frac{F}{cm^2}$$

12. For a n-channel MOSFET, gate oxide thickness $t_{ox} = 400^o$A, substrate doping concentration is $1.5\times10^{16}/cm^3$, density of fixed positively charged surface ions $N_{ox} = 5\times10^{10}/cm^2$. Calculate the following quantities for the given device:

a) Depth of the depletion region (x_d) **[02]**

$$x_d = \left[\frac{2\epsilon_s|-2\phi_{fn}|}{qN_A}\right]^{0.5} = \left[\frac{2\times 10^{-12}\times 0.36}{1.6\times 10^{-19}\times 1.5\times 10^{16}}\right]^{0.5} = \mathbf{25}\times 10^{-4}\ \mathbf{cm}$$

b) Fermi potential of the substrate (ϕ_{fp}) **[02]**

$$\phi_{fp} = \frac{kT}{q} ln\left(\frac{n_i}{N_A}\right) = 0.026\, ln\left(\frac{1\times 10^{10}}{1.5\times 10^{16}}\right) = \textbf{-0.36}\text{ V}$$

c) Depletion region charge density (Q_{BO}) **[02]**

$$Q_{BO} = -\left(2qN_A\epsilon_s|-2\phi_{fn}|\right)^{0.5}$$

$$Q_{BO} = -\left(2\times 1.6\times 10^{-19}\times 10^{-12}\times 1.5\times 10^{16}\times 2\times 0.36\right)^{0.5}$$

$$Q_{BO} = -\mathbf{60}\times 10^{-9}\frac{C}{cm^2}$$

d) Threshold voltage (V_{TO}) **[02]**

$$V_{TO} = \phi_{GC} - 2\phi_{fp} - \frac{Q_{BO}}{C_{ox}} - \frac{Q_{ox}}{C_{ox}} - \frac{Q_{ss}}{C_{ox}}$$

$$\phi_{GC} = \phi_{fp} - \phi_m = -0.36 - 0.55 = -0.91\text{ V}$$

$$C_{ox} = \frac{\epsilon_{ox}}{t_{ox}} = \frac{3.97\times 8.854\times 10^{-14}}{400\times 10^{-8}} = 86\times 10^{-9}\frac{F}{cm^2}$$

$$Q_{ox} = qN_{ox} = 1.6\times 10^{-19}\times 5\times 10^{10} = 8\times 10^{-9}\frac{C}{cm^2}$$

$$V_{TO} = -0.91 - 2\times -0.36 - \frac{-60\times 10^{-9}}{86\times 10^{-9}} - \frac{8\times 10^{-9}}{86\times 10^{-9}}$$

$$V_{TO} = \mathbf{0.4\ V}$$

e) Body factor (γ) **[02]**

$$\gamma = \frac{(2q\epsilon_s N_A)^{0.5}}{C_{ox}} = \mathbf{0.817}\ V^{0.5}$$

f) Flat band voltage (V_{FB}) **[02]**

$$V_{FB} = \phi_{GC} - \frac{Q_{ox}}{C_{ox}} = -0.91 - \frac{8 \times 10^{-9}}{86 \times 10^{-9}} = \mathbf{-1V}$$

13. A contact is made between tungsten and n-type Si semiconductor doped to $N_D = 10^{16} cm^3$ at T=300k. Metal work function for tungsten is $\phi_m = 4.55$V, electron affinity for semiconductor $\chi_s = 4.01$ eV and effective density of states $N_C = 2.8 \times 10^{19} cm^3$ Calculate the following quantities for the given device:

a) Ideal Schottky barrier height (ϕ_{BO}) **[02]**

$q\phi_{BO} = q\phi_m - \chi_s = 4.55 - 4.01 = 0.54\text{eV}$ or

$\phi_{BO} = \mathbf{0.54V}$

b) Built-in potential barrier (V_{bi}) **[02]**

$$\phi_n = \frac{kT}{q} ln\left[\frac{N_C}{N_D}\right] = 0.026\, ln\left[\frac{2.8 \times 10^{19}}{10^{16}}\right] = \mathbf{0.206V}$$

$$V_{bi} = \phi_{BO} - \phi_n = 0.54 - 0.206 = \mathbf{0.33\ V}$$

c) Space-charge width at zero-bias (x_n) **[02]**

$$x_n = \left[\frac{2\epsilon_s V_{bi}}{qN_D}\right]^{0.5} = \left[\frac{2 \times 11.7 \times 8.854 \times 10^{-14} \times 0.33}{1.6 \times 10^{-19} \times 10^{16}}\right]^{0.5} = \mathbf{0.207} \times 10^{-4}\ \mathbf{cm}$$

d) Maximum electric field strength (E_{max}) **[02]**

$$E_{max} = \frac{qN_D x_n}{\epsilon_s} = \frac{1.6 \times 10^{-19} \times 10^{16} \times 0.207 \times 10^{-4}}{11.7 \times 8.854 \times 10^{-14}} = \mathbf{32}\ \times 10^3 \frac{V}{cm}$$

14. Which of the following are true about Schottky diode: **[02]**

a) It is a high current diode used in high frequency and fast switching applications

b) It is formed by joining a doped semiconductor with a metal

c) Current conduction in schottky diode is only due to majority carriers

d) **All of the above**

15. The MOSFET differs from a JFET mainly because **[02]**

a) **The JFET has a p-n junction**

b) The MOSFET has two gates

c) of power ratings

d) None of the above

16. Drain of an n-channel MOSFET is shorted to gate so that $V_{GS} = V_{DS}$. The threshold voltage of MOSFET is 2V. If the drain current I_D is 2.5mA for $V_{GS} = 3$V, then for $V_{GS} = 5$V, I_D is **[04]**

    a) 4mA

    b) 9mA

    c) 15mA

    d) **22.5mA**

    Solution:

    $V_{GS} = V_{DS} \Rightarrow$ MOSFET is in saturation

    $\Rightarrow I_D = \frac{K_n}{2}(V_{GS} - V_T)^2$

    $\Rightarrow 2.5 \times 10^{-3} = \frac{K_n}{2}(3-2)^2$

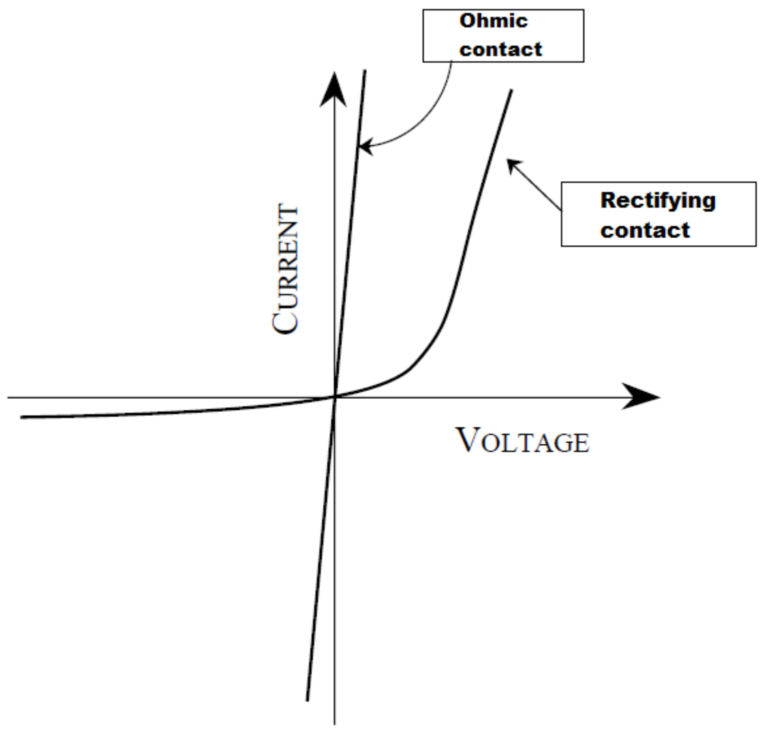
    $\Rightarrow k_n = 5 \times 10^{-3} \frac{A}{V^2}$

    Now, $\Rightarrow I_D = \frac{K_n}{2}(V_{GS} - V_T)^2$

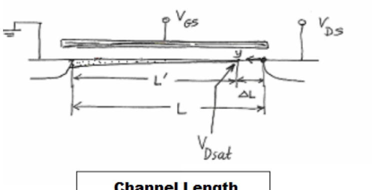
    $\Rightarrow I_D = \frac{5 \times 10^{-3}}{2}(5-2)^2$

    $\Rightarrow I_D = 22.5$ mA

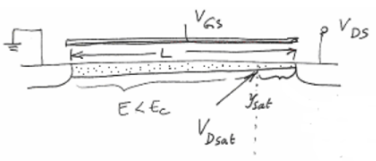
17. Identify the type of contacts from the I-V curve given below and write the answer inside the box provided. **[02]**



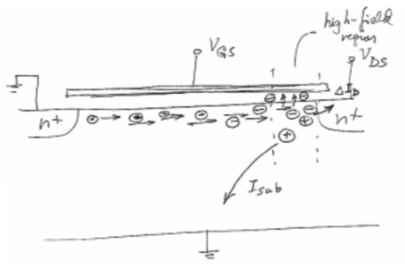
18. Identify the type of Short channel effects in MOSFET from diagrams given below and write the answers inside the box provided. **[03]**



Channel Length Modulation

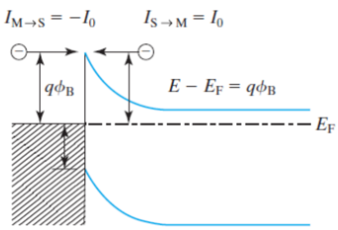


Velocity Saturation

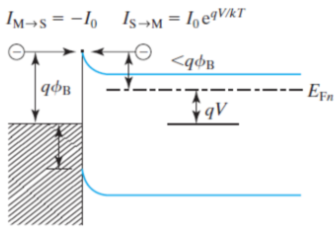


Hot carrier effect

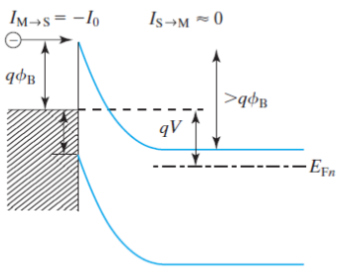
19. Identify the type of Metal semiconductor junction from EBD's given below and write the answers (i.e mention whether it is rectifying or ohmic contact, equilibrium or forward or it is reverse bias and whether n-type or p-type semiconductor) inside the box provided. **[06]**



Rectifying n type contact in equilibrium



Rectifying n type contact in forward bias

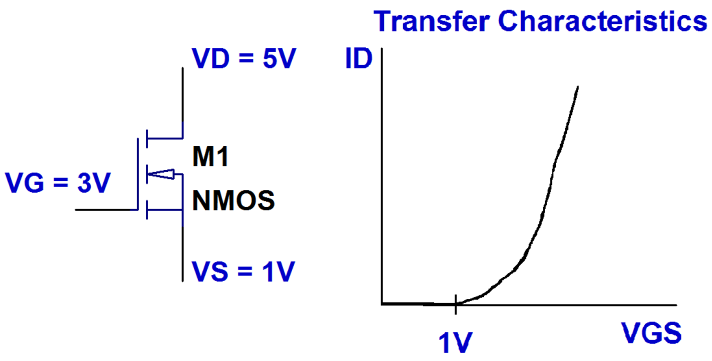


Rectifying n type contact in reverse bias

20. For an n-channel MOSFET, its transfer characteristics is shown in the figure below, the threshold voltage is **[04]**

a) 1V and the device is in active region

b) -1V and the device is in saturation region



c) **1V and the device is in saturation region**

d) -1V and the device is in active region

21. MOSFET can be used as a **[02]**
    a) Current controlled capacitor
    b) **Voltage controlled capacitor**
    c) Current controlled inductor
    d) Voltage controlled inductor

22. Consider the following two statements about the internal conditions in an n-channel MOSFET operating in the active region **[02]**
    S1 : The inversion charge decreases from source to drain
    S2 : The channel potential increases from source to drain
    Which of the following is correct ?
    a) Only S2 is true
    b) Both S1 and S2 are false
    c) **Both S1 and S2 are true; but S2 is not a reason for S1**
    d) Both S1 and S2 are true; but S2 is a reason for S1

23. Consider the following statements S1 and S2 **[02]**
    S1: V_T of a MOS capacitor decreases with increase in gate oxide thickness
    S2: V_T of a MOS capacitor decreases with increase in substrate doping concentration
    Which of the following is correct ?
    a) S1 is false and S2 is true
    b) **Both S1 and S2 are false**
    c) Both S1 and S2 are true
    d) S1 is true and S2 is false

    Explanation: If we increase the gate oxide thickness, then it becomes difficult to induce charges in channel so, V_T increases when we increase gate oxide thickness. Hence, S1 is false.

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