D. J. SANGHVI COLLEGE OF ENGINEERING
DEPARTMENT OF ELECTRONICS ENGINEERING
ELX302: ELECTRONIC DEVICES AND CIRCUITS 1 SEM III
ASSIGNMENT 01

26^{th} **August, 2017** **[Total Marks: 50]**

1. **Assume any suitable data if necessary**
2. **Read the questions carefully before attempting**
3. **Questions to be attempted by B1 batch : 01,07,08,12,13,16,17**
4. **Questions to be attempted by B2 batch : 02,07,09,11,15,16,18**
5. **Questions to be attempted by B3 batch : 01,03,05,08,15,16,19**
6. **Questions to be attempted by B4 batch (excluding diploma) : 03,04,06,11,14,16,20**

1. Draw Energy band diagram of pn junction under **[05]**
   a) Zero bias
   b) Forward bias
   c) Reverse bias

2. For a Si pn junction at T=300K, acceptor dopant and donor dopant have equal concentration of $10^{17}/cm^3$, $D_n = 25cm^2/s$, $D_p = 15cm^2/s$, $\tau_p = \tau_n = 50ns$, Area $=10^{-4}/cm^2$. Find the value of forward current for the forward-bias of 0.7V. **[05]**

3. A Si pn junction has $V_{bi} = 0.65V$ and acceptor concentration on p-side is 100 times greater than donor concentration on n-side. Find the width of depletion region and value of depletion capacitance per unit area when a reverse bias voltage of 10V is applied across it. **[05]**

4. Justify why the space charge width increases with reverse-bias voltage in a pn junction diode ? **[05]**

5. Derive the expression of built-in potential V_{bi} for a pn junction under zero-bias and hence calculate V_{bi} at T=300 K for $N_D = 10^{15}/cm^3$ and $N_D = 10^{15}/cm^3$. **[05]**

6. A Si pn junction at T=300K has doping profile shown below in figure 1: Estimate the following: **[05]**
   i) Built-in potential
   ii) x_n and x_p at zero bias
   iii) Sketch E-field Vs distance for the given situation.

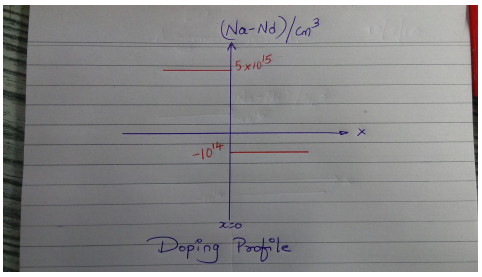

Figure 1: Question 6

7. An abrupt PN junction has dopant concentration of $N_D = 2 \times 10^{16}/cm^3$ and $N_A = 2 \times 10^{15}/cm^3$ at T =300 K. Calculate: **[05]**

   a) Built-in potential V_{bi}

   b) W at $V_R = 0$ and $V_R = 8$ V

   c) E_{max} at $V_R = 0$ and $V_R = 8$ V

8. Discuss the effects of temperature change on forward and reverse biased pn junctions. **[05]**

9. Write the ideal diode equation (or Shockley equation) for junction current in terms of junction voltage and other quantities. Define each quantity in the equation. From the Shockley equation for junction current, derive the junction voltage equation. **[05]**

10. For diodes, define forward voltage drop, maximum forward current, dynamic resistance, reverse saturation current, and reverse breakdown voltage. **[05]**

11. Explain the purpose of a dc load line. Write the equation for drawing a dc load line for a series circuit consisting of a supple voltage V_1, a resistor R_1 and a diode D_1. Next, define the Q-point in the circuit described above, and explain how it is related to the diode characteristics and the dc load line. **[05]**

12. Explain the origins of depletion layer capacitance and diffusion capacitance, and discuss the importance of each. **[05]**

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13. Design a clamper to perform the function indicated in figure 2. **[05]**

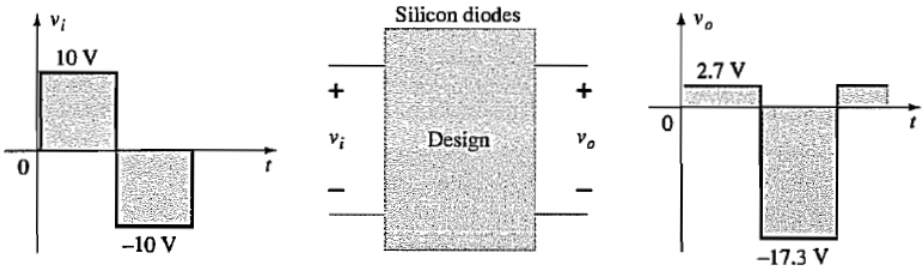

Figure 2: Question 13

14. Identify the circuit given in figure 3 and draw output waveform with proper voltage levels. **[05]**

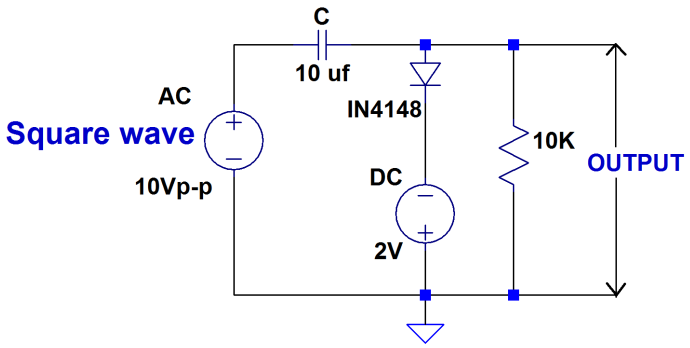

Figure 3: Question 14

15. Explain the difference between between clipping and clamping circuits. A positive voltage clamping circuit and a positive shunt clipping circuit each have a $\pm 12V$ square wave input. Sketch the output waveform from each circuit. **[05]**

16. For the circuits given below in figure 4, $V_m = 5V$, use SEQUEL or LT-spice to estimate the output voltage V_{out} vs time waveforms, and verify your answer with theoretical analysis using **[20]**

    a) Constant voltage model

    b) Sketch transfer characteristics (curve of V_{in} vs V_{out}) of all circuits.

    (use Sequel to verify your answer)

    NOTE: Attach the plots from simulation tool mentioned above along with your answer.

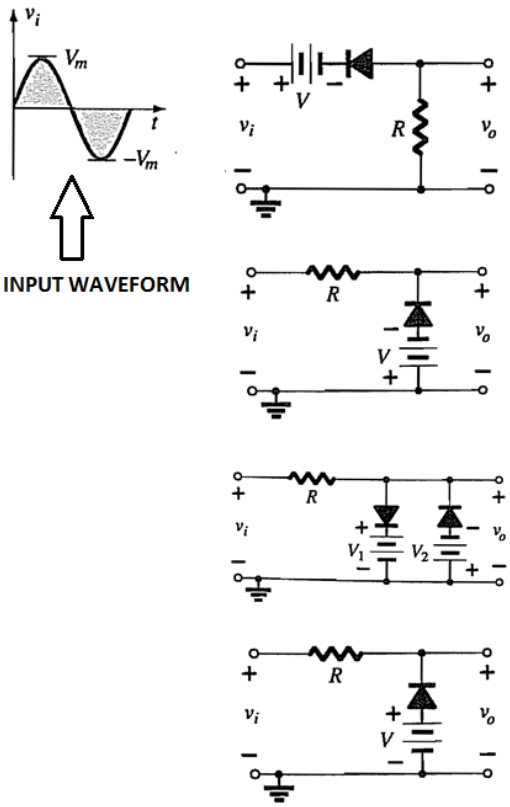

Figure 4: Question 16

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17. Explain the working of Zener as voltage regulator w.r.t **[05]**

    a) Source variations

    b) Load variations

18. Determine the minimum and maximum input voltages that can be regulator by zener whose ratings are $V_z = 5.6V, Iz_{min} = 2mA, Iz_{max} = 10mA$ and load resistor of value $R_L = 1k\Omega$. Also calculate the range of load current over which the output voltage remains constant. **[05]**

19. For the Zener diode network of figure 5, determine V_L, V_R, I_z and P_z **[05]**

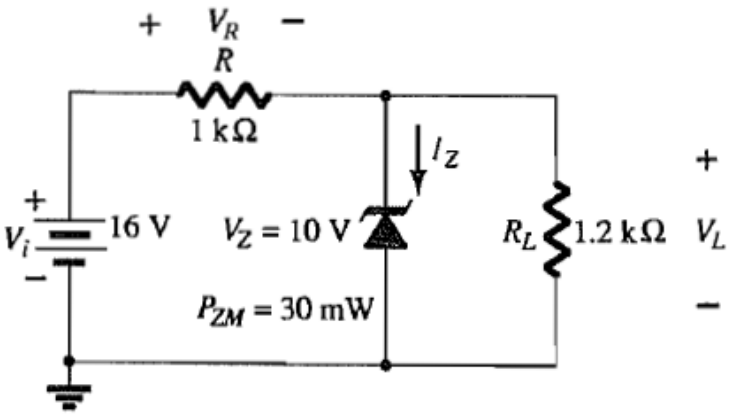

Figure 5: Question 19

20. Predict what will be the output for the circuit given in the figure 6 **[05]**

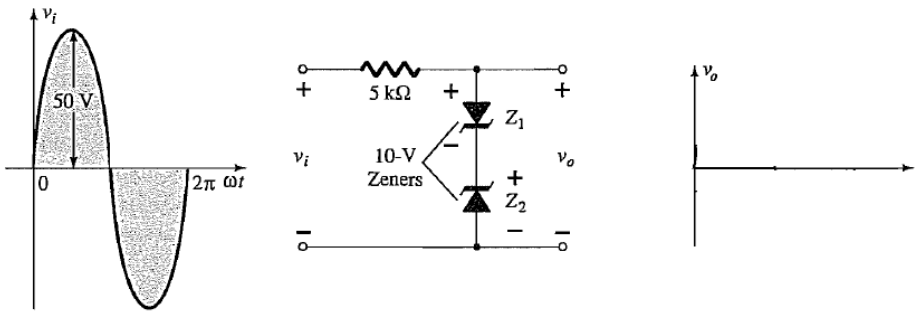

Figure 6: Question 20

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