D. J. SANGHVI COLLEGE OF ENGINEERING
DEPARTMENT OF ELECTRONICS ENGINEERING
ELX302: ELECTRONIC DEVICES AND CIRCUITS 1 SEM III
ASSIGNMENT 03

10^{th} **October, 2017** **[Total Marks: 80]**

1. **Assume any suitable data if necessary**
2. **Read the questions carefully before attempting**
3. **Questions to be attempted by B1 batch : 01,02,05,08,14,15,17,18**
4. **Questions to be attempted by B2 batch : 01,03,04,09,14,16,17,18**
5. **Questions to be attempted by B3 batch : 01,06,10,11,14,15,16,18**
6. **Questions to be attempted by B4 batch : 01,07,12,13,14,16,17,18**
7. **Date of submission: 14-10-2017**
8. **Hint: One can verify answers in LT Spice only for E- type MOSFETs**

1. Consider the figure 1

   ✠ Input to amplifier is 20mV peak to peak voltage, with 1KHz frequency

   i) What type of circuit is this **[1]**

   ii) Find k_n **[1]**

   iii) Calculate the value of V_{GSQ} **[1]**

   iv) Calculate the value of I_{DQ} **[1]**

   v) Sketch the small signal AC equivalent of the figure 1 **[1]**

   vi) Calculate the value of g_m **[1]**

   vii) Find r_d **[1]**

   viii) Find the input impedance Z_i of the circuit **[1]**

   ix) Find the output impedance Z_o of the circuit **[1]**

   x) Calculate the voltage gain of the circuit **[1]**

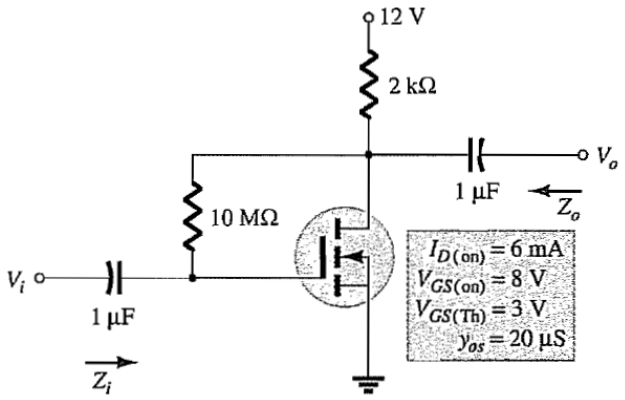

Figure 1: Question 1

2. Draw circuit diagram of common-source amplifier with voltage divider bias with unbypassed source resistance R_S using n-channel E-MOSFET. Derive the expression for voltage gain, input resistance and output resistance. **[10]**

3. For the given circuit, find V_{GSQ}, I_{DQ} and voltage gain A_V with C_S and without C_S Given: $V_T = 1V, k_n = 1mA/V^2$ **[10]**

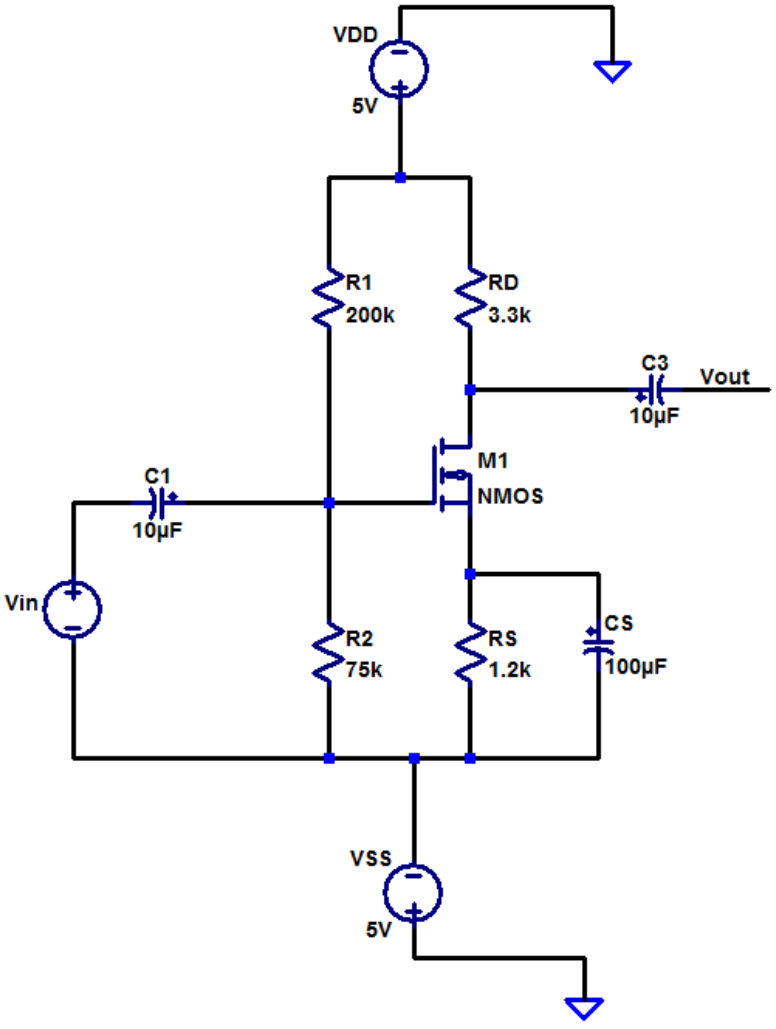

Figure 2: Question 3

4. Draw circuit diagram of common-source amplifier with voltage divider bias with C_S using n-channel E-MOSFET. Derive the expression for voltage gain, input resistance and output resistance. **[10]**

5. Determine V_o if $y_{os} = 20\mu S$

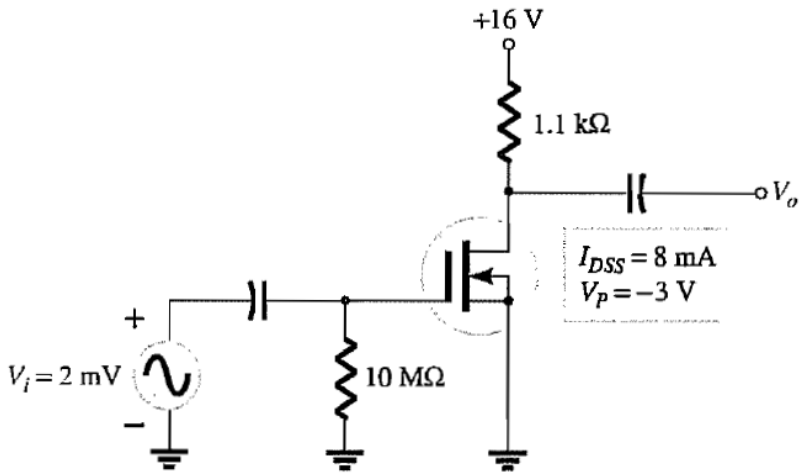

Figure 3: Question 5

6. What are different biasing circuits for E-MOSFET. Explain drain-feedback bias in detail. **[10]**

7. What are different biasing circuits for D-MOSFET. Explain voltage divider bias in detail. **[10]**

8. For the circuit shown find A_V, R_i and R_o **[10]**
   Given: $V_{GS(th)} = 3V, \quad I_{D(on)} = 5mA, \quad V_{GS(on)} = 6V, \quad r_d = 80K$

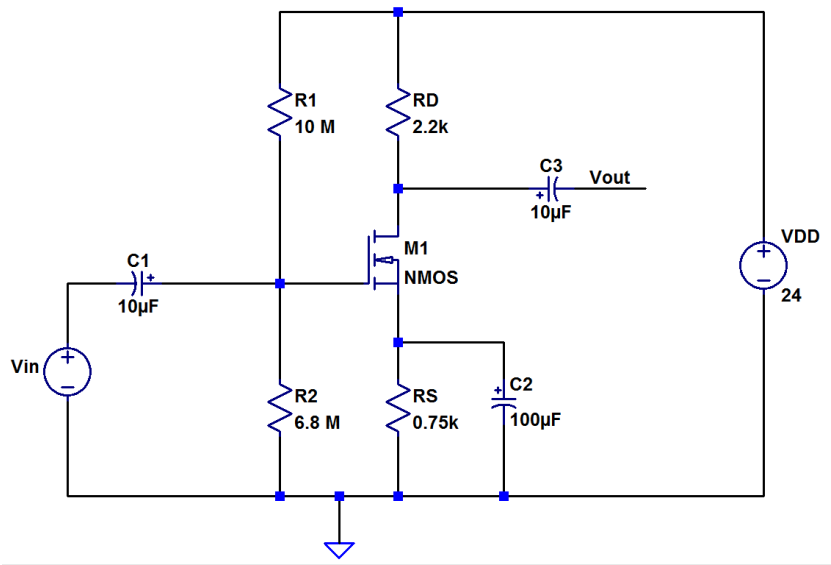

Figure 4: Question 8

9. Compare D-MOSFET and E-MOSFET considering construction and characteristics. **[10]**

10. Draw circuit diagram of common-source amplifier with voltage divider bias with unbypassed source resistance R_S using D-MOSFET. Derive the expression for voltage gain, input resistance and output resistance **[10]**

11. For the circuit shown find A_V, R_i and R_o **[10]**
Given: $V_{GS(th)} = 3V, \quad K = 0.4 \times 10^{-3}, \quad r_d = 80K\Omega$

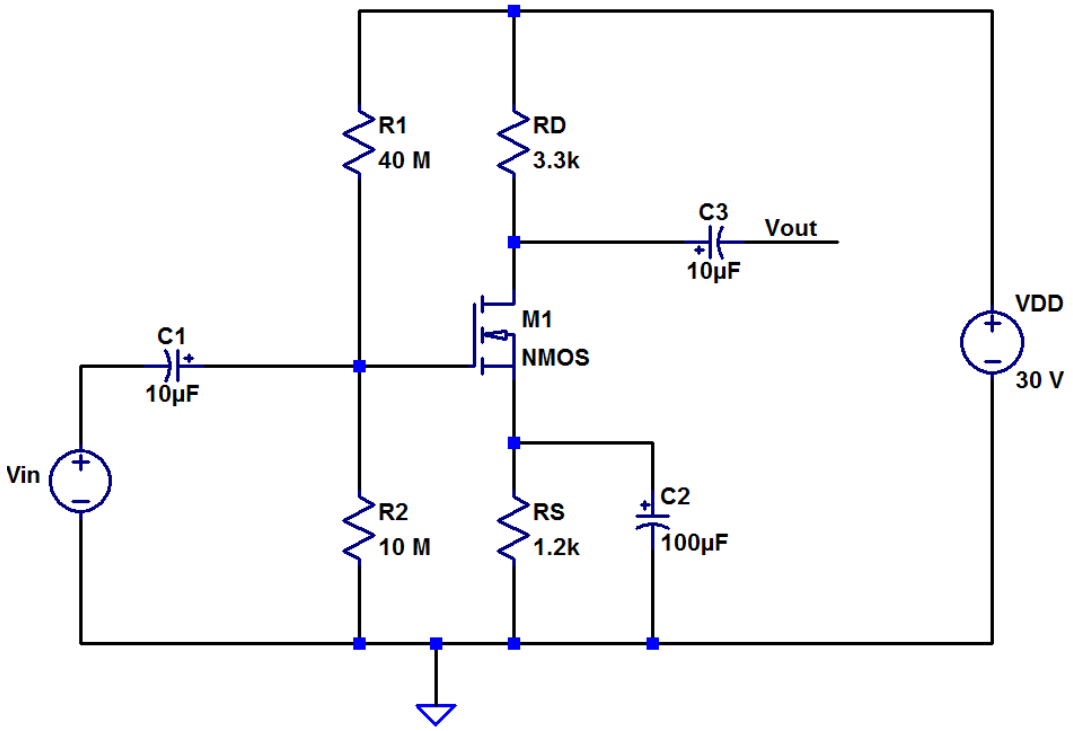

Figure 5: Question 11

12. Draw circuit diagram of common-drain amplifier using MOSFET. Derive the expression for voltage gain, input resistance and output resistance. **[10]**

13. Draw circuit diagram of common-gate amplifier using MOSFET. Derive the expression for voltage gain, input resistance and output resistance. **[10]**

14. Design an N-channel Enhancement type MOSFET using voltage-divider biasing for the following specifications: **[10]**

$I_{DQ} = 5mA$, $V_{DSQ} = 5V$

MOSFET parameters given are: $K_n = 20mA/V^2$, $V_{TN} = 1V$

15. Determine Z_i, Z_o and A_v if $r_d = 60K\Omega$ **[10]**

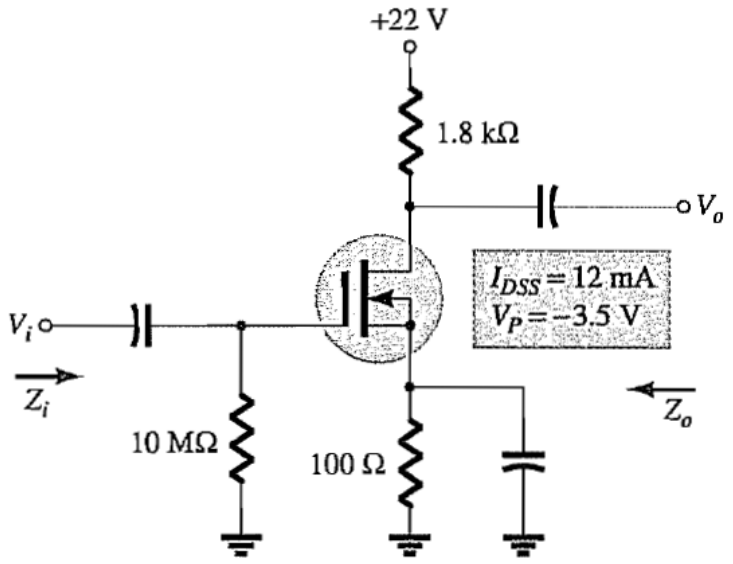

Figure 6: Question 15

16. Determine Z_i, Z_o and A_v **[10]**

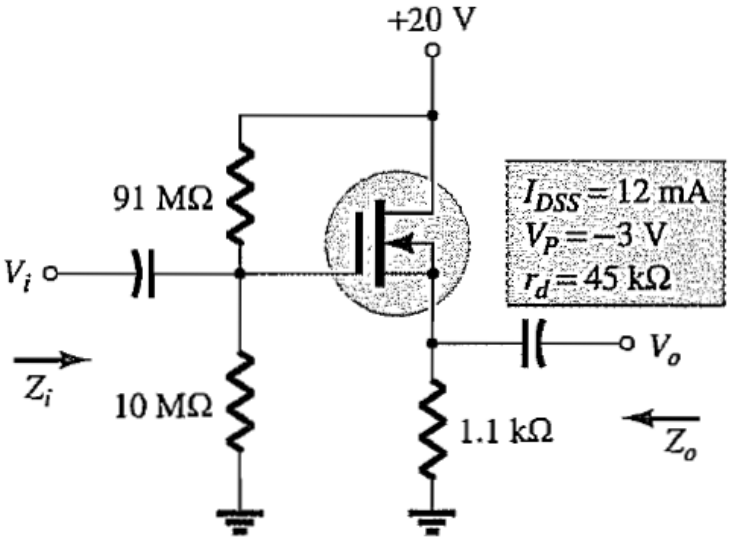

Figure 7: Question 16

17. For the NMOS common-source amplifier, the transistor parameters are: **[10]**

MOSFET parameters given are: $K_n = 1mA/V^2$, $V_{TN} = 0.8V$ and $\lambda = 0$

The circuit parameters are: $V_{DD} = 5V, R_S = 1K\Omega, R_D = 4K\Omega, R_1 = 225K\Omega,$ $R_2 = 175K\Omega$

a) Calculate the quiescent values I_{DQ} and V_{DSQ}

b) Determine the small- signal voltage gain for $R_L = \infty$

c) Determine the value of R_L that will reduce the small-signal voltage gain to 75 % of the value found in part (b)

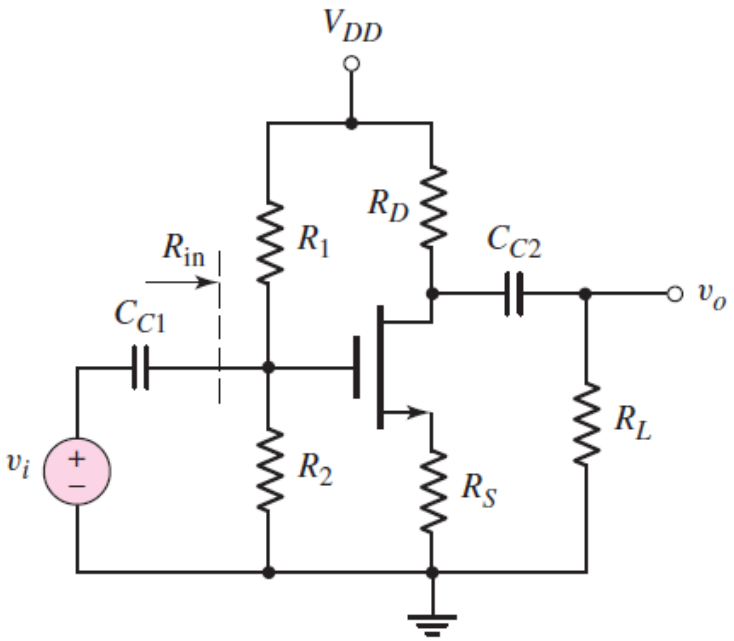

Figure 8: Question 17

18. Compare CS, CG and CD configuration using NMOS-E type w.r.t following parameters: **[10]**

i) Input impedance

ii) Circuit diagram

iii) Output impedance

iv) Voltage gain

v) Phase shift between input and output

vi) Application

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