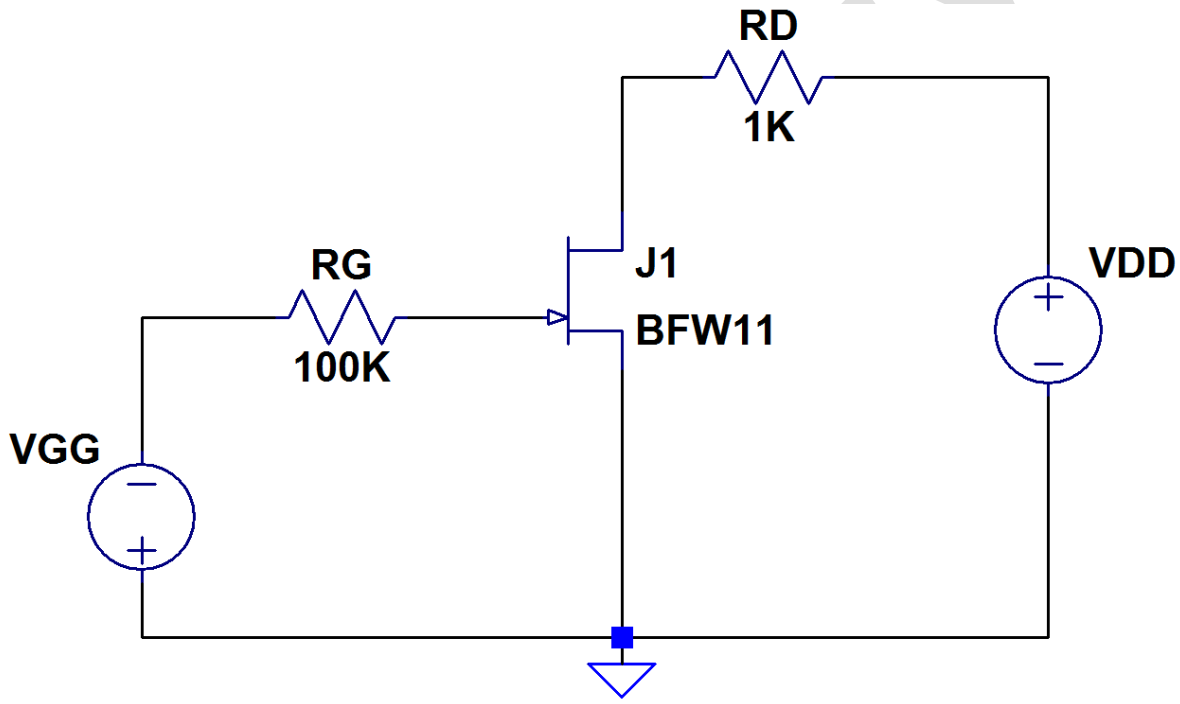
EXPERIMENT 05: N-CHANNEL JFET CHARACTERISTICS

AIM: To study transfer and output characteristics of a n-channel Junction field effect Transistor (JFET) in Common-source configuration.

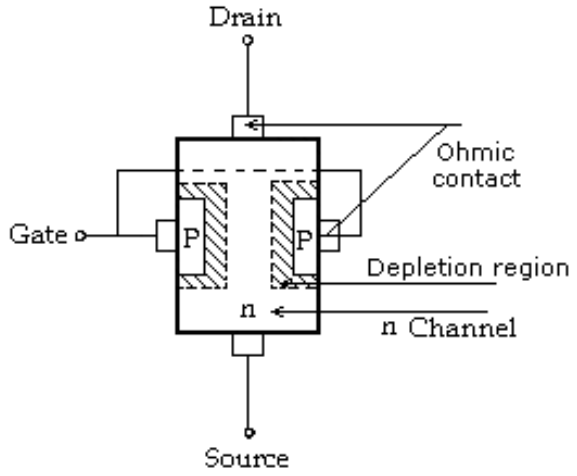
APPARATUS: JFET (BFW-11), Bread board, resistor (1KΩ, 100KΩ), connecting wires, Ammeters (0-10mA/ 0-25mA), DC power supply (0-30V) and multimeter.

CIRCUIT DIAGRAM:



THEORY:

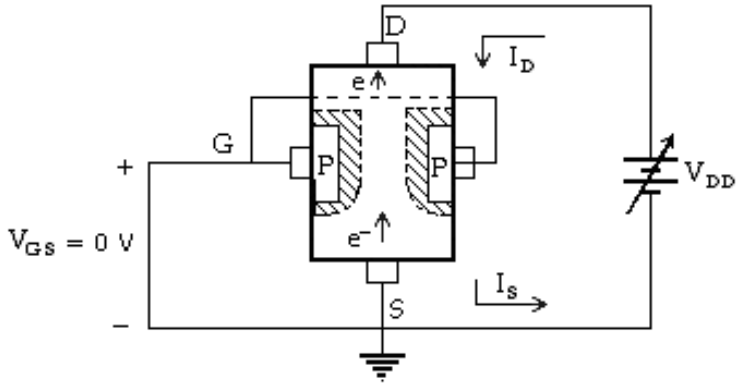
Construction & Characteristics of JFET



The basic construction of n-channel FET is as shown in figure. The major part of JEET is the channel between embedded P types of material. The top of the n-channel is connected to an ohmic contact called as 'Drain' (D) & lower end of Channel is called as 'Source' (S). The two p types of materials are connected together & to the 'Gate' terminal (G).

Characteristic:-

1. V_{GS} = 0V , V_{DS} - Some +ve Value:-



As shown in the figure the gate is directly connected to source to achieve V_{GS} = 0V, this is similar to no bias condition. The instant the voltage V_{DD} (=V_{DS}) is applied, the electrons will be

drawn to the drain terminal, causing I_D & I_S to flow (i.e. $I_D = I_S$). Under this condition the flow of charge is limited solely by resistance of the n channel between drain & source. It is important to note that the depletion region wider at the top of both p type of material. Since the upper terminal is more R .B. than the lower terminal (source - S).

As voltage V_{DS} is increased from 0 to few volts, the current will increase as determined by ohm's law. If still V_{DS} is increased & approaches a level referred as V_P, the depletion region will widen, causing a noticeable reduction in channel width. The reduced path of conduction causes the resistance to increase. The more the horizontal curve, the higher resistance.

If V_{DS} is increase to a level where it appears that the two depletion region would touch each other, the condition referred as 'pinch–off' will result. The level of V_{DS} that establish this condition is called as 'pinch off voltage' (V_P). At V_P, I_D should be zero, but practically a small channel still exists & very high density current still flows through the channel.

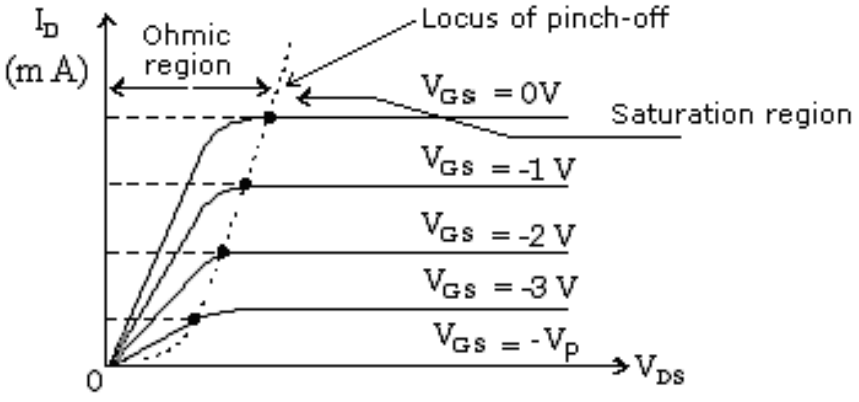
As V_{DS} is increased beyond V_P, the saturation current will flow through the channel (i.e I_{DSS}).

I_{DSS} – Drain to source current with short cut connection from source to Gate.

2. V_{GS} < 0V:-

If a –ve bias is applied between gate and source, the effect of the applied –ve bias V_{GS} is to establish depletion region similar to those obtained with V_{GS} = 0V but at lower level of V_{DS}.

As V_{GS} will become more & more –ve biased, the depletion layer pinch off occur at the less & less value of V_{DS}. Eventually, when $V_{GS} = -V_P$, will be sufficiently –ve to establish a saturation level, i.e. essentially 0 mA & for all practical purpose the device has been 'turned OFF'.



The region to the right of the pinch–off locus is typically employed in linear amplifiers (Amplifier with minimum distortion at applied signal) is commonly referred as the constant current, saturation or linear amplification region.

Voltage controlled region:-

The region left of pinch–off locus is called as ohmic or voltage controlled region. In this region the JEET can actually be employed as a variable register whose resistance is controlled by V_{GS}. As V_{GS} becomes more & more –ve, the slope of the curve becomes more and more horizontal, corresponding with an increasing resistance level.

$$rd = \frac{ro}{\left(1 - \frac{V_{GS}}{V_P}\right)^2}$$

where,

ro – the resistance with $V_{GS} = 0V$,

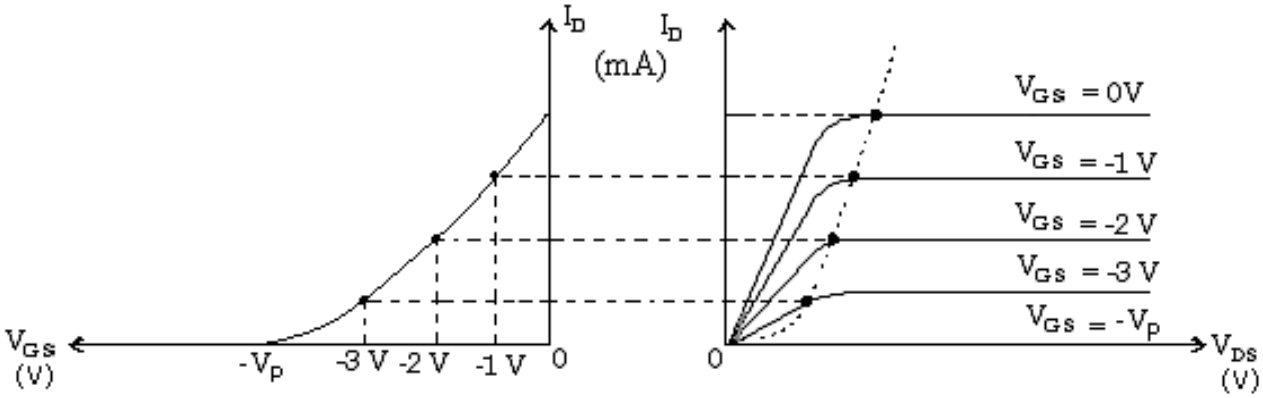
rd – the resistance at particular value of V_{GS}.

Transfer characteristic:-

The relation between I_D & V_{GS}, is given by Shockley's equation.

$$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2$$

The squared term of equation will result in a non–linear relationship between I_D & V_{GS}.



PROCEDURE:

OUTPUT CHARACTERISTICS:

1. Connect the circuit as per given diagram properly.
2. Keep V_{GS} = 0V by varying V_{GG}
3. Vary V_{DS} in step of 1V up to 10 volts and measure the drain current I_D. Tabulate all the readings.
4. Repeat the above procedure for V_{GS} as -0.5, -1V, -1.5V, -2V, -2.5V, -3V, -3.5V etc

TRANSFER CHARACTERISTICS:

1. Connect the circuit as per given diagram properly.
2. Set the voltage V_{DS} constant at 10 V.
3. Vary V_{GS} by varying V_{GG} in the step of 0.5 up to 3.5V and note down value of drain current I_D. Tabulate all the readings.
4. Plot the output characteristics V_{DS} vs I_D and transfer characteristics V_{GS} vs I_D.
5. Calculate I_{DSS}, V_P, gm, rd or ro from the graphs and verify it from the data sheet

OBSERVATION TABLE:

OUTPUT / DRAIN CHARACTERISTICS

V_{GS} = 0 V		**V_{GS} = -0.5 V**		**V_{GS} = -1 V**		**V_{GS} = -1.5 V**		**V_{GS} = -2 V ….. upto -3.5 V**	
V_{DS} (V)	**I_D (mA)**	**V_{DS} (V)**	**I_D (mA)**	**V_{DS} (V)**	**I_D (mA)**	**V_{DS} (V)**	**I_D (mA)**	**V_{DS} (V)**	**I_D (mA)**
0		0		0		0		0	
1		1		1		1		1	
2		2		2		2		2	
.		.		.		.		.	
.		.		.		.		.	
.		.		.		.		.	
Upto 10		Upto 10		Upto 10		Upto 10		Upto 10	

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TRANSFER CHARACTERISTICS

V_{DS} = 10 V	
V_{GS} (V)	**I_D (mA)**
0	
-0.5	
-1	
-1.5	
-2	
-2.5	
-3	
-3.5	

CALCULATION:

1. **Drain saturation current I_{DSS}:** Maximum current flowing through JFET when gate to source voltage is zero.

2. **Pinch-off voltage V_P :** Gate to source voltage at which, drain current becomes zero.

3. **Transconductance gm :** Ratio of small change in drain current (ΔI_D) to the corresponding change in gate to source voltage (ΔV_{GS}) for a constant V_{DS}.

   gm = ΔI_D / ΔV_{GS} at constant V_{DS}

4. **Output resistance :** It is given by the relation of small change in drain to source voltage (ΔV_{DS}) to the corresponding change in Drain Current (ΔI_D) for a constant V_{GS}, when the JFET is operating in pinch-off region.

   rd or ro = ΔV_{DS} / ΔI_D at a constant V_{GS}

RESULTS:

1. **I_{DSS} : _____**
2. **V_P : _____**
3. **gm : _____**
4. **ro : _____**

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CONCLUSION:

POST LAB QUESTIONS:

1. What are the advantages of JFET?
2. What is Transconductance?
3. What are the disadvantages of JFET?
4. Why an input characteristic of JFET is not drawn?
5. What is the difference between n- channel JFET and p-channel JFET?

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