**EXPERIMENT 08:** SPICE Simulation of and implementation for MOSFET characteristics

**AIM:** Simulate output and transfer I-V characteristics for n-channel and p-channel Enhancement type MOSFET in common source configuration.

**SOFTWARE TOOL:** PC loaded with LT-Spice

**THEORY:**

**PART A**

**Introduction to LTspice:**

LTspice is freeware computer software implementing a SPICE simulator of electronic circuits, produced by semiconductor manufacturer Linear Technology (LTC).

LTspice IV provides a schematic capture and waveform viewer with enhancements and models to speed the simulation of switching regulators. Supplied with LTspice IV are macro models for 80% of LTC's switching regulators and operational amplifiers, transistors, MOSFETs, and passive components.

LTspice IV is node-unlimited and third-party models can be imported. Circuit simulations based on transient, AC, noise and DC analysis can be plotted as well as Fourier analysis. Heat dissipation of components can be calculated and efficiency reports can also be generated.

LTspice IV is used within LTC, and by many users in fields including radio frequency electronics, power electronics, digital electronics, and other disciplines. LTspice IV does not generate printed circuit board (PCB) layouts, but netlists can be imported into layout programs. LTspice IV can't simulate a complex digital logic.

**PART B**

**Introduction to SPICE programming:**

SPICE (Simulation Program with Integrated Circuit Emphasis) is a general-purpose, open source analog electronic circuit simulator. It is a program used in integrated circuit and board-level design to check the integrity of circuit designs and to predict circuit behavior.

SPICE is a general-purpose circuit simulation program for nonlinear dc, nonlinear transient, and linear ac analyses. Circuits may contain resistors, capacitors, inductors, mutual inductors, independent voltage and current sources, four types of dependent sources, switches, and uniform distributed RC lines, and the five most common semiconductor devices: diodes, BJTs, JFETs, MESFETs, and MOSFETs.

SPICE has built-in models for the semiconductor devices, and the user need specify only the pertinent model parameter values. The model for the BJT is based on the integral-charge model of Gummel and Poon; however, if the Gummel- Poon parameters are not specified, the model reduces to the simpler Ebers-Moll model. In either case, charge-storage effects, ohmic resistances, and a current-dependent output conductance may be included. The diode model can be used for either junction diodes or Schottky barrier diodes. The JFET model is based on the FET model of Shichman and Hodges. Different MOSFET models are implemented: MOS1 is described by a square-law I-V characteristic, MOS2 is an analytical model, while MOS3 is a semi-empirical model.

**Semiconductor Devices**

1. **MOSFET's**

General form:

MXXXXXXX ND NG NS NB MNAME <L=VAL> <W=VAL> <AD=VAL> <AS=VAL>+ <PD=VAL> <PS=VAL> <NRD=VAL> <NRS=VAL> <OFF> <IC=VDS,VGS,VBS>

Examples:

M1 24 2 0 20 TYPE1

M31 2 17 6 10 MODM L=5U W=2U

M31 2 16 6 10 MODM 5U 2U

M1 2 9 3 0 MOD1 L=10U W=5U AD=100P AS=100P PD=40U PS=40U

M1 2 9 3 0 MOD1 10U 5U 2P 2P

ND, NG, NS, and NB are the drain, gate, source, and bulk (substrate) nodes, respectively. MNAME is the model name. L and W are the channel length and width, in meters. AD and AS are the areas of the drain and source diffusions, in sq-meters. Note that the suffix U specifies microns (1E-6 m) and P sq-microns (1E-12 sq-m). If any of L, W, AD, or AS are not specified, default values are used. The user may specify the values to be used for these default parameters on the .OPTIONS card. The use of defaults simplifies input deck preparation, as well as the editing required if device geometries are to be changed. PD and PS are the perimeters of the drain and source junctions, in meters. NRD and NRS designate the equivalent number of squares of the drain and source diffusions; these values multiply the sheet resistance RSH specified on the .MODEL card for an accurate representation of the parasitic series drain and source resistance of each transistor. PD and PS default to 0.0 while NRD and NRS to 1.0.

**MOSFET Models (both N and P Channel)**

SPICE provides three MOSFET device models which differ in the formulation of the I-V characteristic. The variable LEVEL specifies the model to be used:

LEVEL=1 -> Shichman-Hodges

LEVEL=2 -> MOS2

LEVEL=3 -> MOS3, a semi-empirical model

The dc characteristics of the MOSFET are defined by the device parameters VTO, KP, LAMBDA, PHI and GAMMA. These parameters are computed by SPICE if process parameters (NSUB, TOX, ...) are given, but user-specified values always override. VTO is positive (negative) for enhancement mode and negative (positive) for depletion mode N-channel (P-channel) devices. Charge storage is modeled by three constant capacitors, CGSO, CGDO, and CGBO which represent overlap capacitances, by the nonlinear thin-oxide capacitance which is distributed among the gate, source, drain, and bulk regions, and by the nonlinear depletion-layer capacitances for both substrate junctions divided into bottom and periphery, which vary as the MJ and MJSW power of junction voltage respectively, and are determined by the parameters CBD, CBS, CJ, CJSW, MJ, MJSW and PB. There are two built-in models of the charge storage effects associated with the thin-oxide. The thin-oxide charge storage effects are treated slightly different for the LEVEL=1 model. These voltage-dependent capacitances are included only if TOX is specified in the input description.

There is some overlap among the parameters describing the junctions, e.g. the reverse current can be input either as IS (in A) or as JS (in A/m\*\*2). Whereas the first is an absolute value the second is multiplied by AD and AS to give the reverse current of the drain and source junctions respectively. This methodology has been chosen since there is no sense in relating always junction characteristics with AD and AS entered on the device card; the areas can be defaulted. The same idea applies also to the zero-bias junction capacitances CBD and CBS (in F) on one hand, and CJ (in F/m\*\*2) on the other. The parasitic drain and source series resistance can be expressed as either RD or RS (in ohms) or RSH (in ohms/sq.), the latter being multiplied by the number of squares NRD and NRS input on the device card.

name parameter units default example

---- --------- ----- ------- ----

1 LEVEL model index - 1

2 VTO zero-bias threshold voltage V 0.0 1.0

3 KP transconductance parameter A/V\*\*2 2.0E-5 3.1E-5

4 GAMMA bulk threshold parameter V\*\*0.5 0.0 0.37

5 PHI surface potential V 0.6 0.65

6 LAMBDA channel-length modulation

(MOS1 and MOS2 only) 1/V 0.0 0.02

7 RD drain ohmic resistance Ohm 0.0 1.0

8 RS source ohmic resistance Ohm 0.0 1.0

9 CBD zero-bias B-D junction capacitance. F 0.0 20FF

10 CBS zero-bias B-S junction capacitance. F 0.0 20FF

11 IS bulk junction saturation current A 1.0E-14 1.0E-15

12 PB bulk junction potential V 0.8 0.87

13 CGSO gate-source overlap capacitance

per meter channel width F/m 0.0 4.0E-11

14 CGDO gate-drain overlap capacitance

per meter channel width F/m 0.0 4.0E-11

15 CGBO gate-bulk overlap capacitance

per meter channel length F/m 0.0 2.0E-10

16 RSH drain and source diffusion

sheet resistance W/sq. 0.0 10.0

17 CJ zero-bias bulk junction bottom cap.

per sq-meter of junction area F/m\*\*2 0.0 2.0E-4

18 CJSW zero-bias bulk junction sidewall cap.

per meter of junction perimeter F/m 0.0 1.0E-9

19 MJSW bulk junction sidewall grading coef. - 0.33

20 TOX oxide thickness meter 1.0E-7 1.0E-7

21 NSUB substrate doping 1/cm\*\*3 0.0 4.0E15

22 NSS surface state density 1/cm\*\*2 0.0 1.0E10

23 NFS fast surface state density 1/cm\*\*2 0.0 1.0E10

24 XJ metallurgical junction depth meter 0.0 1U

25 LD lateral diffusion meter 0.0 0.8U

26 UO surface mobility cm\*\*2/V-s 600 700

27 UCRIT critical field for mobility

degradation (MOS2 only) V/cm 1.0E4 1.0E4

28 UEXP critical field exponent in

mobility degradation (MOS2 only) - 0.0 0.1

29 UTRA transverse field coef (mobility)

(deleted for MOS2) - 0.0 0.3

30 VMAX maximum drift velocity of carriers m/s 0.0 5.0E4

31 DELTA width effect on threshold voltage

(MOS2 and MOS3) - 0.0 1.0

32 KAPPA saturation field factor (MOS3 only) - 0.2 0.5

**PROBLEM STATEMENT 1A**

Simulate I-V transfer and output characteristics for an N-channel MOSFET in common source configuration using schematic capture in LTspice.

**CIRCUIT SCHEMATIC 1A**

**CIRCUIT SCHEMATIC will come here**

**Add separate circuits for output and transfer**

**PROBLEM STATEMENT 1B**

Simulate I-V transfer and output characteristics for an N-channel MOSFET in common source configuration using SPICE programming in LTspice

**SPICE CODE 1B**

**spice code for I-V transfer and output characteristics for an N-channel MOSFET**

**Write two separate spices codes for transfer and output curves**

**Add L and W as model parameters in the spice code and observe the changes in the simulation results (optional)**

**SIMULATION RESULT 1A and 1B**

**Simulation results for n-channel MOSFET transfer and output curve will come here**

**Observe the following from the simulation plot for Problem Statement 1a and 1b**

1. **VT : \_\_\_\_\_\_\_\_**
2. **gm : \_\_\_\_\_\_\_\_**

**PROBLEM STATEMENT 2A**

Simulate I-V transfer and output characteristics for a P-channel MOSFET in common source configuration using schematic capture in LTspice.

**CIRCUIT SCHEMATIC 2A**

**CIRCUIT SCHEMATIC will come here**

**Add separate circuits for output and transfer**

**PROBLEM STATEMENT 2B**

Simulate I-V transfer and output characteristics for a P-channel MOSFET in common source configuration using SPICE programming in LTspice

**SPICE CODE 2B**

**spice code for I-V transfer and output characteristics for an p-channel MOSFET**

**Write two separate spices codes for transfer and output curves**

**Add L and W as model parameters in the spice code and observe the changes in the simulation results (optional)**

**SIMULATION RESULT 2A and 2B**

**Simulation results for p- channel MOSFET transfer and output curve will come here**

**Observe the following from the simulation plot for Problem Statement 2a and 2b**

1. **VT : \_\_\_\_\_\_\_\_**
2. **gm : \_\_\_\_\_\_\_\_**

**CONLUSION:**