EXPERIMENT 12: SIMULATION STUDY OF DIFFERENT BIASING CIRCUITS USING NPN BJT

AIM:

1) To study different BJT DC biasing circuits
2) To design voltage divider bias circuit using NPN BJT

SOFTWARE TOOL: PC loaded with LT-Spice

THEORY:

Transistor Biasing is the process of setting a transistors DC operating voltage or current conditions to the correct level so that any AC input signal can be amplified correctly by the transistor.

A transistors steady state of operation depends a great deal on its base current, collector voltage, and collector current and therefore, if a transistor is to operate as a linear amplifier, it must be properly biased to have a suitable operating point.

Establishing the correct operating point requires the proper selection of bias resistors and load resistors to provide the appropriate input current and collector voltage conditions. The correct biasing point for a bipolar transistor, either NPN or PNP, generally lies somewhere between the two extremes of operation w.r.t it being either "fully-ON" or "fully-OFF" along its load line. This central operating point is called the "Quiescent Operating Point", or Q-point

When a bipolar transistor is biased so that the Q-point is near the middle of its operating range that is approximately halfway between cut-off and saturation. This mode of operation allows the output current to increase and decrease around the amplifiers Q-point without distortion as the input signal swings through a complete cycle. In other words, the output current flows for the full 360^o of the input cycle.

The best bias circuits have the greatest stability, they hold the currents and voltages substantially constant regardless of the h_{fe} and temperature variations.

PROCEDURE:

PART 1:

Analysis of various biasing circuits for different values of β

1) Implement the biasing circuits on the work space of LT Spice
2) Perform the DC operating point analysis and find the terminal voltages and currents for different values of β
3) From the analysis, comment on the stability of various biasing circuits.

PART 2:
Design of Voltage divider biasing circuit

1) Implement the designed biasing circuits on the work space of LT Spice
2) From the dc operating point analysis, compare theoretical design calculations with those of simulation results.

OBSERVATIONS & CALCULATIONS:

PART 1

Fixed Bias Circuit

β	I_{CQ}	V_{CEQ}
50		
100		
150		

One can take any three values of β i.e eg 50,75,100
Draw Circuit of Fixed Bias circuit and show theoretical calculations for any one value of β

Emitter Bias Circuit

β	I_{CQ}	V_{CEQ}
50		
100		
150		

One can take any three values of β i.e eg 50,75,100
Draw Circuit of Emitter Bias circuit and show theoretical calculations for any one value of β

Collector to Base Bias Circuit

β	I_{CQ}	V_{CEQ}
50		
100		
150		

One can take any three values of β i.e eg 50,75,100
Draw Circuit of Collector to base Bias circuit and show theoretical calculations for any one value of β

Collector to Base Bias with emitter resistor

β	I_{CQ}	V_{CEQ}
50		
100		
150		

One can take any three values of β i.e eg 50,75,100
Draw Circuit of Collector to base Bias with emitter resistor and show theoretical calculations for any one value of β

Voltage divider Bias Circuit

β	I_{CQ}	V_{CEQ}
50		
100		
150		

One can take any three values of β i.e eg 50,75,100
Draw Circuit of Voltage divider Bias circuit and show theoretical calculations for any one value of β

PART 2

Draw Circuit of designed Voltage divider Bias circuit and show the design steps for Voltage divider bias for Q point (5V, 5mA) on ruled side of the page

RESULTS:

Compare the β variations for various biasing circuit

CONCLUSION:

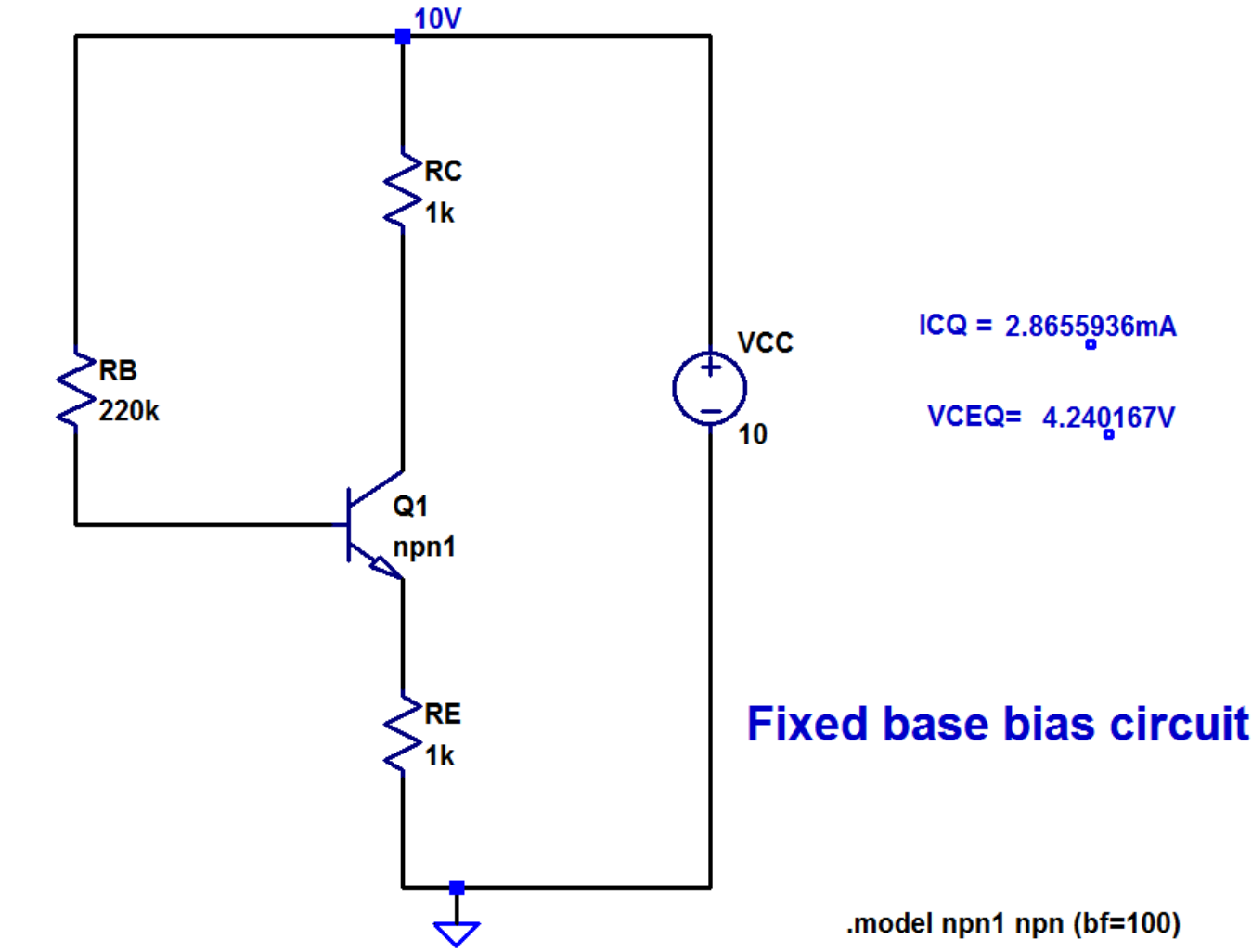
Part 1
Part 2

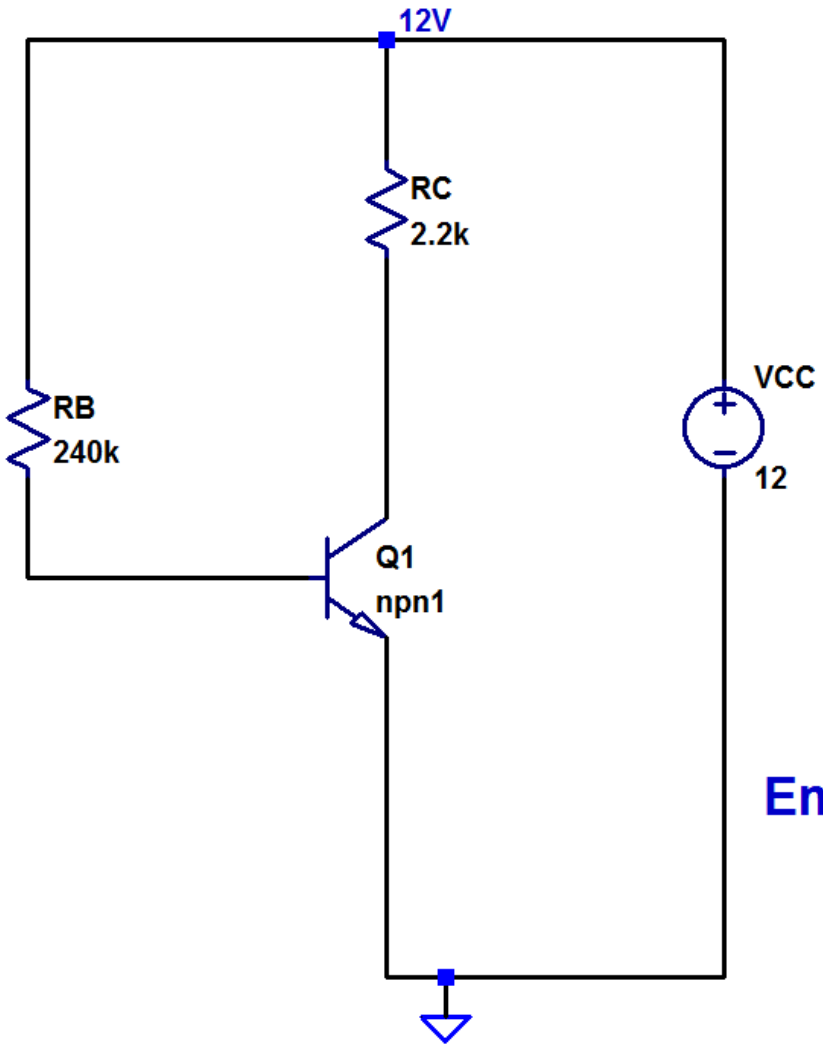
Write conclusion part wise:

POST LAB QUESTIONS:

1. Why is voltage divider bias best in terms of stability ?
2. Define the various stability factors

Following 6 PRINTOUTS TO BE ATTACHED with the experiment:





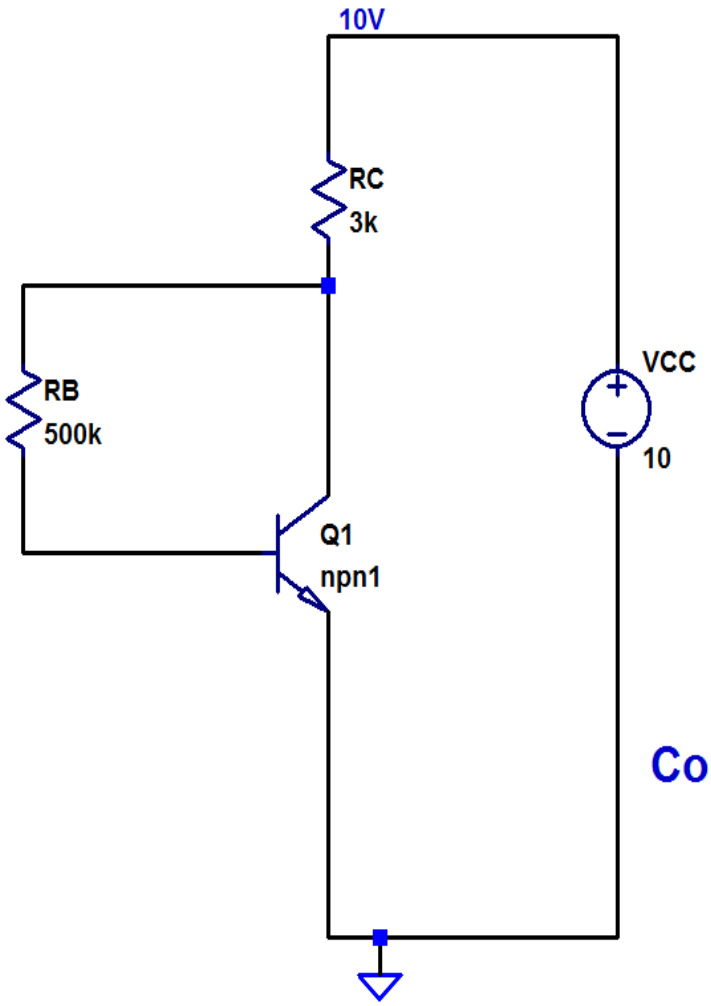
ICQ = 2.3341649mA

VCEQ= 6.8649042V

Emitter bias circuit

.model npn1 npn (bf=50)

.op



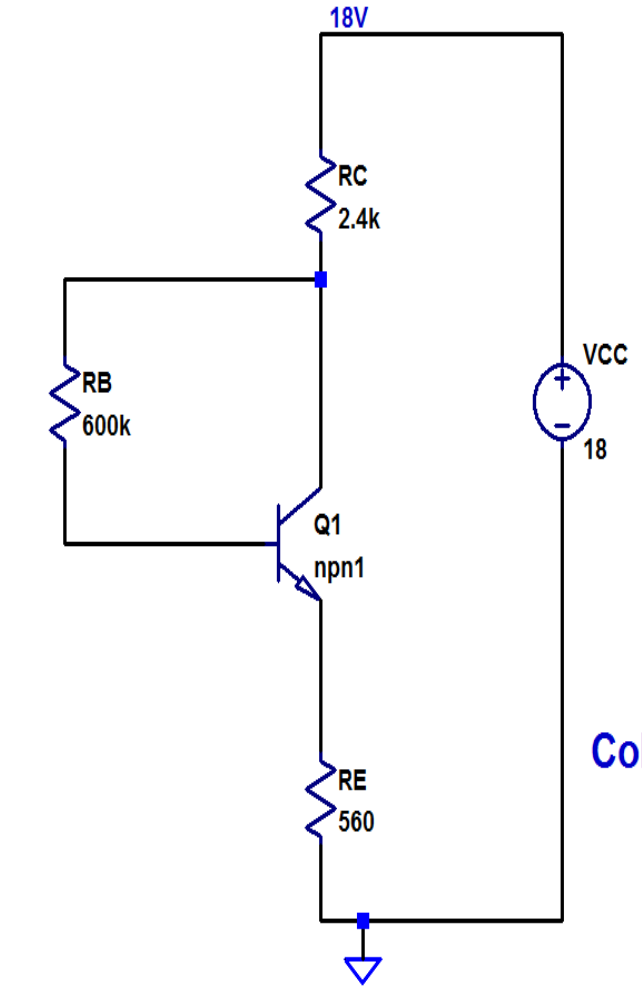
ICQ = 1.1484687mA

VCEQ= 6.5201447V

Collector to base bias circuit

.model npn1 npn (bf=100)

.op



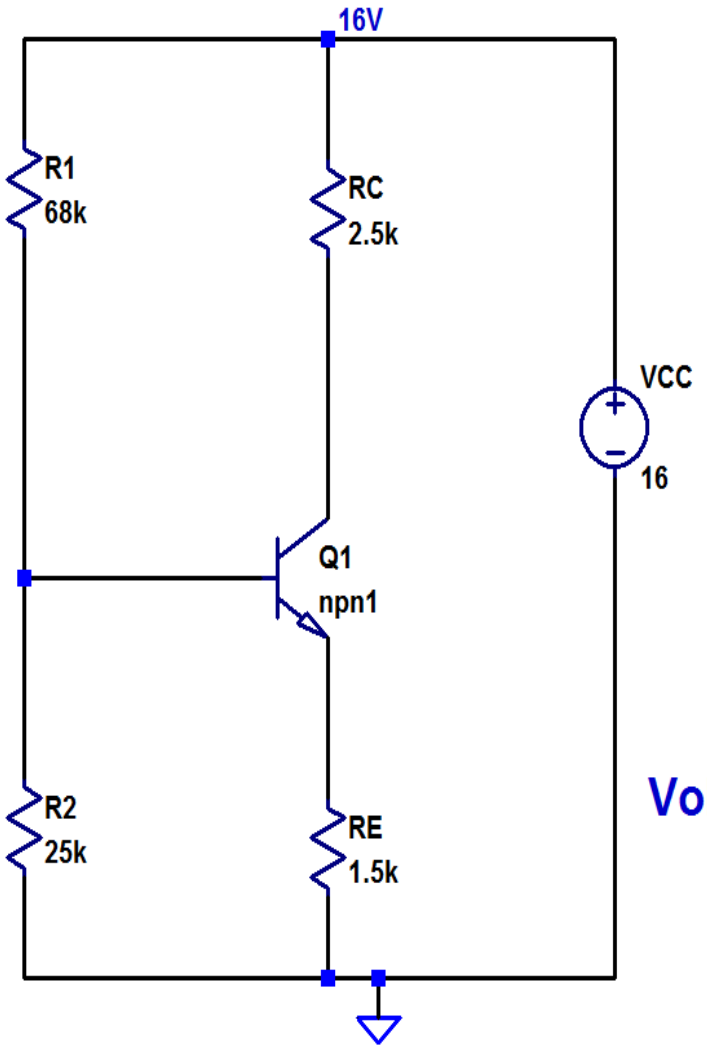
ICQ = 1.5650024mA

VCEQ= 13.305828V

Collector to base bias with Emitter resistor

.model npn1 npn (bf=75)

.op



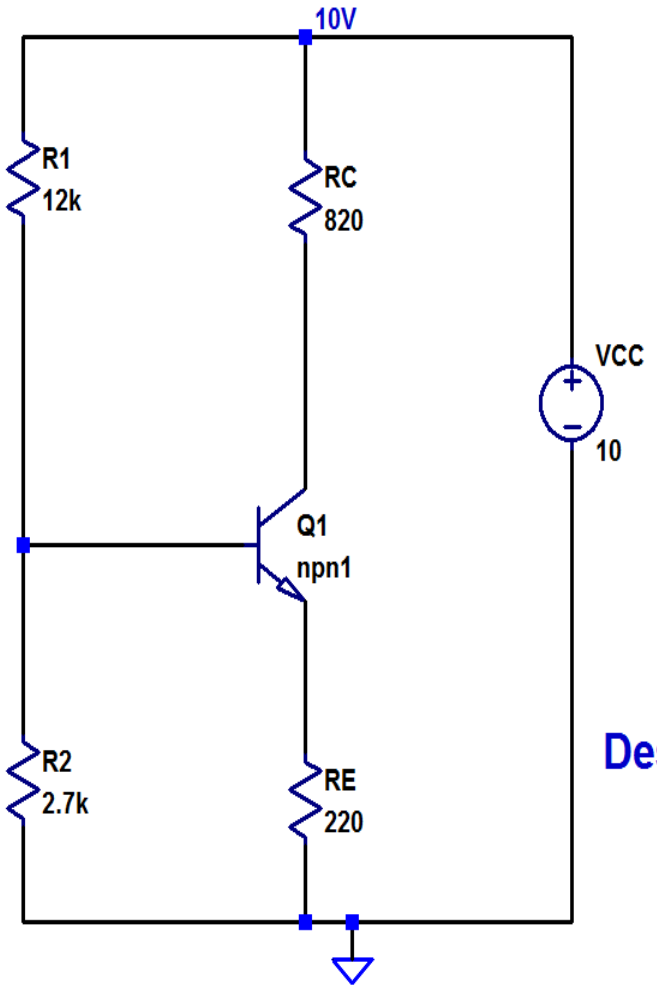
ICQ = 2.1214653mA

VCEQ= 7.485051V

Voltage divider bias circuit

.model npn1 npn (bf=100, IS = 1E-15, Vaf = 80)

.op



ICQ = 4.7131465mA

VCEQ= 5.0886667V

Designed Voltage divider bias circuit

.model npn1 npn (bf=100, IS = 1E-14, Vaf = 60)

.op