D. J. SANGHVI COLLEGE OF ENGINEERING
DEPARTMENT OF ELECTRONICS ENGINEERING
EXL302: ELECTRONIC DEVICES AND CIRCUITS 1 SEM III
MID TERM 2

11^{th} **October, 2017** **[Total Marks: 20]**

1. **Attempt all the questions for 20 marks**
2. **Read the questions carefully before attempting**
3. **Don't rewrite the question while answering, only answers have to be written.**

1. Consider the circuit 1

   ✠ Input to amplifier is 20mV peak to peak voltage, with 1KHz frequency

   i) What type of circuit is this **[1]**

   ii) Calculate the value of V_{GSQ} **[1]**

   iii) Calculate the value of I_{DQ} **[1]**

   iv) Sketch the small signal AC equivalent of the circuit 1 **[1]**

   v) Calculate the value of g_m **[1]**

   vi) Find the input impedance Z_i of the circuit **[1]**

   vii) Find the output impedance Z_o of the circuit **[1]**

   viii) Calculate the voltage gain of the circuit **[1]**

   ix) If input is 20mV p-p, calculate the output voltage of the circuit **[1]**

   x) Plot input Vin(t) and output Vout(t) waveforms of the circuit **[1]**

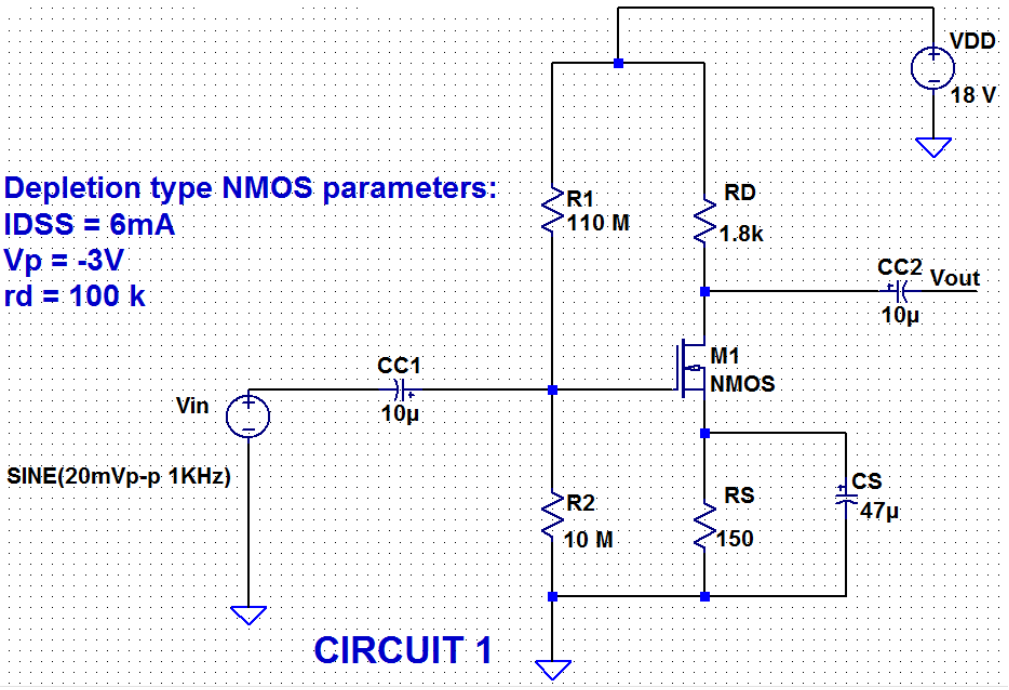

Figure 1: Question 1

2. a) Design an N-channel Enhancement type MOSFET using voltage-divider biasing for the following specifications: **[5]**

$I_{DQ} = 5mA$, $V_{DSQ} = 5V$

MOSFET parameters given are: $K_n = 25mA/V^2$, $V_{TN} = 1V$

OR

a) Mention the various DC biasing schemes for n-channel E-type MOSFET. **[1]**

b) Draw voltage divider bias circuit using n-channel enhancement type MOSFET and write the expressions of V_{DSQ}, V_{GSQ} and I_{DQ}. **[1+2]**

c) Draw the DC load line for the voltage divider biasing scheme along with equation for DC load line. **[1]**

3. a) Draw voltage divider bias circuit using NPN BJT and derive the expression of V_{CEQ} and I_{CQ} **[1+3]**

b) For an NPN BJT to be in active region, how should be the EB junction and BC junction be biased. **[1]**

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