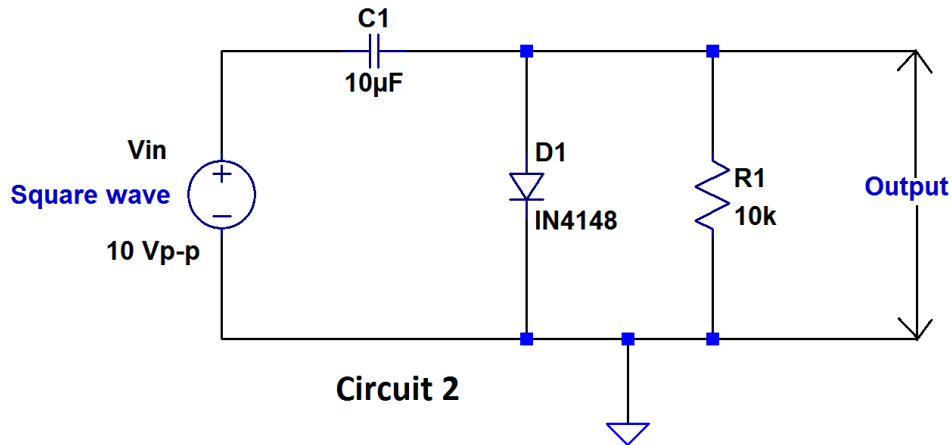


D. J. SANGHVI COLLEGE OF ENGINEERING
DEPARTMENT OF ELECTRONICS ENGINEERING
ELX302: Electronic Devices and Circuits I SEM III
CLAMPER Circuit

25th July, 2017

[Total Marks: 05]

1. Identify the circuit 2 and draw output waveform with proper voltage levels. Write the output expression [05]
 output expression



Solution : Given circuit is a Negative clamper

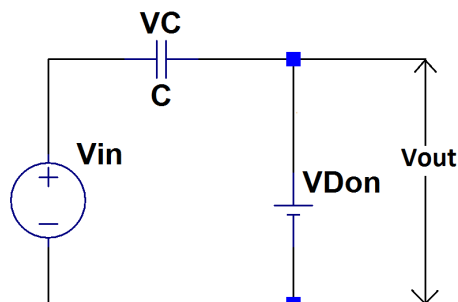
Since given diode IN4148 is a practical diode , we will prefer constant voltage model (i.e $V_{Don} = 0.7V$).

Given : $V_{in} = 10Vp - p$, i.e $V_m = 5V$

Assumption: RC time constant is large enough to ensure that voltage across capacitor does not discharge significantly during the period the diode is OFF.

OPERATION:

1. During positive half cycle, Diode D1 is ON when $V_{in} > V_{Don}$, i.e the circuit becomes:

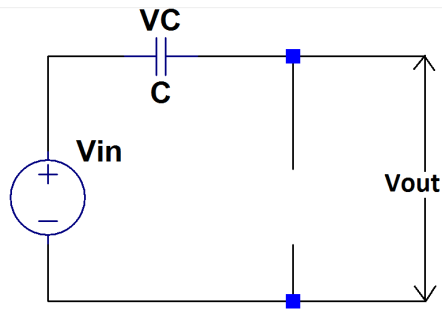


$V_{out} = V_{Don} = 0.7V$ during positive half cycle

At the same time, voltage across capacitor V_C charges upto V_m ,

KVL gives us: $V_{in} - V_C - V_{Don} = 0$

$V_C = V_{in} - V_{Don} = V_m - V_{Don} = 5 - 0.7 = 4.3V$... voltage across Capacitor during positive half cycle.



2. During negative half cycle, Diode D1 is OFF for entire negative cycle , i.e the circuit becomes:

Note: During negative half cycle, capacitor holds the charges $V_C = 4.3V$ and act as a battery.

KVL gives us: $-V_{in} - V_C - V_{out} = 0$

$V_{out} = -V_{in} - V_C = -V_m - V_C = -5 - 4.3 = -9.3V$ during negative half cycle

Hence, the output waveform is as follows:

