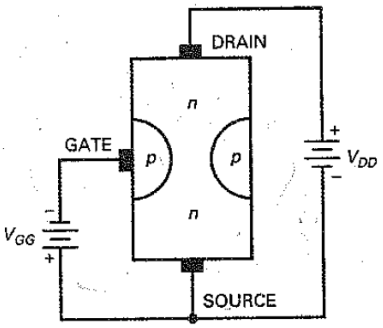
Reference: Electronic Devices and Circuit by Dr. R.S Sedha

Gate Voltage Controls Drain Current

In Fig. 13-2, electrons flowing from the source to the drain must pass through the narrow **channel** between the depletion layers. When the gate voltage becomes more negative, the depletion layers expand and the conducting channel becomes narrower. The more negative the gate voltage, the smaller the current between the source and the drain.

The JFET is a **voltage-controlled device** because an input voltage controls an output current. In a JFET, the gate-to-source voltage V_{GS} determines how much current flows between the source and the drain. When V_{GS} is zero, maximum drain current flows through the JFET. This is why a JFET is referred to as a normally on device. On the other hand, if V_{GS} is negative enough, the depletion layers touch and the drain current is cut off.

Figure 13–2 Normal biasing of JFET.



19.9 Salient Features of JFET

The following are some salient features of *JFET* :

(*i*) A *JFET* is a three-terminal *voltage-controlled* semiconductor device *i.e.* input voltage controls the output characteristics of *JFET*.

(*ii*) The *JFET* is *always* operated with gate-source *pn* junction *reverse biased.

(*iii*) In a *JFET*, the gate current is zero *i.e.* $I_G = 0$A.

(*iv*) Since there is no gate current, $I_D = I_S$.

(*v*) The *JFET* must be operated between V_{GS} and $V_{GS\,(off)}$. For this range of gate-to-source voltages, I_D will vary from a maximum of I_{DSS} to a minimum of almost zero.

(*vi*) Because the two gates are at the same potential, both depletion layers widen or narrow down by an equal amount.

(*vii*) The *JFET* is not subjected to thermal runaway when the temperature of the device increases.

(*viii*) The drain current I_D is controlled by changing the channel width.

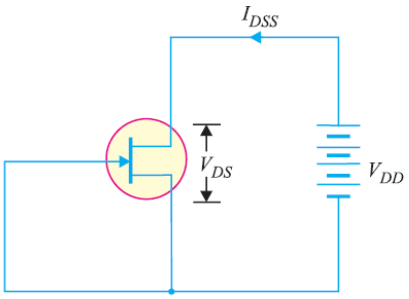


Fig. 19.9

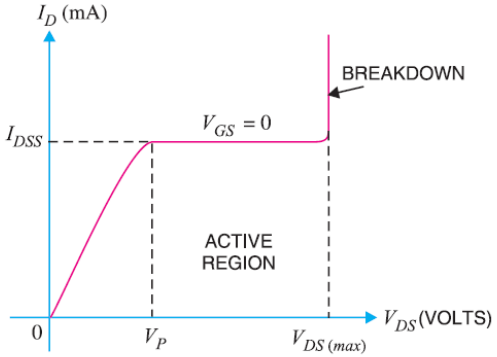


Fig. 19.10

The following points may be noted carefully :

(*i*) Since I_{DSS} is measured under shorted gate conditions, it is the maximum drain current that you can get with normal operation of *JFET*.

(*ii*) There is a maximum drain voltage [$V_{DS\,(max)}$] that can be applied to a *JFET*. If the drain voltage exceeds $V_{DS\,(max)}$, *JFET* would breakdown as shown in Fig. 19.10.

(*iii*) The region between V_P and $V_{DS\,(max)}$ (breakdown voltage) is called *constant-current region* or *active region*. As long as V_{DS} is kept within this range, I_D will remain constant for a constant value of V_{GS}. In other words, in the active region, *JFET* behaves as a constant–current device. For proper working of *JFET*, it must be operated in the active region.

19.10 Important Terms

In the analysis of a *JFET* circuit, the following important terms are often used :

1. Shorted-gate drain current (I_{DSS})
2. Pinch off voltage (V_P)
3. Gate-source cut off voltage [$V_{GS\,(off)}$]

1. Shorted-gate drain current (I_{DSS}). *It is the drain current with source short-circuited to gate (i.e. $V_{GS} = 0$) and drain voltage (V_{DS}) equal to pinch off voltage.* It is sometimes called *zero-bias current*.

Fig 19.9 shows the *JFET* circuit with $V_{GS} = 0$ *i.e.*, source shorted-circuited to gate. This is normally called shorted-gate condition. Fig. 19.10 shows the graph between I_D and V_{DS} for the shorted gate condition. The drain current rises rapidly at first and then levels off at pinch off voltage V_P. The drain current has now reached the maximum value I_{DSS}. When V_{DS} is increased beyond V_P, the depletion layers expand at the top of the channel. The channel now acts as a current limiter and **holds drain current constant at I_{DSS}.

** When drain voltage equals V_P, the channel becomes narrow and the depletion layers almost touch each other. The channel now acts as a current limiter and holds drain current at a constant value of I_{DSS}.

2. Pinch off Voltage (V_P). *It is the minimum drain-source voltage at which the drain current essentially becomes constant.*

Figure 19.11 shows the drain curves of a *JFET*. Note that pinch off voltage is V_P. The highest curve is for $V_{GS} = 0$V, the shorted-gate condition. For values of V_{DS} greater than V_P, the drain current is almost constant. It is because when V_{DS} equals V_P, the channel is effectively closed and does not allow further increase in drain current. It may be noted that for proper function of *JFET*, it is always operated for $V_{DS} > V_P$. However, V_{DS} should not exceed $V_{DS\,(max)}$ otherwise *JFET* may breakdown.

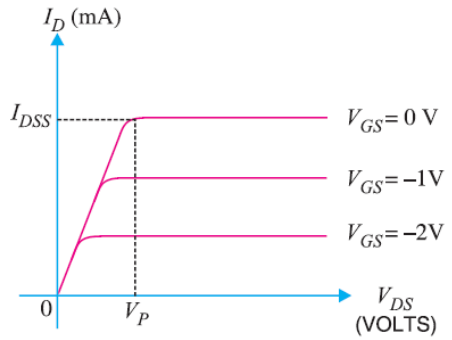


Fig . 19.11

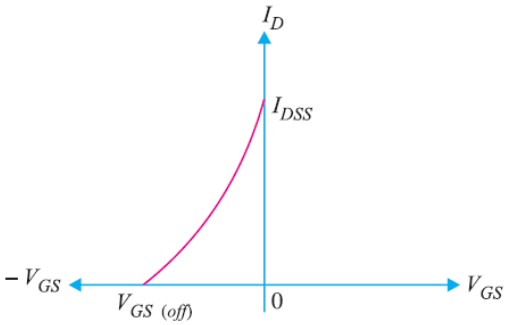


Fig . 19.12

3. Gate-source cut off voltage $V_{GS\ (off)}$. *It is the gate-source voltage where the channel is completely cut off and the drain current becomes zero.*

The idea of gate-source cut off voltage can be easily understood if we refer to the transfer characteristic of a *JFET* shown in Fig. 19.12. As the reverse gate-source voltage is increased, the cross-sectional area of the channel decreases. This in turn decreases the drain current. At some reverse gate-source voltage, the depletion layers extend completely across the channel. In this condition, the channel is cut off and the drain current reduces to zero. The gate voltage at which the channel is cut off (*i.e.* channel becomes non-conducting) is called gate-source cut off voltage $V_{GS\,(off)}$.

Notes. **(*i*)** It is interesting to note that $V_{GS\ (off)}$ will always have the same magnitude value as V_P. For example if $V_P = 6$ V, then $V_{GS\ (off)} = -6$ V. Since these two values are always equal and opposite, only one is listed on the specification sheet for a given *JFET*.

(*ii*) There is a distinct difference between V_P and $V_{GS\,(off)}$. Note that V_P is the value of V_{DS} that causes the *JEFT* to become a constant current device. It is measured at $V_{GS} = 0$ V and will have a constant drain current = I_{DSS}. However, $V_{GS\ (off)}$ is the value of V_{GS} that causes I_D to drop to nearly zero.

19.12 Advantages of JFET

A *JFET* is a voltage controlled, constant current device (similar to a vacuum pentode) in which variations in input voltage control the output current. It combines the many advantages of both bipolar transistor and vacuum pentode. Some of the advantages of a *JFET* are :

(*i*) It has a very high input impedance (of the order of 100 MΩ). This permits high degree of isolation between the input and output circuits.

(*ii*) The operation of a *JFET* depends upon the bulk material current carriers that do not cross junctions. Therefore, the inherent noise of tubes (due to high-temperature operation) and those of transistors (due to junction transitions) are not present in a *JFET*.

(*iii*) A *JFET* has a negative temperature co-efficient of resistance. This avoids the risk of thermal runaway.

(*iv*) A *JFET* has a very high power gain. This eliminates the necessity of using driver stages.

(*v*) A *JFET* has a smaller size, longer life and high efficiency.