FAILURE MECHANISM RELATED TO ELECTRONIC PACKAGES

INSTANTANEOUS ELECTRICAL FAILURE

1. Electrostatic discharge (ESD):

As semiconductor devices are miniaturized, the resistance to static electricity is being deteriorated. So, this section describes the failure modes, mechanisms and damage models regarding electrostatic damage of semiconductor devices.

a) Electrostatic discharge models

1) Damage models

A semiconductor device causes electrostatic discharge if external static electricity is discharged to the device, if static electricity stored in the device is discharged to an external conductor, or if the electric field condition around the device is abruptly changed. Based on these facts, electrostatic discharge models can be classified as shown in Table 3.6.

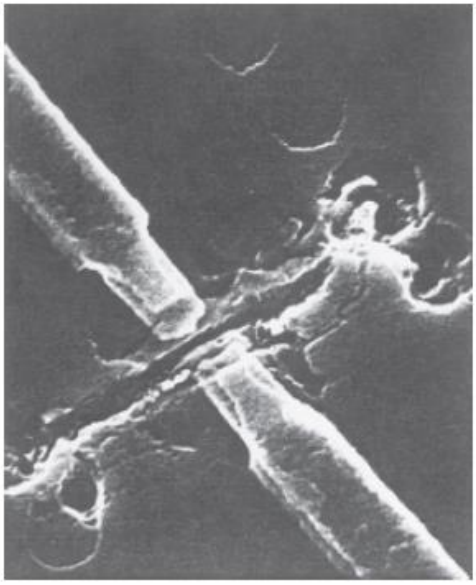
Table 3.6 Electrostatic discharge models

A (Large capacity, comparatively low speed)	B (Small capacity, high speed)	C
Description of model: A metal or a conductor near the device is electrostatically charged, and then the charged static electricity is discharged to a terminal of the device. As a result, electrostatic discharge will occur.	Description of model: The device is directly or indirectly charged with static electricity, and a terminal of the device discharges the static electricity to a metal or a conductor near the device. As a result, electrostatic discharge will occur.	Description of model: Transient voltage or overcurrent is generated inside the device due to a change in the electric field around the device. As a result, electrostatic discharge will occur.

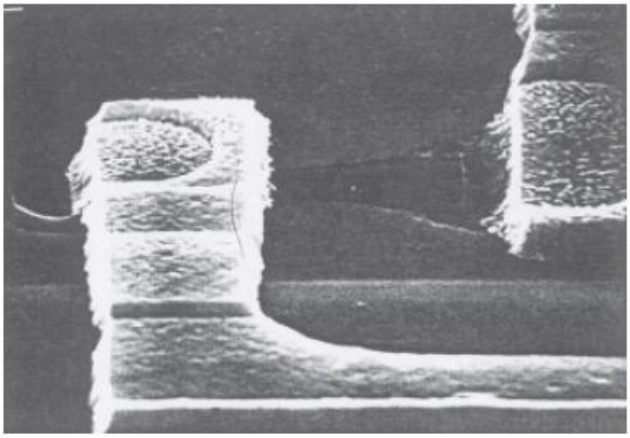
2) **Failure modes and mechanisms**

When static electricity is applied to a semiconductor device, elements in the device may be damaged. So, leakage current may flow mainly, and the characteristics of the device may deteriorate. If an extremely high static electricity is applied to a device (though such a problem rarely occurs), the electrostatic energy may melt the wire material, etc. So an “open” failure may occur. The mechanisms of device damage and deterioration caused by static electricity can be roughly classified into two types. One type is the thermal damage type, and the other type is the electric field damage type.

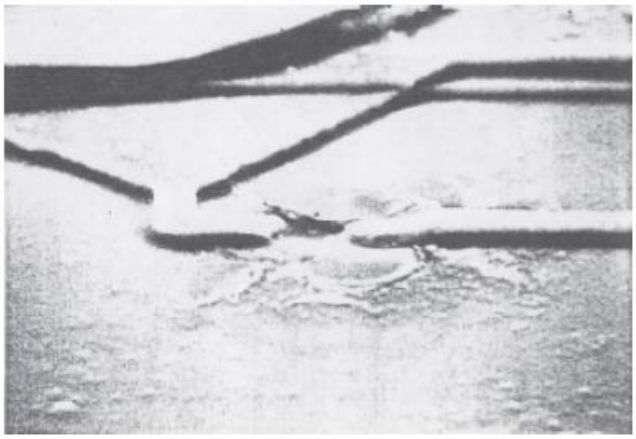
Figures 3.61 respectively show typical examples of damage by electrostatic discharge: junction damage of a MOS transistor, junction damage of a bipolar transistor, and Al wire melting.



a) MOS Tr damage
(damage between drain and source)



b) Bipolar Tr damage
(damage between emitter and base)



c) Al wire melting

Figure 3.61 Examples of electrostatic discharge

2. Electrical Over-Stress (EOS):

Electrical Over-Stress (EOS) is a term/acronym used to describe the thermal damage that may occur when an electronic device is subjected to a current or voltage that is beyond the specification limits of the device.

EOS Damage

The thermal damage is the result of the excessive heat generated during the EOS event. The heat is a result of resistive heating in the connections within the device. The high currents experienced during the EOS event can generate very localized high temperatures even in the normally low resistance paths. The high temperature causes destructive damage to the materials used in the device's construction.

An EOS event can be a momentary event lasting only milliseconds or can last as long as the conditions persist.

ESD and EOS are related types of over stress events but at opposite ends of a continuum of current/voltage/time stress conditions.

ESD is a very high voltage (generally >500V) and moderate peak current (~1A to 10A) event that occurs in a short time frame (generally <1μs).

EOS is a lower voltage (<100V) and large peak current (>10A) event that occurs over longer time frame (generally >1ms).

Latch-up can create EOS damage if the current is large and/or if it persist over a long time period.

3. Latch-up:

Due to the structure of the CMOS integrated circuit, a bipolar type parasitic transistor circuit will be constructed in the integrated circuit. Since it has the same structure as the thyristor, an external surge can trigger this thyristor, and an extremely large current will continuously flow. This is referred to as "latch-up". As a result, the integrated circuit may operate abnormally or may be damaged. In this way, latch-up causes great problems in practical use. Since integrated circuits have been further miniaturized recently, these circuits are easily affected by parasitic devices. Latch-up, therefore, is one of the significant problems that should be considered in designing the CMOS integrated circuits.

Latch-mechanism :

Figure 3.76 shows the cross section of a CMOS inverter (P well-CMOS) consisting of parasitic bipolar transistors. The equivalent circuit using such parasitic transistors (lateral PNP transistor and vertical NPN transistor) is the same circuit as that of the PNPN structure thyristor. If the CMOS circuit is operating properly, this thyristor is in the high impedance status. However, if the thyristor is triggered by a factor, the impedance will be rapidly reduced to low impedance, and a large current will flow between the VCC and the VSS. This current will continuously flow until the power supply voltage drops below the holding voltage (holding current) of the thyristor. The factors that can trigger the thyristor are as follows:

1) Breakdown caused by an extremely large reverse bias applied between VCC and VSS (P well-N sub junction shown in the figure).
2) Application of external noise or surge to the input/output terminal.
3) Flow of displacement current caused by rapid change in the power supply voltage.
4) Flow of abnormal current in the substrate, well, etc. caused by irradiation of a radioactive ray, such as α ray.

Among these factors, factor 2) causes most of the problems in practical use.

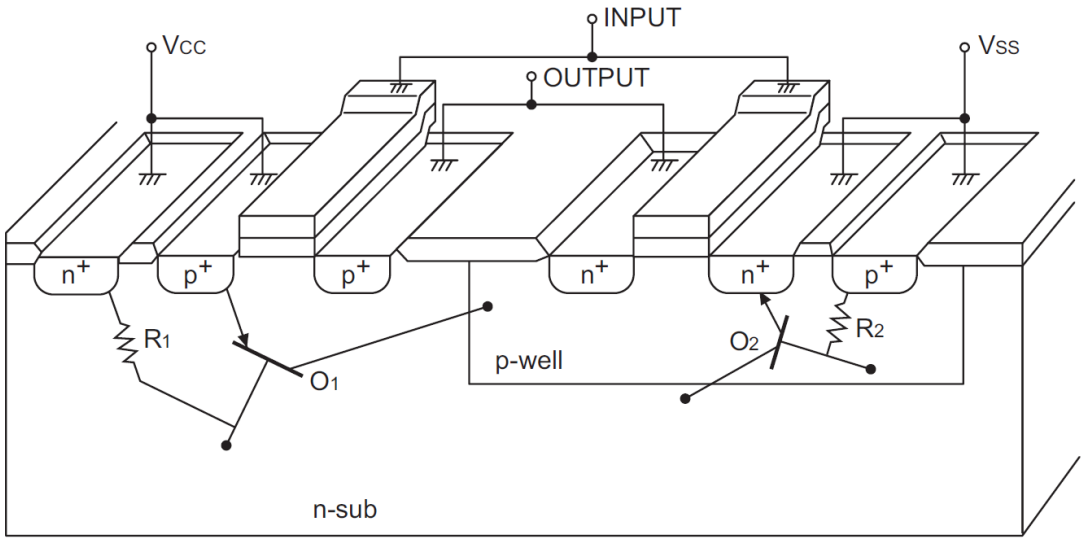


Figure 3.76 Structure of CMOS inverter

TIME-DEPENDENT ELECTRICAL FAILURE MECHANISMS:

1. **Time dependent dielectric breakdown (TDDB) :**
   As integrated circuits are miniaturized, the gate oxide films are becoming extremely thin, and in these oxide films, the electric field strength is getting ever stronger. Oxide film breakage is caused by either an initial defect or deterioration of the oxide film. The former breakage will result in an early failure, and the latter breakage will result in a long-term reliability failure. It is generally said that the true withstand voltage against dielectric breakdown is 10 MV/cm for oxide films. For this reason, when the electric field applied to an oxide film exceeds this dielectric breakdown withstand voltage, the oxide film may be broken. However, even if an oxide film is put to practical use in an electric field of 2 MV/cm to 5 MV/cm (low enough compared with the dielectric breakdown withstand voltage of oxide films), continuous application of such a low electric field for a long time may also cause breakage as time elapses. This type of breakage is referred to as a time dependent dielectric breakdown (TDDB).

2. **Electro-migration :**
   Electric current flowing to a conductor may move metal ions. This phenomenon is referred to as Electromigration. If Al wire is used, Al ions will move in the same direction as the electron flows, and finally voids may be generated on the cathode side and the problem of open circuit failures may be caused. On the anode side, hillocks and whiskers may grow, and in the worst case, short circuit may occur. Electromigration is one of diffusion phenomena that can be caused by interaction between metal atoms in a conductor and electrons that pass through the conductor. Metal atoms in a conductor are heat-vibrated in the energy potential well. If the energy of an atom is increased and exceeds a certain point, the atom will be released from the energy potential well to move freely (to become a free atom). Such self-diffusion, however, just causes rearrangement among metal atoms, and no change can be seen from the macro point of view. As shown in Figure 3.18, interaction between free atoms and current (electrons)

can finally move the atoms. When the current density is in the range of 105 A/cm2 to 106 A/cm2, Al atoms will be diffused into the crystal lattice or the grain boundary by exchanging the momentum with free electrons. Figure 3.19 shows an example of electromigration phenomenon. When generation of voids is started, the cross-section area of the conductor will be reduced, but the current density will be further increased. In addition, the temperature will rise due to the Joule heat, etc., and growth of the voids will be further accelerated. Finally, disconnection will occur.

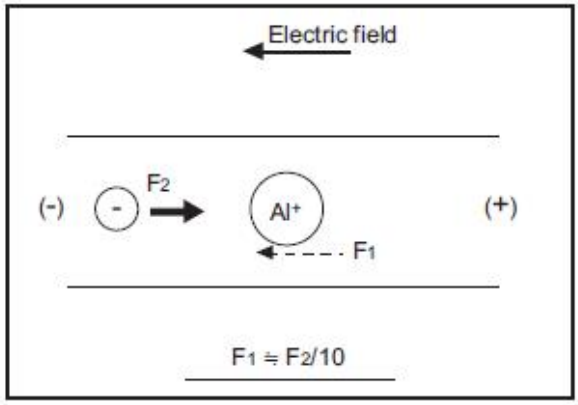


Figure 3.18 Force acting between metal atoms

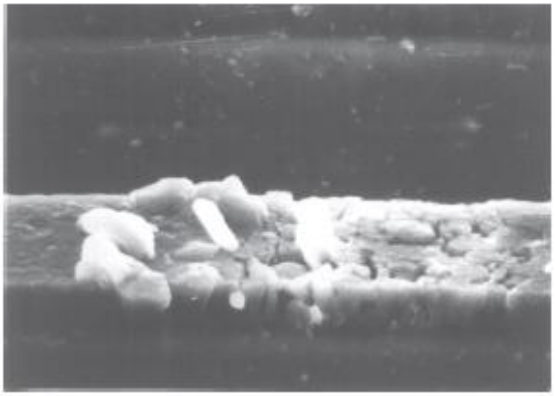


Figure 3.19 Example of electromigration phenomenon

The following formula is generally used for expression of the mean time to failure due to electromigration:

$MTTF = A\ J^{-n} \exp(Ea/kT)$

where, MTTF : Mean time to failure

A : Constant of wire , J : Current density (A/cm2), n : Constant, Ea : Activation energy (eV), k : Boltzmann constant (eV/K) , T : Absolute temperature of wire (K)

It is reported that the "n" value is in the range of 1 to 3, and the "Ea" value is in the range of 0.5 eV to 0.7 eV.

The following factors can reduce the failures caused by electromigration:

a) Crystal structure (grain diameter, crystal orientation, etc.)

b) Addition of other elements to metal film

c) Laminated wiring structure