Experiment Number	1
Aim	Draw and simulate layout for the CMOS inverter. Carry out static as well as transient simulation. Analyze CMOS inverter for i) $(W/L)_{pmos}>(W/L)_{nmos}$ ii) $(W/L)_{pmos}=(W/L)_{nmos}$ iii) $(W/L)_{pmos}<(W/L)_{nmos}$. Do parasitic extraction. Feed these parasitic in circuit simulator (LT Spice) and do layout versus schematic verification.
Apparatus Required	PC loaded with Microwind Tool, LTSpice

Circuit Diagram and Stick diagram with Truth table on the blank side

Theory:

Introduction to Microwind:

The MICROWIND program allows the student to design and simulate an integrated circuit at physical description level. The package contains a library of common logic and analog ICs to view and simulate. MICROWIND includes all the commands for a mask editor as well as original tools never gathered before in a single module (2D and 3D process view, VERILOG compiler, tutorial on MOS devices). You can gain access to Circuit Simulation by pressing one single key. The electric extraction of your circuit is automatically performed and the analog simulator produces voltage and current curves immediately.

Features

1) Handles both conventional pattern based logic simulation and onscreen moves dries simulation.
2) Supports hierarchy logic design
3) Current and power consumption analysis
4) Generation of a voltage description of schematic for layout design
5) Immediate access to symbols for layout design
6) Modes & assembly support of 8051 PIC16F84
7) Sub mirror, deep sub mirror nanoscale technology supported by huge symbol library

CMOS Inverter:

CMOS uses complementary and symmetrical pairs of p-type and n-type metal oxide semiconductor field effect transistors (MOSFETs) for logic functions. Two important characteristics of CMOS devices are high noise immunity and low static power consumption. Significant power is only drawn while the transistors in the CMOS device are switching between on and off states.

The CMOS inverter forms the basis of most static CMOS logic design. More complex logic can be designed from it by simple thumb rules. A common (though not universal) design requirement is symmetric charge and discharge behaviour and equal noise margins for high and low logic values. This requires matched values of Kn and Kp and equal values of VTnand VTp. For a constant load capacitance, rise and fall times depend linearly on Kn and Kp. Thus it is a straightforward calculation to determine transistor geometries if speed requirements and techno- logical parameters are given. However, as transistor geometries are made larger, self loading can become significant.

Procedure	1. Draw the circuit diagram and stick diagram of CMOS Inverter 2. Draw the layout according to lambda based design rules in microwind tool.

	3. Simulate the design and observe I/P and O/P waveforms 4. Extract parasitic capacitance from the spice netlist of layout and feed in circuit simulator (LTSpice). 5. Observe the VTC curve in LTSpice for the following cases: i) $(W/L)_{pmos}>(W/L)_{nmos}$ ii) $(W/L)_{pmos}=(W/L)_{nmos}$ iii) $(W/L)_{pmos}<(W/L)_{nmos}$.
Conclusion:	