Experiment Number	2
Aim	Draw and simulate layout for the following circuits. a. CMOS NAND b. CMOS NOR
Apparatus Required	PC loaded with Microwind Tool, LT-Spice

Circuit Diagram and Stick diagram with Truth table on the blank side

Theory:

CMOS NAND :

CMOS implementation of a two-input NAND gate consist of pull-down sub-circuit made of a series combination of two nMOS transistors. These are responsible for conducting logic '0' to the output node when both of the gates are at logic '1'. The pull-up path on the other hand consists of a parallel combination of two pMOS transistors. If either of the logic is `0', the output node assumes the value `1'.

CMOS NOR:

CMOS implementation of a two-input NOR gate consist of pull-up sub-circuit made of a series combination of two pMOS transistors. These are responsible for conducting logic `1' to the output node when both of the gates are at logic `0'. The pull-down path on the other hand consists of a parallel combination of two nMOS transistors. If either of the logic is `1', the output node assumes the value `0'.

Euler's Theory:

The Euler path is defined as an uninterrupted path that traverses each edge (branch) of the graph exactly once. It is a simple method for finding the optimum gate ordering .

For a given complex CMOS logic gate : find a Euler path in the pull down graph and an Euler path in the pull-up graph with identical ordering of input labels; i.e. find a common Euler path for both graphs.

Procedure	1. Draw the circuit diagram and stick diagram of 2 I/P CMOS NAND & NOR gate. 2. Draw the layout according to lambda based design rules in microwind tool. 3. Simulate the design and observe I/P and O/P waveforms Extract parasitic capacitance from the spice netlist of layout..
Conclusion:	