Experiment Number	4
Aim	Draw and simulate layout for the given equation $\overline{AB + AC + AD}$ with the static CMOS design style
Apparatus Required	PC loaded with Microwind Tool

Circuit Diagram and Stick diagram on the blank side

Theory:

Static CMOS Design Style:

The most common design style in modern VLSI design is the Static CMOS logic style. In this, each logic stage contains pull up and pull down networks which are controlled by input signals. The pull up network contains p channel transistors, whereas the pull down network is made of n channel transistors. The networks are so designed that the pull up and pull down networks are never 'on' simultaneously. This ensures that there is no static power consumption.

N- and P-channel Networks:
N- and P-channel networks implement logic functions
Each network connected between Output and VDD or VSS
Function defines path between the terminals
Straightforward way of constructing static CMOS circuits is to implement dual N- and P- networks
Duality sufficient for correct operation (but not necessary)
For pull down networks AND expressions are implemented using series connection of n transistors and OR expressions are implemented using parallel connection of n transistors
Static CMOS implementation uses total 2N no. of MOSFETS for N inputs.

Procedure	1. Draw the circuit diagram and stick diagram of given expression 2. Draw the layout according to lambda based design rules in microwind tool. 3. Simulate the design and observe I/P & O/P waveforms.
Conclusion:	