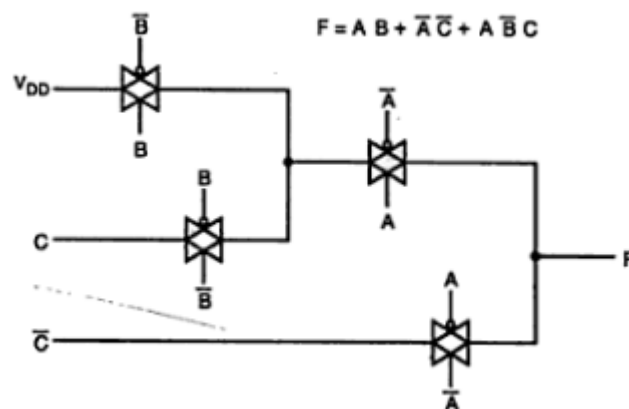


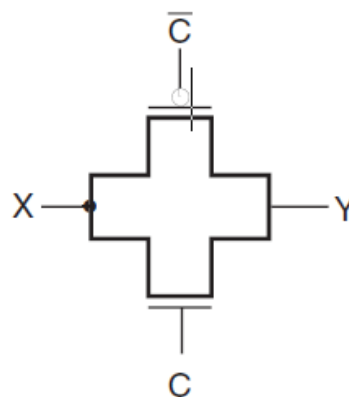
<b>Experiment Number</b>	5
<b>Aim</b>	Draw and simulate layout for the given equation $F = AB + \bar{A}\bar{C} + A\bar{B}C$ with Transmission gate(TG) design style
<b>Apparatus Required</b>	PC loaded with Microwind Tool

Circuit Diagram and Stick diagram on the blank side



**Theory:**

A transmission gate is used as an electronic switch for making a connection between two points in a circuit. It consists of an n-channel transistor and a p-channel transistor in parallel, as shown in Fig. The two types of transistor are used because the p-channel transistor passes 1 (H) well and the n-channel transistor passes 0 (L) well. The fig given is the switch model for the transmission gate. Here X is the input, Y is the output, and the two terminals C and C-bar are control inputs. If C=1 (H) and C-bar=0 (L), there is a path between X and Y for the signal to pass through. If C= 0 and C-bar=1, there is no path, and the circuit behaves like an open switch. Transmission gates are particularly useful for performing selection functions



In TG logic design conducting TG network (low impedance path) should always be provided between the output node and one of the inputs, for all possible input combinations. This is to make sure that the output node with its capacitive load is never left in a high impedance state.

If each CMOS transmission gate in TG logic circuits is realized with full nMOS-pMOS pair, the disjoint n-well structures of the pMOS transistors and the diffusion contacts may cause a significant overall area increase. To reduce silicon area occupied by TG circuits, the transmission gates can be laid out as separated nMOS-pMOS pairs with all pMOS transistors placed in one single n-well. However the routing area required for connecting the p-type diffusion regions to input signals must be carefully considered.

<b>Procedure</b>	<ol style="list-style-type: none"><li>1. Draw the circuit diagram and stick diagram of given expression</li><li>2. Draw the layout according to lambda based design rules in microwind tool.</li><li>3. Simulate the design and observe I/P &amp; O/P waveforms.</li></ol>
<b>Conclusion:</b>	