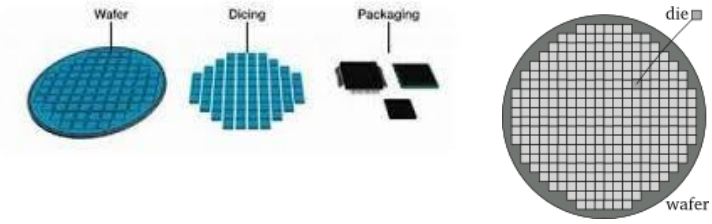
IC Packaging

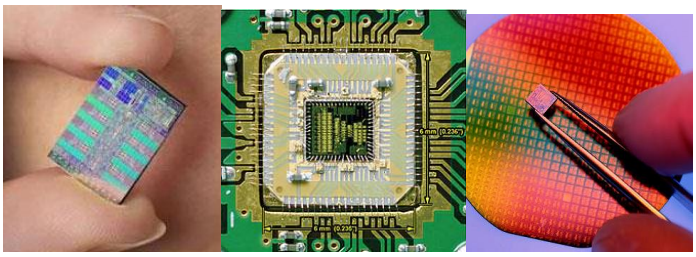
- Purposes
  1) Electrical connections
     - Signals
     - Power and ground
  2) Aids heat dissipation
     - Increase effective surface area for increased convection
     - Heat conduction into PC board
  3) Physical protection for IC
     - e.g., against breakage
  4) Environmental protection
     - Hermetic (airtight) seal
     - e.g., against corrosion or moisture

Integrated Circuit (IC) Packages

1958 – First IC invented – one transistor
Today – Intel Pentium has roughly 3.1 x 10^6 transistors

- **As Semiconductor devices become more complex – the interconnections from the die to the circuit hardware keep evolving.**
- **Devices with high clock rates** and **high power dissipation**, or with **multiple die** , are leading to various **new pacakges.**
- A **die** in the context of **integrated circuits** is a small block of semiconducting material, on which a given **functional circuit is fabricated**.





- Typically, integrated circuits (ICs) are produced in large batches on a **single wafer** of electronic-grade silicon (EGS) or other semiconductors through manufacturing processes steps
- **The wafer is cut ("diced") into many pieces, each containing one copy of the circuit.** Each of these pieces is called a **die**.
- These will be packaged in a suitable package or placed directly on a **PCB substrate** as " **bare die**".
- A DIE is the actual silicon chip (IC) that would normally be inside a package/chip. Their just a piece of the wafer disk, **but instead of being mounted and connected in a 'chip', and covered with epoxy.**

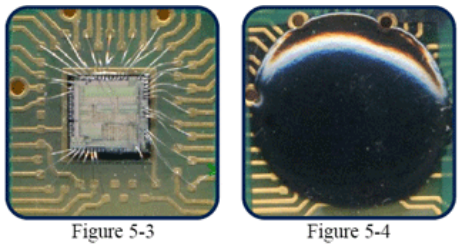
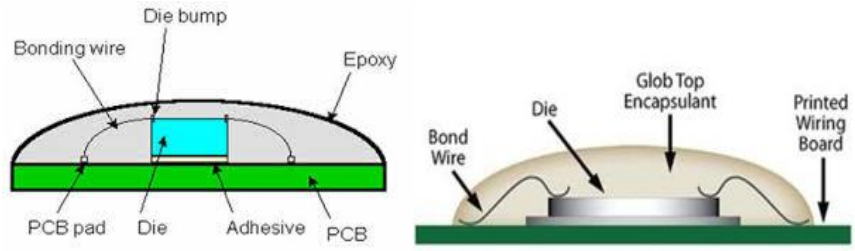


Figure 5-3 Figure 5-4

- The left image shows the **die directly mounted on the PCB**, with the **bond wires** connected to the **copper traces.** The right image shows the **protective epoxy coating** applied after the connections have been made.
- **A bare die may be mounted in integrated circuit packaging for ease of handling and testing, ready to be soldered to a printed circuit board.**



Reasons To Use Bare Die:

- Smaller Size and Weight - Using bare die can allow for reduced board space.
- **Operating Temperature Size** - Package thermal characteristics no longer inhibit the performance of the die or the environments where they can operate.
- **Ruggedness** - Direct die attach and wirebond provides protections against high levels of shock and vibration.
- **Lighter Weight** - Smaller designs and higher densities reduce weight and size of your application.
- **More Efficient Performance** - Removing extra package interconnect can reduce capacitance and inductance.

- **Reliability** - The reduced number of interconnects with die use leads to improved reliability. The typical packaged part has three connection points per I/O.
- **Electrical Performance** - The lower inductance and capacitance of bare die is important in analog, RF, and power applications. Faster signal flight time (lower propagation delay) and improved power/ground distributions.
- **Hermetically Sealing** - Air tight sealed packages can be selected that can be injected with inert gasses.

- **These die advantages promote higher levels of integration, improved electrical and reliability performance, and increased functionality per square area.**
- The **availability of IC products in die form** gives customers a convenient option for small-footprint designs, enabling them to optimize their product designs for limited space and to implement innovative, proprietary packaging solutions.
- **Using Bare die is not without problems, including testing issues and cost .**At this time it more costly for vendors to handle and ship bare die than packaged devices .
- Using bare parts makes it important to use **known good die (KGD) ;** otherwise, the final assembly has to be scrapped as the device cannot be removed.

IC Packaging can be divided into the following categories :

1. Surface mount packages (plastic or ceramic)

2. Chip-scale packaging

3. Bare die

4. Through hole packages

5. Modules assemblies

There are many different types of IC packages, each of which has **unique dimensions, mounting-types, and/or pin-counts.**

1. **Dual In-line Packages [DIP], or Dual In-Line [DIL**] packages are packages with two rows of leads on two sides of the package. **DIP ICs may be through-hole [PDIP or CERDIP] or SMT package [SOJ or SOIC].**

2. **Quad Flat Packs or Chip** Carriers are **square packages** [or nearly square], with leads on all four sides. Examples :**PLCCs** and other variants are strictly Surface Mount Technology (SMT).

3. **Grid Arrays** are those type packages that have their pins arranged in a grid. The **pin grid** may consist of **Leads, pads, or solder balls** on an area array.
   The **through hole variant** is called a **PGA**, while the **SMT variant** might be called **LGA or BGA.**

Mounting Style

One of the main distinguishing package type characteristics is **the way they mount to a circuit board**. All packages fall into one of two mounting types: **through-hole (PTH) or surface-mount (SMD)**

Through-hole packages are generally bigger, and much easier to work with. They're designed to be stuck through one side of a board and soldered to the other side.

Surface-mount packages range in size from small to minuscule. They are all designed to sit on one side of a circuit board and be soldered to the surface.

Some Standard IC Packages : DIP , TO (Transistor Outline)

Plastic surface mount packages result in a device that is **light , small , able to withstand physical shock and g forces and inexpensive** due to one step manufacturing process.

Issues with Plastic Packages :

Plastic parts shipped in sealed bags with ***desiccant*** (a hygroscopic substance that absorbs water. It is most commonly used to remove humidity that would normally degrade or even destroy products sensitive to moisture) are **designed for 12 month storage**.

Parts stored longer than 12 months storage , especially ***" Plastic quad flatpack (PQFP)"*** packages devices , should be**bakedto remove moisture** that has entered the package.

Plastic packages are hydroscopic and absorb moisture to a level dependent on the storage environment.

Danger !!

This moisture can vaporize during rapid heating , such as in a solder reflow process, and these stresses can cause *package cracking* (known as ***popcorn effect***) .

Subsequent high temperature and moisture exposures can allow contaminants to enter the IC and cause **failure** at a later time due to corrosion. So there is a need for different packages to handle such extreme cases.

Hermetic packages such ***as ceramic leadless chip carriers (CLCCs)*** are used in harsh applications (such as military and space applications) where water vapor and contaminants can shorten the life of the device.

Application : they are used in mission-critical communication , navigation and avionics systems.

Metal Vs Ceramic Vs Plastic packages

Metal packages with glass seals , provides **highest level of hermetic sealing** followed by glasses and ceramic .

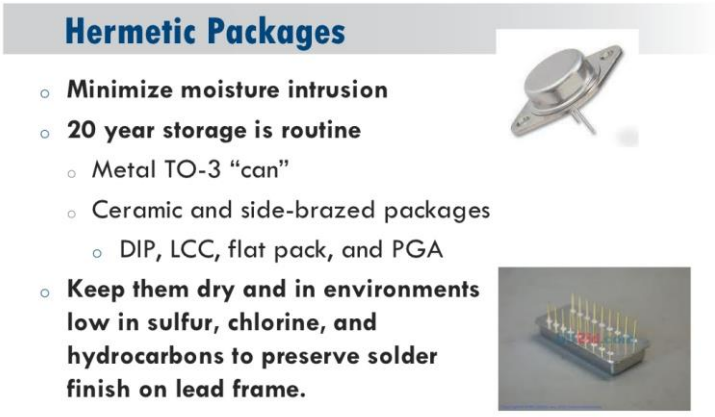
These packages have a higher temperature range than plastic encapsulated parts (typically from -55 ° C to + 125 ° C Vs 0 to 70 ° C, for plastic packages)

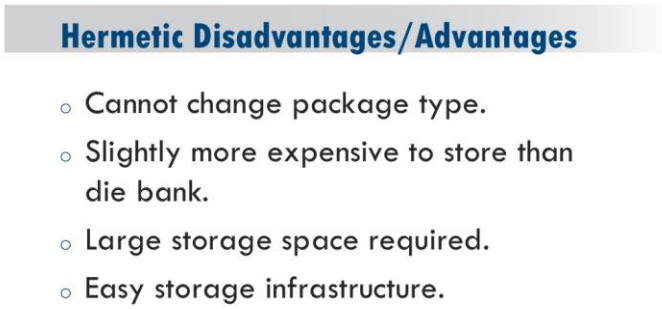
Note :**Aluminum oxide** , is the most commonly used ceramic material , has a thermal conductivity less than plastic packages device.

In a **ceramic sealed device**, the circuit die does not come in contact with the ceramic packaging material .Thus , temperature cycling will not affect the die , and the parts can withstand thousands of temperature cycles (1000 of temperature cycles means 20 years use on a commercial airline)

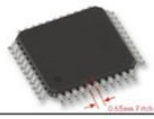
Large die plastic encapsulated parts can fail after only 250 temperature cycles

Drawback of Ceramic packaged device : More complicated manufacturing process , high cost, limited availability .



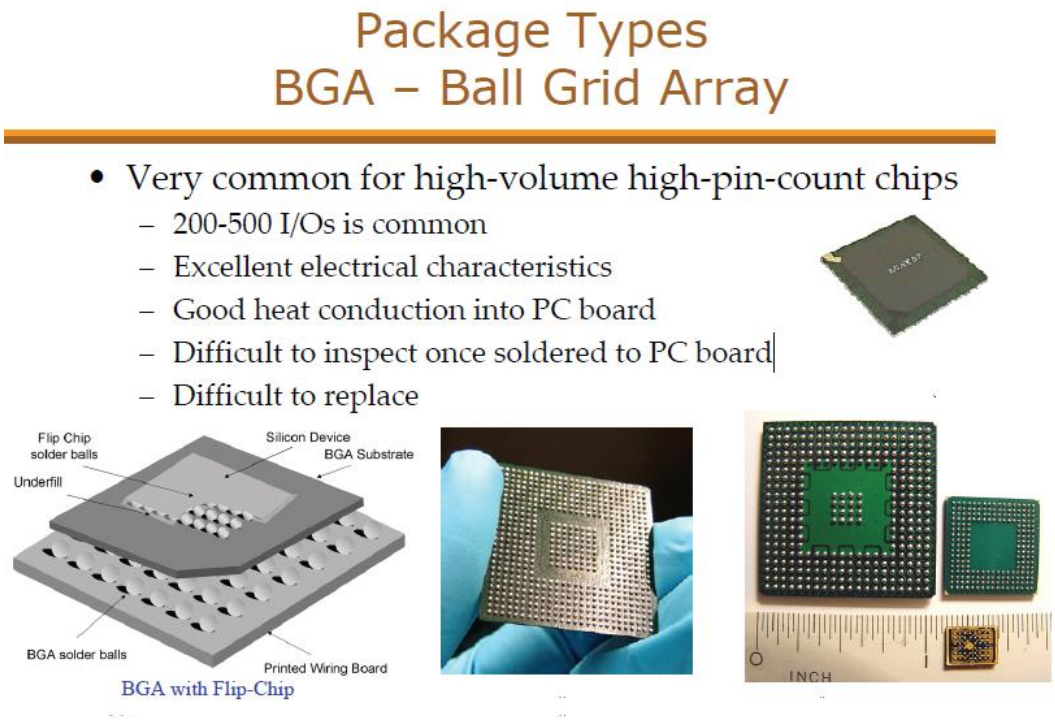


Surface Mount (SMD) Packages

	SOIC - 8 pins
	TQFP - 44 pins
	resistor
	capacitor
	inductor
	diode

Surface-mount packages range in size from small to minuscule. They are all designed to sit on one side of a circuit board and be soldered to the surface.

Surface mount packages types



Ball grid array (BGA)

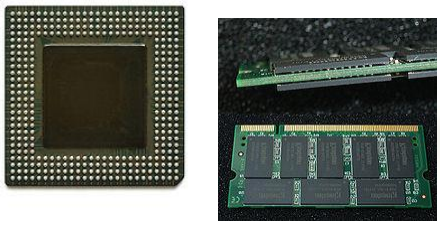


Fig :256 pin perimeter BGA

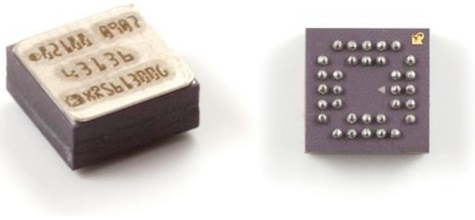


Fig : BGA ICs assembled on a PCB

- Packaging technique developed by IBM.
- A ball grid array (BGA) is a type of surface-mount packaging (a chip carrier) used for integrated circuits.
- In a BGA the ***pins are replaced by pads on the bottom of the package, each with a tiny solder balls stuck to it.***
- The device is placed on a PCB with copper pads in a pattern that matches the solder balls.
- Here , leads , or pads are replaced by solder balls that replace high pin count **Quad flatpacks (QFPs)**
- The **whole bottom surface** of the device can be used, instead of just the perimeter.

Advantages :

- **High package density.**
- **Better Heat conduction :** A further advantage of BGA packages over packages with discrete leads (i.e. packages with legs) is the **lower thermal resistance between the package and the PCB**. This allows heat generated by the integrated circuit inside the package to flow more easily to the PCB, preventing the chip from overheating.
- **Low-inductance leads** : BGAs, with their very short distance between the package and the PCB, have **low lead inductances,** giving them superior electrical performance to pinned devices.

Disadvantages :

- **Difficulty of inspection : Solder connections cannot be visually inspected** (requires X-ray BGA inspection)
- **Removed** parts cannot be reused (the solder balls are melted)
- **Expensive equipment** is required to reliably solder BGA packages; hand-soldering BGA packages is very difficult and unreliable.
- **Noncompliant connections**

BGA package versions :

1) **Perimeter lead BGA**
2) **CBGA**: **Ceramic Ball Grid Array**
3) **PBGA: Plastic Ball Grid Array**

- PBGA is a surface mount package, made of plastic, that uses solder balls to attach to the Printed Wiring Board [PWB] or BGA socket.

- PBGA lends itself to the most advanced available assembly processes and designs for low cost, high performance applications.
- The combination of high speed and high power advantages offered by PBGAs make them the first choice for deployment of mixed signal (analog and digital) or mixed semiconductor (CMOS and bipolar) technologies in a single package, in devices such as ASICs, and FPGAs/CPLDs (programmable logic), among others.

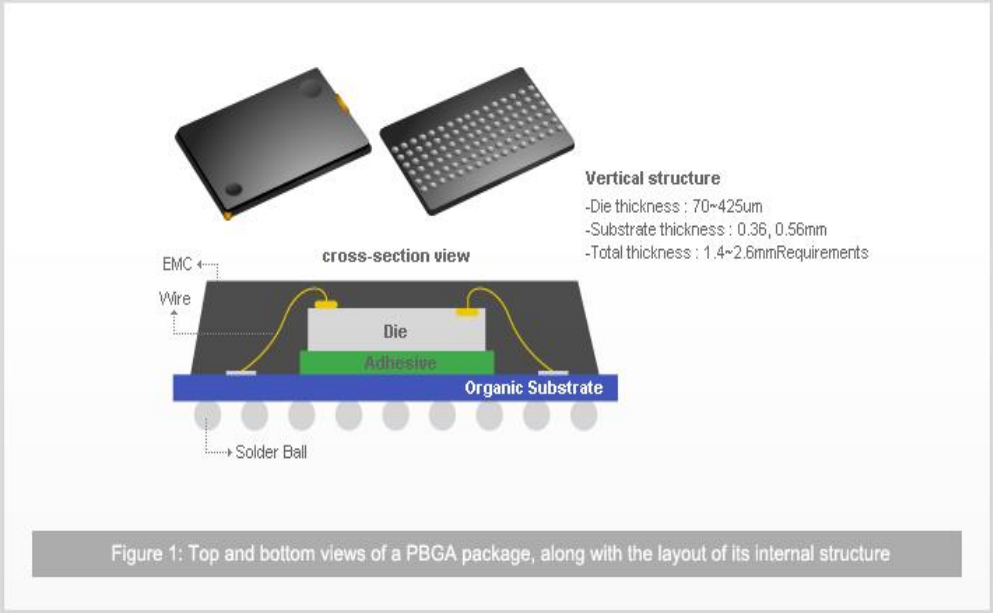


Figure 1: Top and bottom views of a PBGA package, along with the layout of its internal structure

Application

PBGAs find widespread applications in devices across multiple segments. Some of these applications are listed below :

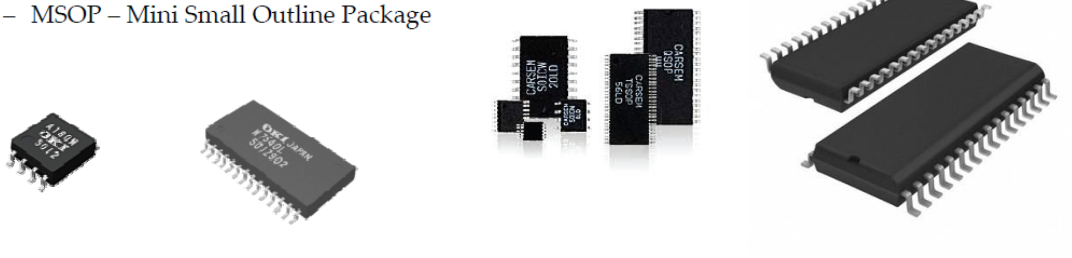
- Devices such as digital televisions, high-end graphics, microprocessors/microcontrollers, DSPs, and chipsets
- High-density memory devices, such as DRAM and flash memory
- Devices with high I/Os (from 200, to more than 1000)
- Devices operating at high frequencies and handling high powers, such as wireless communications base stations, and network servers

Feature

- Wide range of available body sizes, from 17 x 17 mm, to 35 x 35 mm, with ball counts from 208 to more than 1000
- Superior thermal performance (2~3 W) under a wide range of operating conditions and Excellent reliability
- Available in lead- and halogen-free variants (Green Products) making the material for the devices environment-friendly, and easier to recycle and reuse

Package Types
SOP – Small Outline Package

- SOP includes a large family of packages
  - SOIC – Small Outline Integrated Circuit
  - SSOP – Shrink Small Outline Package
  - QSOP – Quarter-size Small Outline Package
  - TSSOP – Thin Shrink Small Outline Package
  - MSOP – Mini Small Outline Package



- SOIC packages are the **surface-mount cousin** of the **DIP**.
- It's what you'd get if you bent all the pins on a DIP outward, and shrunk it down to size.
- Easiest SMD parts to hand solder.
- SOP package is a lead frame based package with gull-wing type leads, which are drawn out from the two sides of the package body.
- SOP package is suitable for memory module, portable consumer products, cell phones and office appliances, etc.
- On SOIC packages, commonly 0.05" (1.27mm) pin spacing.
- The SSOP is an even smaller version of SOIC packages.
- Other, similar IC packages include TSOP (thin small-outline package) and TSSOP.
- Single-task-oriented ICs like the MAX232 or multiplexers come in SOIC or SSOP forms.

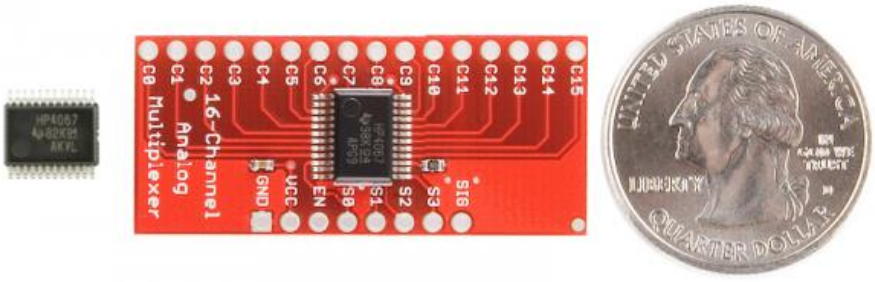
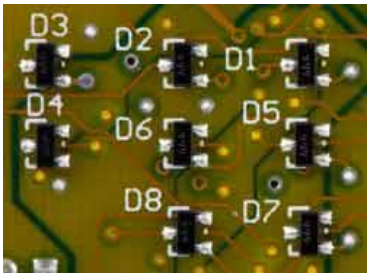


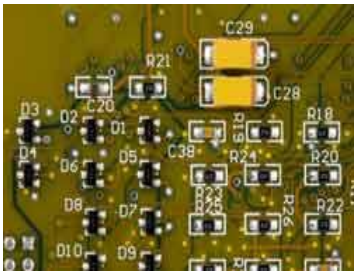
Fig :A 16-Channel Multiplexer (CD74HC4067) in a 24-pin SSOP package. Mounted on a board in the middle (quarter added for size-comparison).

Other SOP versions :

Small Outline large (SOL)



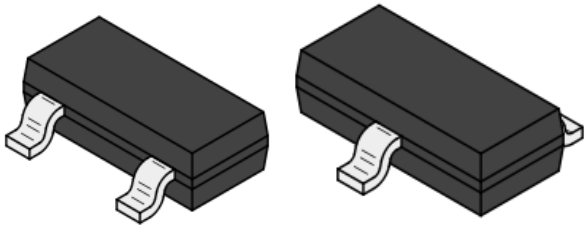
SMD diodes on a printed circuit



SMD diodes and transistors on a PCB

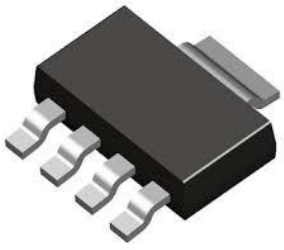
Small Outline transistor (SOT) :

- A plastic leaded package for diodes and transistors
- SOT-23 Body style Transistor or FET SMD package
- The SOT-23 package is a 3-terminal plastic surface mount component.
- A similar package style is the TO-236AA SMD Transistor.



SOT 23

- Because the SOT-23 is a Surface Mount Device [SMD] heat transfer will also be conducted via the component leads.
- **SOT-23 - Small Outline Transistor**: This is SMT package has three terminals for a diode of transistor. It measures 3 mm x 1.75 mm x 1.3 mm.
- **SOT-223 - Small Outline Transistor**: This package is used for higher power devices. It measures 6.7 mm x 3.7 mm x 1.8 mm. There are generally four terminals, one of which is a large heat-transfer pad.

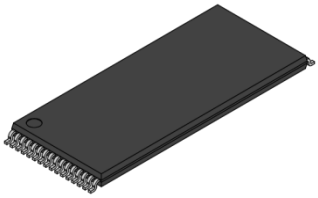


SOT 223

Package Types
TSOP – Thin Small Outline Package

- One of the smallest packages available
- Type I – leads on short sides

- Type II – leads on long sides

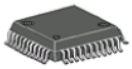


TSOP and TSSOP Package :

- TSOP (Thin Small Outline Package)
- TSSOP (Thin Shrunk Small Outline Package)

Package Types
QFP – Quad Flat Package

- Common in modern electronics



- TQFP – Thin Quad Flat Package
  - Typical thickness 1.4 mm

Quad Flat Packages(QFP)

- Oldest Surface mount packages , used mainly on military programs.
- QFP package is a flat structure with 4-sided peripheral leads which provides medium high pin counts (< 256 leads). QFP package is often used for SRAM, graphic processors, PC Chipsets, digital signal processors, multi-media and other related devices.

- A Quad Flat Pack IC is a surface mount component that contains pins, on each side of the body.
- QFP ICs might have anywhere from eight pins per side (32 total) to upwards of seventy (300+ total).
- Many microprocessors, sensors, and other modern ICs come in QFP or QFN packages
- Smaller variants of the standard QFP package include thin (TQFP), very thin (VQFP), and low-profile (LQFP) packages.

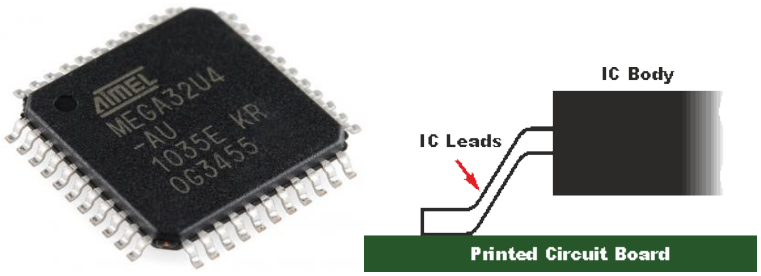


Fig : The ATmega32U4 in a 44-pin (11 on each side) TQFP package.Quad Flat Package, QFP lead arrangement

- Thin (TQFN), very thin (VQFN), and micro-lead (MLF) packages are smaller variations of the standard QFN package. There are even dual no-lead (DFN) and thin-dual no-lead (TDFN) packages, which have pins on just two of the sides.

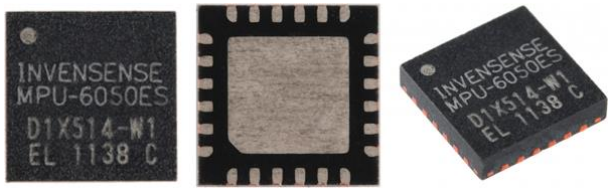


Fig : The multitalented MPU-6050 (a tiny accelerometer/gyroscope) IMU sensor comes in a relatively tiny QFN package, with 24 total pins hiding on the bottom edge of the IC.

Thin Quad Flat Pack IC Package

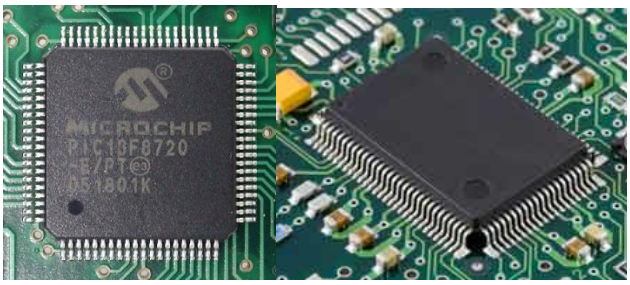


Fig :80 pin TQFP IC Package shown mounted on a PCB

- A **Thin Quad Flat Pack device** is a surface mount component that has it's pins 'leads' folded out from its body in the shape of a '**L**'. The type of lead is called a **Gull-Wing terminal** [shape].
- The TQFP IC package is similar to the surface mount [Dual In-line] SOIC device because both packages use a gull-wing shaped lead.
- The difference between the two is that a SOIC package has leads on two sides of the package and a TQFP has leads on all four sides.

Quad flat package variants

BQFP - Bumpered Quad Flat Pack: This form of quad flat package has extensions at the four corners to protect the leads against mechanical damage before the unit is soldered.

Fig :Bumpered quad flat pack

CQFP - Ceramic Quad Flat Pack: This is a high quality version of the quad flat pack using ceramic for the package.

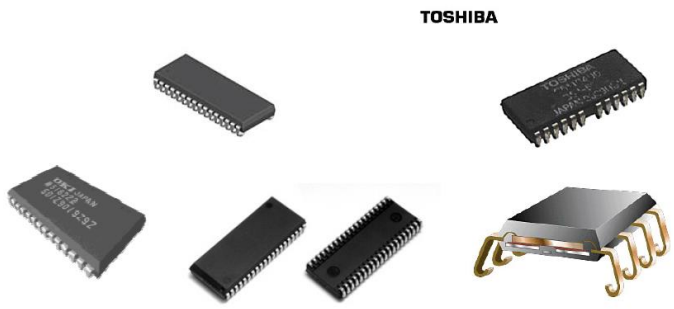
FQFP - Fine pitched Quad Flat Pack: A quad flat pack with, as the name indicates, a fine pitch for the pins.

HQFP - Heat sinked Quad Flat Pack: With many integrated circuits, especially those with high pins counts which have a high level of circuitry may dissipate high levels of heat. This heat may need to be removed. To achieve this a number of the pins, often in the centre of opposing sides are replaced with a thicker pin which is soldered to a large pad on the PCB with a large area of copper connected to it. This will remove a significant amount of heat.

PQFP - Plastic Quad Flat Pack: A quad flat pack where the package material is plastic.

Package Types
SOJ – Small Outline J-lead

- "J" leads on two sides



SOJ – Small outline package with J leads on both sides. The leads are bent back around the chip carrier. Easy to solder by hand, infrared and reflow techniques. Commonly used for crystal oscillators.

Fig :Photo of a SOJ-28 package, a variant of the SOIC package with J-type leads.

Note : The term J-Lead defines the pin shape and does not define the physical size or shape of the component body

LCC : Leadless Chip Carrier

- Surface mount device [SMD] that uses surfaces on the side of its body for board attachment and has no leads or legs. A chip carrier has terminals on all four sides of the package.
- All (LCC) package has terminals/pads on all four edges of the package. The lid for this package can be either ceramic or metal "solder sealed".
- This package provides a hermetic environment for the IC inside. These packages enable end products to be reduced in size and weight.
- Exceptional thermal and electrical performance by design

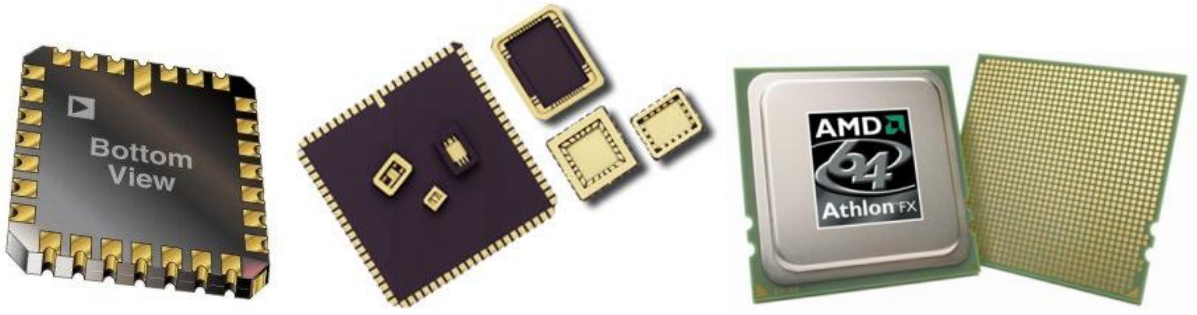
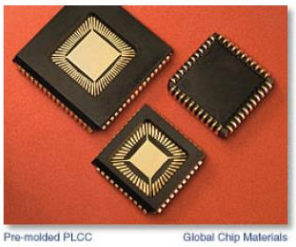


Fig : LCC packages

Package Types
PLCC – Plastic Leaded Chip Carrier

- Also called QFJ – Quad Flat J-lead
- Common in many products



PLCC in socket

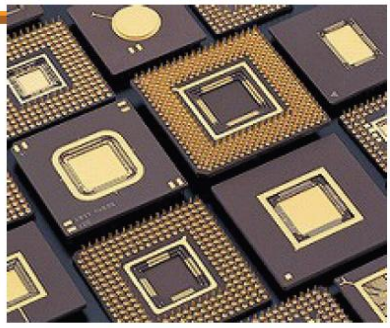
- A surface mount device that uses J-leads on each side of its 4-leaded body for board attachment
- It's common for PLDs and other programmable logic devices, using PLCC packages, to be installed in sockets so they can be removed and re-installed to be programmed.

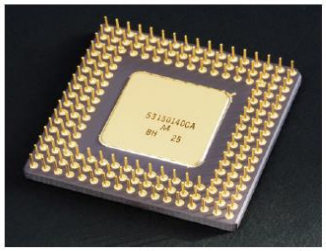
Fig : PLCC Socket

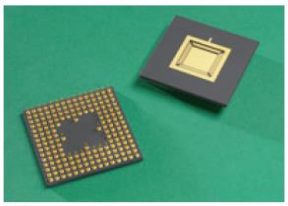
- The graphic above shows an example of a UVEPROM that has a window so the device may be erased.

Package Types
PGA – Pin Grid Array Package

- Material—the main body consists of co-firing multilayer alumina ceramics, and pin terminals made of an alloy of iron, nickel, and cobalt are attached with silver-brazing to the main body.
- 400+ pins possible
- Cavity up
- Cavity down







- In a PGA, the package is square or rectangular, and the pins are arranged in a regular array on the underside of the package.
- The pins are commonly spaced 2.54 mm (0.1") apart
- PGAs are often mounted on PCB using the through hole method or inserted into a socket.
- PGAs allow for more pins per IC than older packages such as DIP.

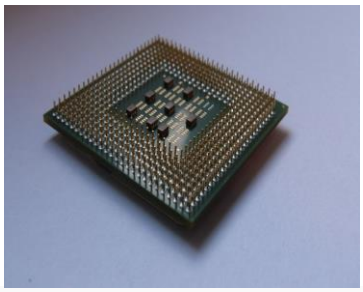


Fig :Underside of a Pentium 4 in a PGA package

Land Grid Array (LGA) package

- **LGA** is a surface mount package that uses pads to attach to solder balls located on the Printed Wiring Board [PWB].
- An LGA package differs from a BGA in that a BGA has the solder-balls attached to the package while an LGA uses solder-balls that are attached to the printed circuit board.
- It is a packaging technology with a square grid of contacts on the underside of a package.

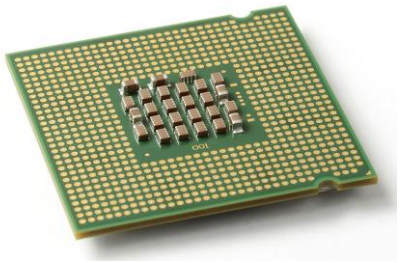


Fig : The LGA 775 package of a Pentium 4 Prescott CPU.

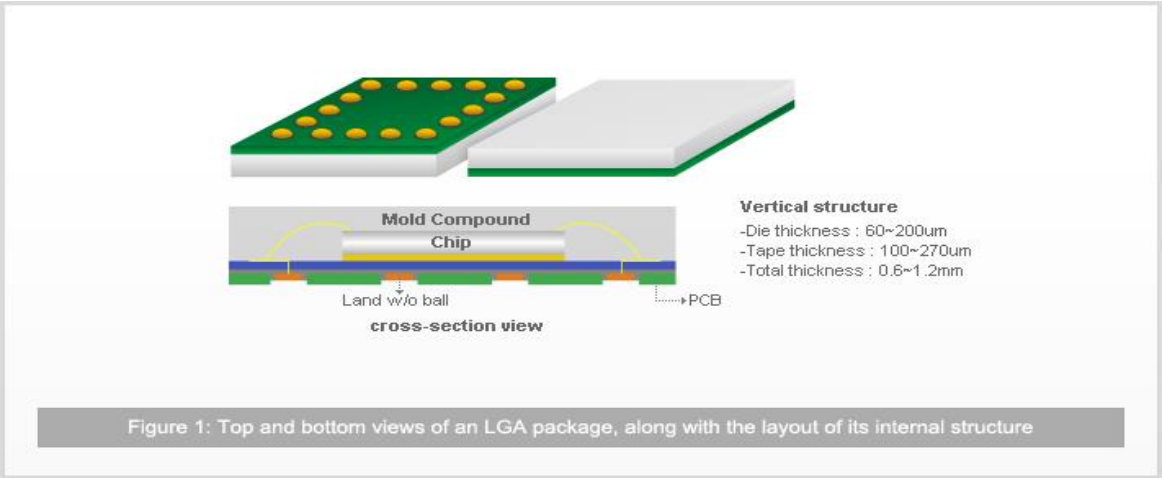


Figure 1: Top and bottom views of an LGA package, along with the layout of its internal structure

- In LGA there are no pins on the chip, in place of the pins are pads of bare gold-plated copper that touch protruding pins on the microprocessor's connector on the motherboard.
- A **Ceramic Land Grid Array [CLGA**] is identical to any LGA package except for the fact that the body of the component is made of ceramic.

Features:

- Wide ball count range, from 8 to more than 600
- Significant improvement in the ***mounting space efficiency*** as detailed below:
  - Reduction in mounting space (std package size: 5 x 5mm)
  - Reduction in mounting height (std thickness: 0.4~1.2 mm)
  - Reduction in package mass
- Superior ***thermal performance*** (1~2 W) under a wide range of operating conditions
- Excellent reliability
- Due to the absence of solder balls, an LGA has ***negligible internal stray parasitic*** elements associated with its external solder pads. This contributes to providing an extremely low thermal resistance to the device, to allow maximum heat transfer from the die to the package pads.
- Available in lead- and halogen-free variants (Green Products) making the material for the devices ***environment-friendly***, and easier to recycle and reuse

Applications

Some of the principal areas of deployment for LGAs include :

1. Compact, space-conscious devices, such as mobile handsets, laptop/tablet computers, and PDAs
2. Devices requiring high levels of integration, and high performance in a small size, such as analog devices (transceivers, amplifiers, and modulators/demodulators), digital logic (ASICs, FPGAs), microprocessors/microcontrollers, and memory (DRAM, flash)
3. Devices requiring high ball counts (more than 600) in a small package
4. Devices expected to handle low to medium power levels (1~2 W), such as wireless transceivers, and disk drives

Chip Scale Packaging

- **It is designed to have the size and performance of bare die parts but with the handling and testability of packaged device.**
- The package size is no more than 1.2 times the original chip i.e here the size of the package is almost the same as the size of the die inside of it.
- Chip scale packaging variations include: flip chip, High Density Interconnect (HDI), Micro Ball Grid Array (µBGA), Micro Surface Mount Technology(MSMT) and Slightly Larger than Integrated Circuit Carrier (SLICC).

1. Flip-chip package :

- Flip chip assembly is the direct electrical connection of face-down (hence, "flipped") electronic components onto substrates, circuit boards, or other components, by means of conductive solder bumps on the chip bond pads.
- These packages have enlarged solder pads (bumps or balls).
- A semiconductor package where the I/O terminations are in the form of bumps on one side of the package (also called bumped chip) .
- After the surface of the chip has been passivated , or treated , it is flipped over and attached to the matching substrate.

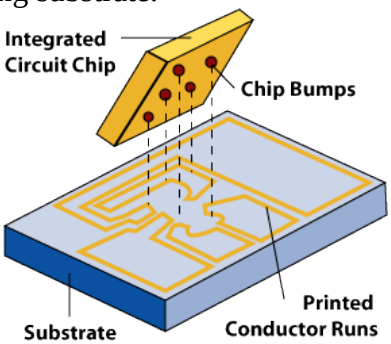


Fig :A flip chip and substrate, shown with the bumped active face of the die to be placed face down upon the matching substrate.

Flip chip has blossomed into today's cell phones, hearing aids, digital cameras, PDA, pagers and many other portable devices. Over the last decade, flip chip has also become the preferred assembly method for hundreds of millions of smart/RFID cards annually.

There are three steps in making a flip chip connection: **putting conductive bumps on the die bond pads**, **attaching the bumped die to matching pads on the board or substrate**, **and filling the remaining space under the die with a protective, electrically non-conductive adhesive**.

The preferred adhesive assembly method for smart cards/RFID goes by the mouth-filling name of "**anisotropic conducting film," or ACF**.

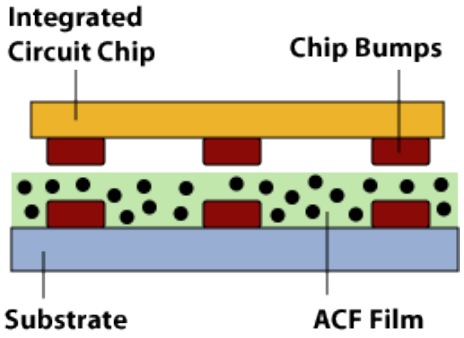


Fig: ACF film before assembly, with the spheres uniformly distributed and making no electrical conducting paths.

In the ACF assembly process, heat softens the film, while pressure forces the die and substrate bond pads together, trapping some conductive spheres between them and breaking through the sphere insulation to form conducting paths from die to substrate pads.

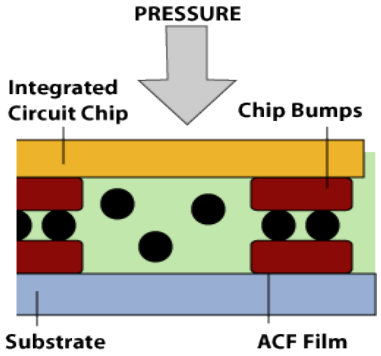


Fig :ACF film after assembly, with the conducting spheres locked between the chip and substrate bond pads.

The non-conducting ACF film also acts as the "underfill" adhesive, filling all of the space under the die to lock together and protect the die and substrate.

Advantages of flip chip assembly

Here the chip sits directly on the circuit board, and is much **smaller than the carrier both in area and height**. The **short wires greatly reduce inductance, allowing higher-speed signals, and also conduct heat better.**

Smallest Size – Eliminating bond wires and cumbersome individual packages reduces the required board area per chip by up to 95% and the height by more than 50%. Weight can be less than 5% of the packaged device weight.

Highest Performance – Because of its small size, flip chip offers the highest speed electrical performance of any assembly method. Eliminating bond wires reduces the delaying inductance and capacitance of the connection by a factor of 10, and shortens the signal path by a factor of 25 to 100. The result is **high speed off-chip interconnection**.

Greatest Connection Flexibility – Flip chip gives the greatest input/output connection flexibility. Flip chip connections can use the whole area of the die, accommodating many more connections on a smaller die, and placing them most efficiently.

Most Rugged – Flip chip is mechanically the most rugged interconnection method. Flip chips, when completed with an adhesive "underfill," are solid little blocks of cured epoxy. They have survived laboratory tests simulating the forces of rocket liftoff and of artillery firing, as well as millions of cumulative total hours of actual use in computers and under automobile hoods.

Lowest Cost – Flip chip can be the lowest cost interconnection for high volume automated production, with costs of a fraction of a cent per connection. This explains flip chip's longevity in the cost-conscious automotive world, and growing popularity in smart cards, RFID cards, cellular telephones, and other cost-dominated applications.

2. Mini-BGA: uses a predetermined grid array for the solder bumps and is similar to flip-chip. The mini-BGA package was designed to be used in a wide variety of applications that require small size, high reliability and low unit cost.

Features:

Body sizes:6 x 8 mm, 8 x 10 mm, 12 x 12 mm , 7 x 9 mm (stacked) and 8 x 11mm (stacked)
Low profile package (total thickness 1.4 mm max.)
Established package infrastructure with standard chip-array BGA footprints
Ball pitch range from 0.75 to 1.0 mm
Ball counts range from 36 to 208 ball

Applications

The mini-BGA package is well suited for long life, high reliability and low-cost applications such as cameras, cellular phone, PDA, notebook computers, personal computers, disk drivers, office equipment, audio and video products and wireless communication products.

3. Micro-surface mount packages (MSMT) :

- In this technology, semiconductors are mass packaged in the wafer state and can be tested as individual devices.
- This package is approximately the same size as the semiconductor die
- It is used for devices less than 200 leads.
- It has lower parasitic inductance than BGA or QFP packages.

4. MicroBGA (µBGA) or Chip-scale packaging :

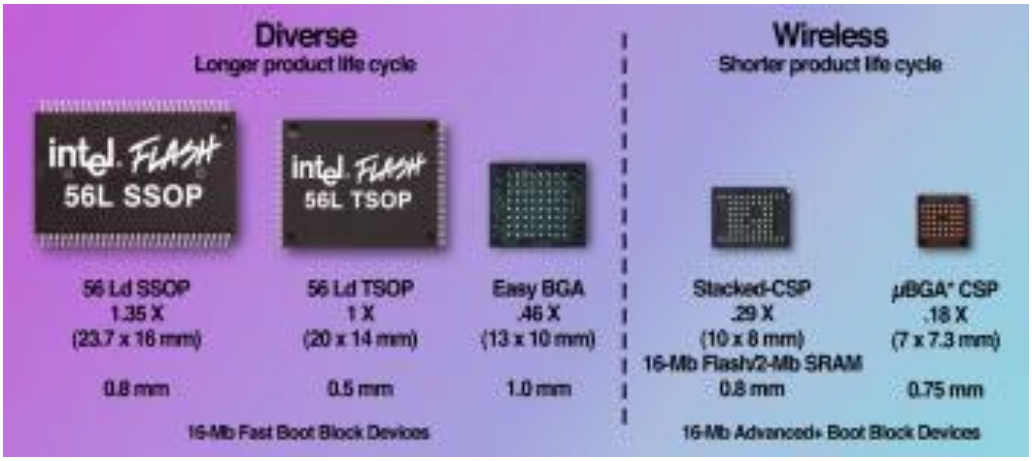
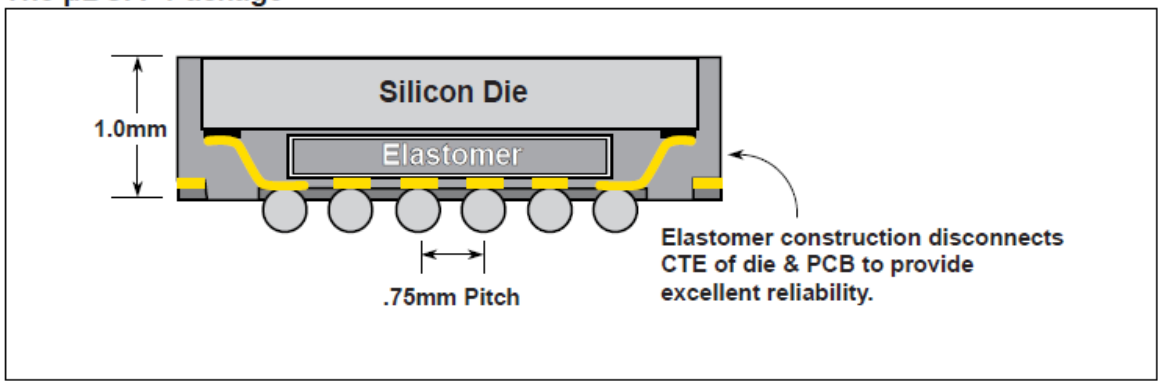


Fig : CSP vs. SOP Size Comparisons

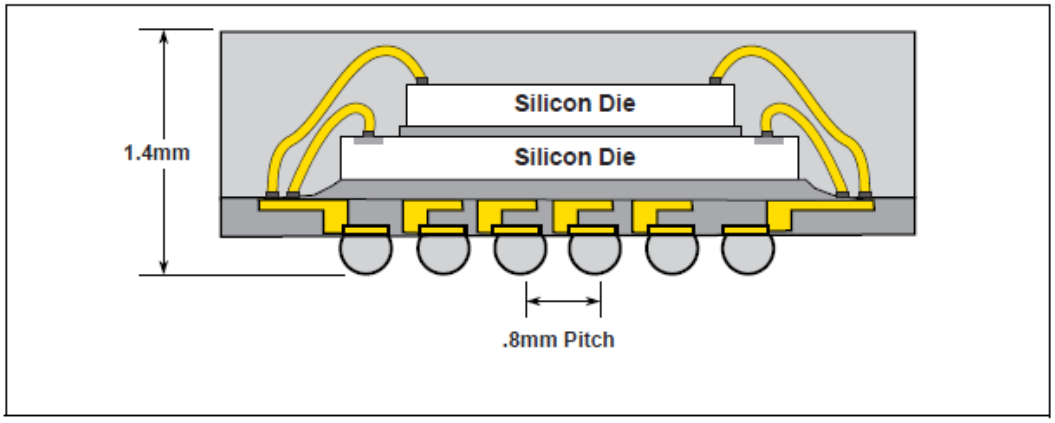
- The µBGA package is a **true chip size package**. Because of this, the actual package dimensions are dependent on the size of the silicon die.
- The µBGA package takes full advantage of any reduction of silicon die size. This makes the µBGA package **the smallest discrete Intel's flash memory package**.

Fig : Intel's Flash Memory

The µBGA Package



Intel® Stacked CSP



Another type of CSP gaining momentum in the industry is the "stacked" CSP. These packages are taking advantage of multiple application requirements, such as SRAM and Flash, and combining both die into one package.
However, instead of placing the individual die side by side (such as multi-chip modules), the Intel Stacked CSP stacks the two die on top of each other to get the maximum space savings advantage possible.

A µBGA exhibits better performance compared to other technologies when **chip delay** is a concern. A µBGA's electrical performance shows it has low resistance, capacitance and inductance

Applications :
If your application requires the ***smallest possible package***, the µBGA package and the Intel Stacked-CSP are the best package choice for your design.
These CSP's were designed to meet the demands of handheld applications such as cellular phones, pagers, personal digital assistants (PDA) and Global Positioning Systems (GPS) units

\

Bare die

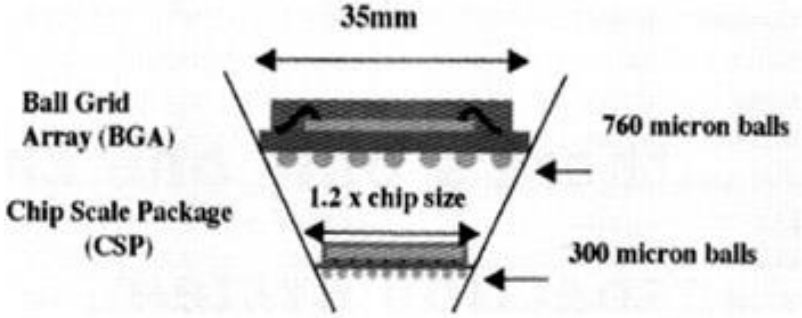
Bare or unpackaged, parts offer the smallest size , with no signal delays associated with the device package. Most common bare die and tape packages (bare die mounted on tape) include the following :

1. C4PBGA : An IC package that attaches the IC die to a plastic substrate using C4 process. It uses a multilayer substrate.

Fig :PCI Bridge Memory Controller using C4PBGA package

2. Chip-scale package (CSP) :

- A package where the IC is surrounded by a protective covering through which external electrode bumps on the bottom provide electrical contacts.
- The package only slightly larger than the chip it houses , has a height about 0.4mm
- An important feature of the CSP that differentiates it from the flip chip is that both the bumps and bump pitch are larger (>0.2 mm, 8 mils) than those of the flip chip.



(Courtesy National Semiconductor)

3. Tape carrier package (TCP) : formerly called TAB package.

- The Chip is mounted to a dielectric film , which has copper foil patterns on it.
- The TCP package uses three separate layers - a carrier film, an adhesive material, and a metal layer - held together by a TAB (Tape Automated Bonding) tape, to form an interconnection from the device's die to the external circuitry for the device.
- The TCP design is about ½ the volume and 1/3rd weight of an equivalent pin count TSOP package.

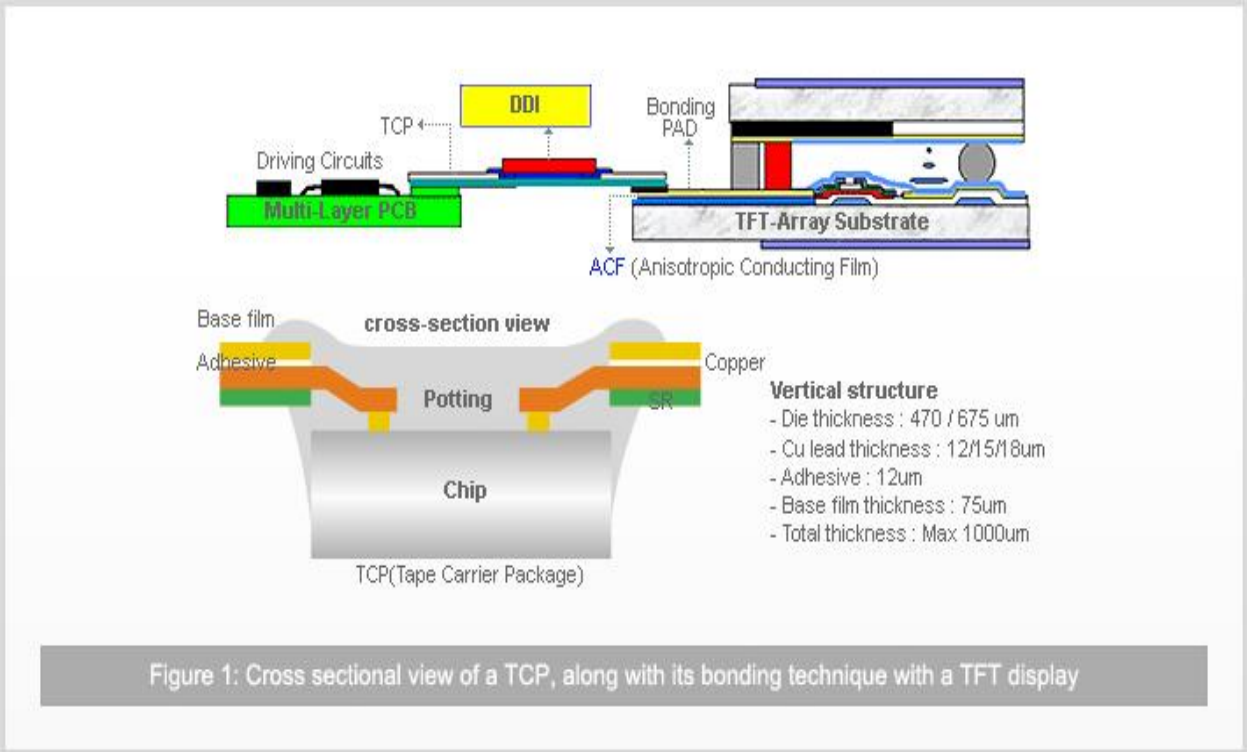


Figure 1: Cross sectional view of a TCP, along with its bonding technique with a TFT display

Figure 1 illustrates the cross-sectional view of a TCP, along with its bonding technique as used in a TFT (Thin-Film Transistor) display panel.

- TCP is a specially designed surface mounted IC package with very small outlines and high lead counts.

Features :

TCP offers all the benefits, such as

- reduced lead pitches, ultra-thin package profiles, and smaller footprints for the device on the PCB, resulting in significant savings of board space for such applications,
- Ease of mass production using standard technology,
- Stable thermal and electrical performance,
- reduced lead inductances for the device due to the pins bonded directly to the die,
- High device and package reliability.
- TCPs possess excellent thermal stability and reliability, both on the shelf and under operation.

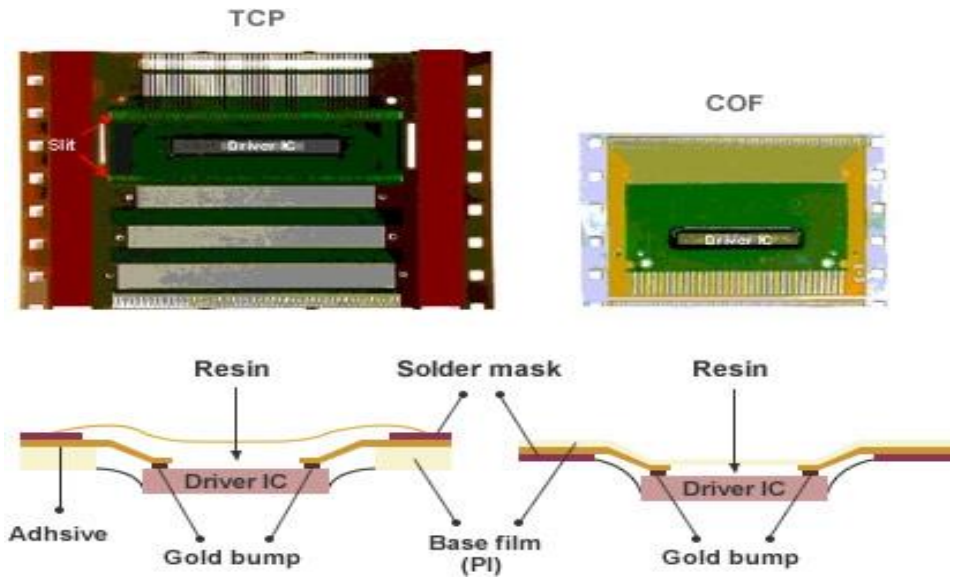
Applications :

- TCPs are widely used as the default packaging solutions for the majority of high-end applications display devices and panels. This includes LCD and Plasma TV panel
- TCP are used in microprocessors/microcontrollers, and ASICs that power a multitude of small and lightweight applications, such as laptop and tablet computers, and advanced mobile handsets.

4. Chip on board (COB) :The die is mounted directly on the Printed circuit board or circuit.

5. Chip on flex/ Film (COF) :

- It is a variation of COB.
- Here, instead of bonding the bare die to a substrate, it is bounded to a piece of 0.15 in thick polyimide film that has a top layer of gold-plated copper.
- Is more expensive than COB , but failed parts can be removed in COF.
- The COF (Chip On Film) structure is specifically designed for connecting displays, such as TFT and LCD panels, to a PCB.



Benefits of COF

COFs lend several advantages to the production of display devices and panels, such as low dimensions and weights, lower power consumption, and ease of scalability with increases in display panel resolutions.

Applications

- COFs are the default technique to implement display devices on all of today's high-end devices, such as mobile handsets, PDAs, LCD/PDP televisions, monitors, laptop/tablet computers, and PMPs, among others.
- For flat panel displays with high-resolution requirement.

6. Tape Automated bounding (TAB)

Tape-automated bonding (TAB) is a process that places bare integrated circuits onto a printed circuit board (PCB) by attaching them to fine conductors in a polyamide or polyimide film, thus providing a means to directly connect to external circuits.

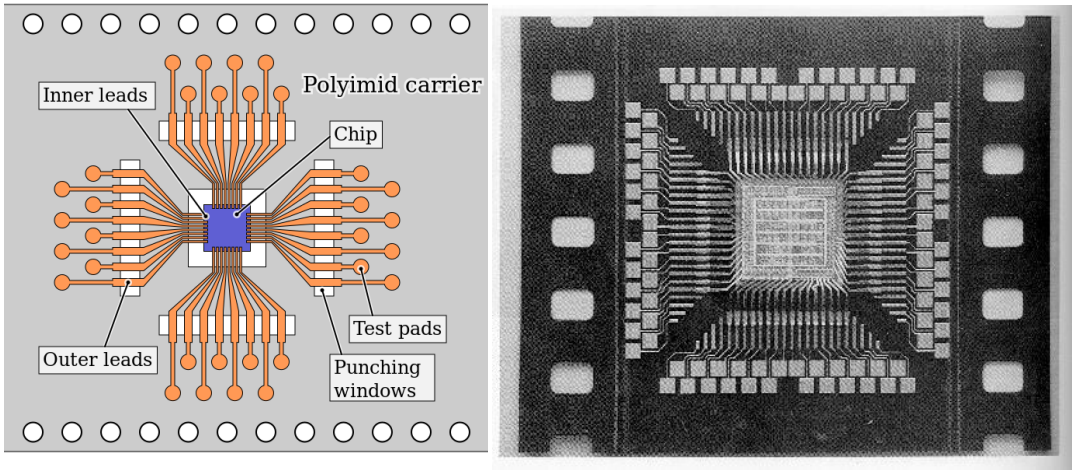


Fig :Tape-automated bonded die with a bare chip placed on the tape and connected to an interconnection pattern

Techniques, such as TAB (Tape Automated Bonding), are normally deployed to connect the display chip with the PCB.

Advantages :

The tape-automated bonding technology provides several advantages over the wire bonding technology.

These advantages include

(a) a smaller bonding pad compared to wire bonding technology,
(b) smaller on-chip bonding pitch
(c) a decrease in the quantity of gold used for bonding,
(d) an increase in production rate because of area or `gang' bonding, and
(e) a stronger and more uniform inner lead bonding strength.

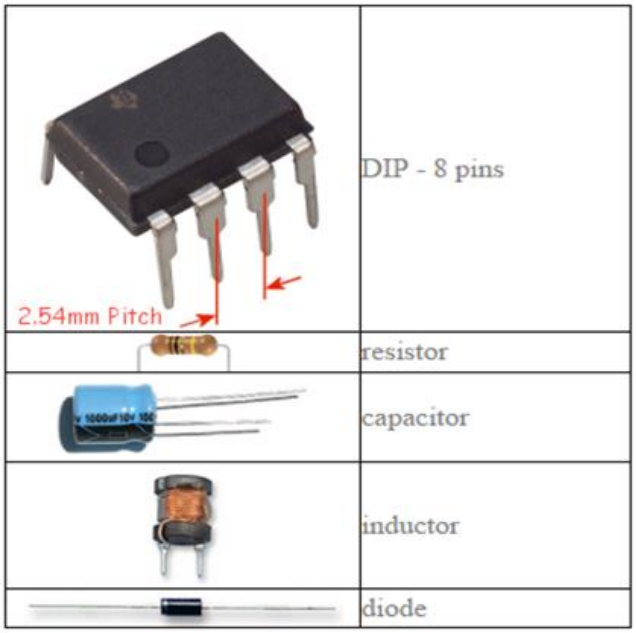
Also Use of such techniques provides multiple advantages, such as use of smaller bonding pads and finer bonding pitches, improved electrical contacts resulting in better electrical performance at higher frequencies, and shorter production cycles.

7. Demountable TAB (DTAB) :

- Developed by Hewlett- Packard (HP) .
- Mechanical screw and plates align and hold the IC to the board (pressure between the tape and the board provides the contact).
- The IC can be replaced by removing the screws.

8. Ultra-high volume density (UHVD) :A process developed by General Electric (GE) to interconnect bare ICs on prefabricated laminated polyimide film.

Through-Hole Packages



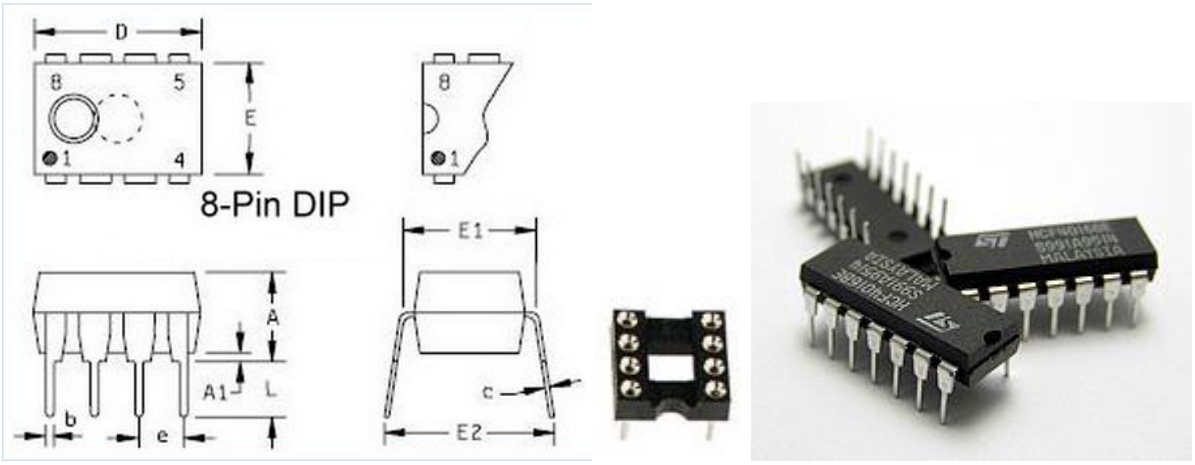
These packages, as the name implies, mount in holes on the PCB. These device packages include the following:

1. **Dual in-line (DIL)** :DIP is the most common through-hole IC package.These little chips have two parallel rows of pins extending perpendicularly out of a rectangular, black, plastic housing.

Fig: A 28-pin DIP-packaged microcontrollers

2. **Dual in-line package (DIP)** : A component with two straight parallel rows of pins or lead wires. The number of leads may be from 8-68 pins , 0.1 –in pin spacing. DIP parts may be ceramic or plastic (where the die is molded into plastic package)

3. **Plastic DIP (PDIP)** :A plastic DIP IC is a normal Dual In-line Package that uses Plastic for the IC body to keep the cost low. The pin to pin spacing on a dual inline package is 0.1 inches



Common ICs found in an 8 pin Plastic DIP:

a. LM741 Operational Amplifier [741 Op Amp].
b. 555 Timer.
c. 4-Position DIP Switch.

8-pin DIP packages are more commonly used with analog components than for digital integrated circuits.

4. **Ceramic dual in-line package (CERDIP)** :

A Ceramic DIP IC is a normal Dual In-line Package that uses Ceramic instead of Plastic for the IC body, at a higher cost. Ceramic protects the IC from higher temperature and humidity conditions.

Fig : Ceramic DIP IC

Fig : A comparison between a Ceramic and Plastic DIP IC

5. **Shrink DIP (SDIP)** : It usually has 24-64 pins with 0.07-in lead spacing.

6. **Single in-line (SIP) :** Single-In-Line Package (SIP) components have a flat body oriented vertically to the printed wiring board and a single row of pins or leads. Most small-form SIPs are parallel-array devices of common value components (i.e. diode, resistor arrays).

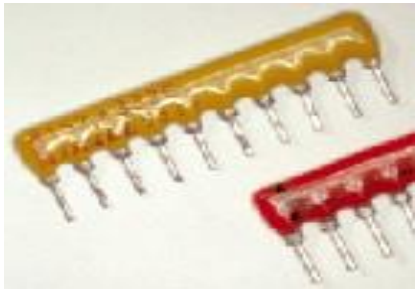


Fig : SIP Resistor Package

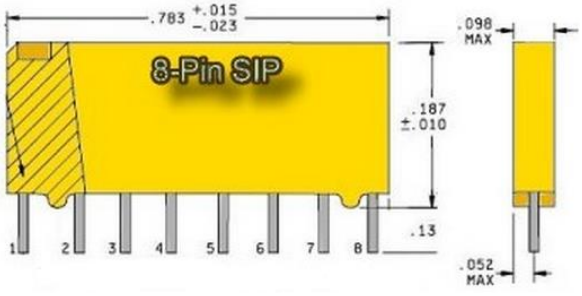
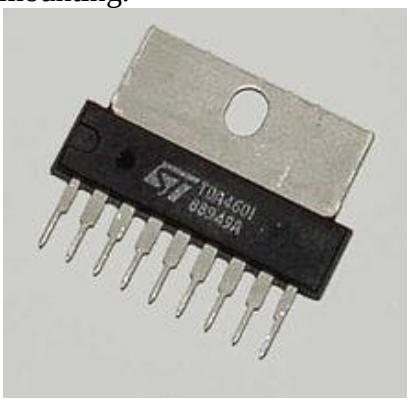


Fig : 8-pin SIP Package Through Hole Component

7. **Single in-line module (SIM)** : Here , electrical connections are made to a row of conductors along one side.

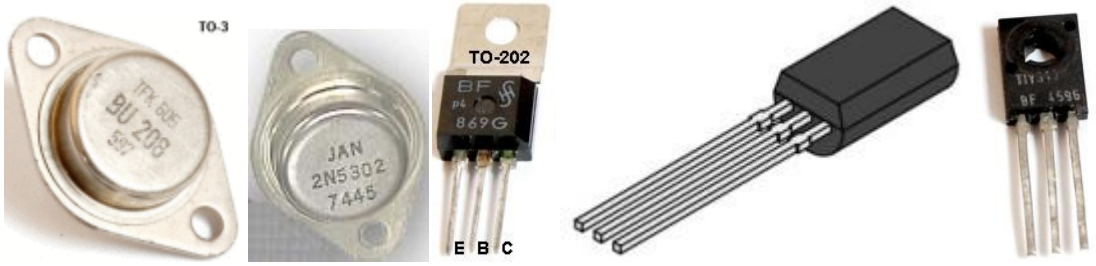
8. **Single in-line package (SIP)** : A vertically mounted module with a single row of pins along one edge for through-hole mounting.



Eg : L298 motor driver IC

9. **Vertical in-line package (VIP)**:

10. **Transistor outline –XX (TO-XX)** : refers to a package style registered with JEDEC.



11. **Quad in-line package (QUIP)** : Similar to DIP except , it has a dual row of pins along the package edge.

Fig : A Rockwell 6502-based microcontroller in a QIP package

12. **Zig- zag in-line package (ZIP)** : This may be either a DIP package that has all the leads on edge in a staggered zig-zag pattern. The ZigZag Package is not used that often

Fig :ZigZag IC & Socket

13.**Pin grid array (PGA)package**: Pin Grid Array [PGA] is a Through-Hole style IC, made up of an array of pins.
A plastic or ceramic square package with pins covering the entire bottom surface of the package. Packages have various pin count (68 or more).

Fig : Celeron PGA Processor

14. **Pinned uncommitted memory array (PUMA II)** : A PGA package ASIC memory array with four 32-pad LCC sites on top of a 66 PGA.

Module Assemblies

- A packaging scheme that take either packaged parts or bare die and use them to make an assembly.
- This may be by either mounting the parts to a substrate or PCB or die to create dense memory modules.
- This packaging scheme maybe surface mount or through–hole.

1. **Dual-in-line memory module (DIMM)**: It has memory chips mounted on both sides of a PC board .These modules are mounted on a PCB and designed for use in personal computers, workstations and servers. It is the most predominant form of memory module available today.

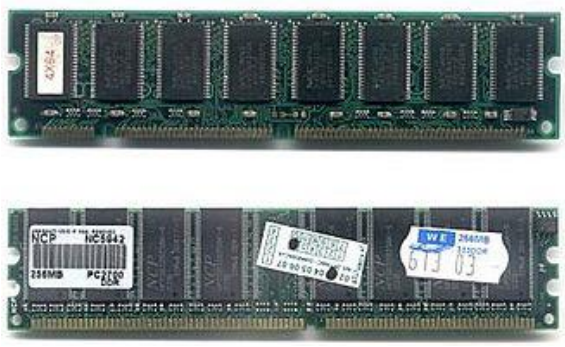


Fig: Two types of DIMMs: a 168-pin SDRAM module (top) and a 184-pin DDR(Double data rate) SDRAM module (bottom). The SDRAM module has two notches (rectangular cuts or incisions) on the bottom edge, while the DDR1 SDRAM module has only one. Also, each module has eight RAM chips, but the lower one has an unoccupied space for the ninth chip.

DIMMs have separate electrical contacts on each side of the module. Another difference is that standard SIMMs have a 32-bit data path, while standard DIMMs have a 64-bit data path.

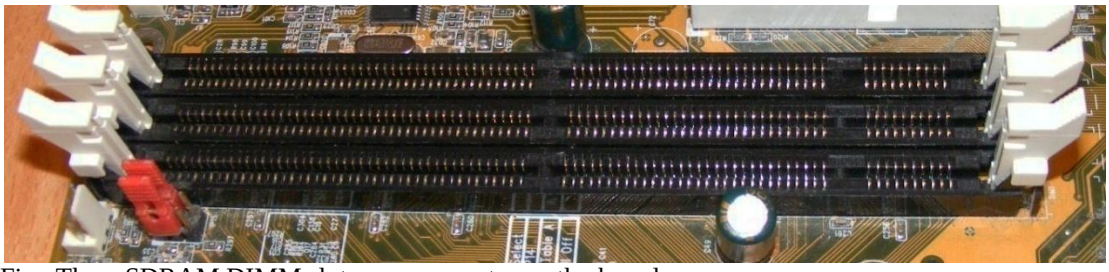
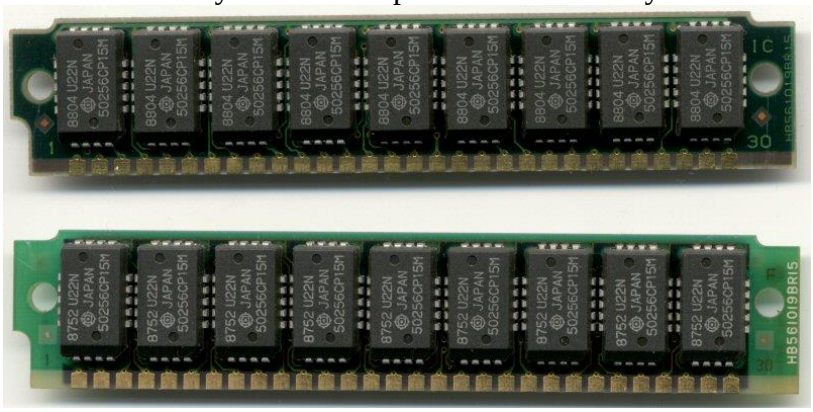


Fig : Three SDRAM DIMM slots on a computer motherboard

It has key features for 5V , 3.3V and 2.5V inputs and for indicating whether it is made with asynchronous DRAMs or flash , SRAM or DRAM ICs.

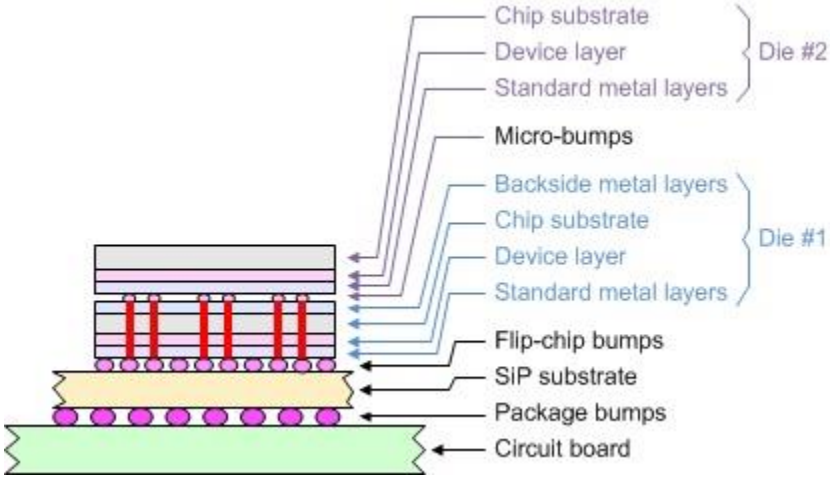
2. **Single-in-line memory module (SIMM)**:A SIMM, is a type of memory module containing random-access memory used in computers from the early 1980s to the late 1990s.

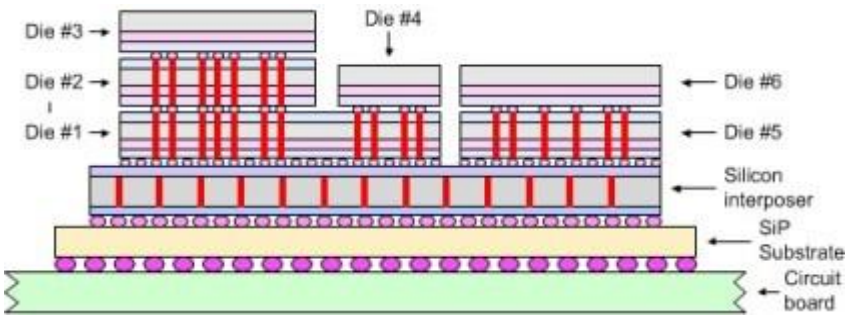


An assembly containing memory chips. SIMM modules are designed to be use with sockets that may hold the SIMM upright or at an angle, which reduces the height of the module on the circuit board.

3. **Flexible-rigid-assembly memory module (FRAMM)** :
The FRAMM (flexible-rigid assembly memory module) memory packaging scheme, from Memory X Inc, can pack 16 Mbytes of dynamic RAM onto a module compatible with industry-standard JEDEC 30-and 72-pin SIMMs
A memory packaging scheme which uses a combination of frigid and flexible PC board assemblies, with flexible board interconnecting to rigid PC boards.

4. **Full Stack technology** : Packing 20-100 dice horizontally in a loaf-of-bread configuration.





5. **Hermetic DIP (HDIP) module** : It has hermetic sealed components mounted on the top and bottom of a ceramic substrate

.

Fig : Hermetically sealed side-brazed ceramic DIP package

6. **Hermetic vertical DIP (HVDIP)** : A vertically mounted ceramic module with pins along both edges (through-hole mounting). Components used in this module are hermetically sealed.

7. **Multi-Chip module (MCM)** : A MCM is generically an electronic assembly where multiple ICs, semiconductor dies and/or other discrete components are integrated, usually onto a unifying substrate, so that in use it is treated as if it were a single component (as though a larger IC) .

Incorporating multiple integrated circuits (ICs) into a single device, multi-chip modules offer benefits in device size and performance. By shortening the signal-path between ICs, and using a common high-performance substrate material, multi-chip modules can improve device operation while managing size and weight constraints.

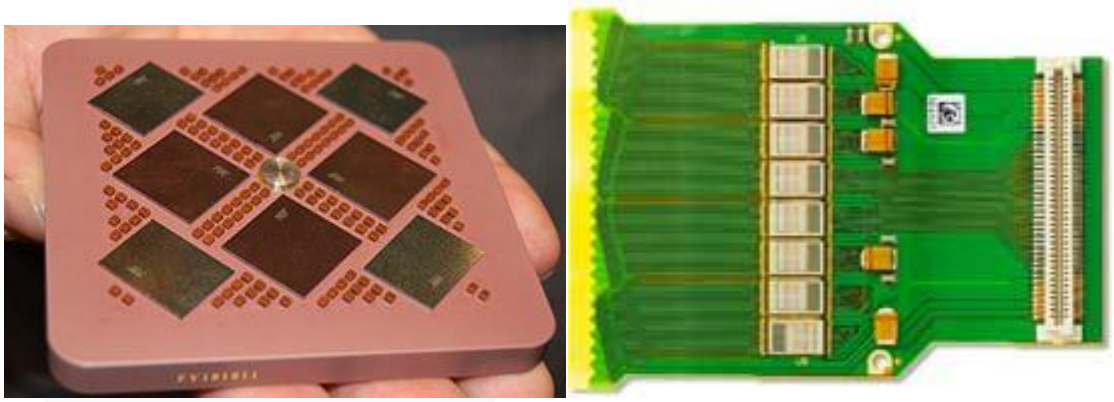


Fig :POWER5 MCM with four processors and four
36 MB external L3 cache dies on a ceramic multi-chip module.

A circuit package with SMT (surface mount) IC chips mounted and interconnected via a substrate similar to a multilayer PC board.

MCMs are classified according to the technology used to create the HDI (High Density Interconnection) substrate.

MCM-L – laminated MCM. The substrate is a multi-layer laminated PCB (Printed circuit board).
MCM-D – deposited MCM. The modules are deposited on the base substrate using thin film technology.
MCM-C – ceramic substrate MCMs, such as LTCC.

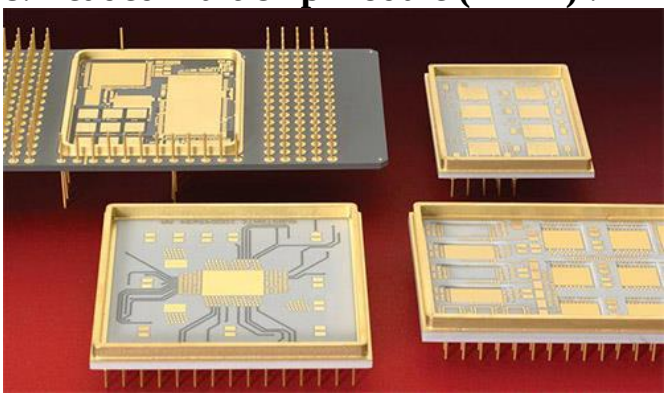
Advantages : MCM devices offer higher speed and performance at lower cost than conventional devices.
Disadvantages : Manufacturing issues associated with MCM module include availability of unpackaged die, how to test/inspect the die, and test of MCM module.

A relatively new development in MCM technology is the so-called "chip-stack" package. Certain ICs, memories in particular, have very similar or identical pinouts when used multiple times within systems.
The chip-stack is an attractive option in many applications such as cell phones and personal digital assistants (PDAs). After a thinning process, as many as ten dies can be stacked to create a high capacity SD memory card.

Examples of MCM technologies

IBM 3081 mainframe's thermal conduction module (1980s)
Intel Pentium Pro, Xeon, Core 2 Quad (Kentsfield and Yorkfield), Clarkdale, Arrandale, and Haswell-H
Sony memory sticks
Xenos, a GPU designed by ATI Technologies for the Xbox 360, with eDRAM
POWER2, POWER4, POWER5 and POWER7 from IBM

8. **Leaded multichip module (LMM)** :



9. **Memory cube** : A 3D module consisting of stacked memory devices such as DRAMs or SRAMs.

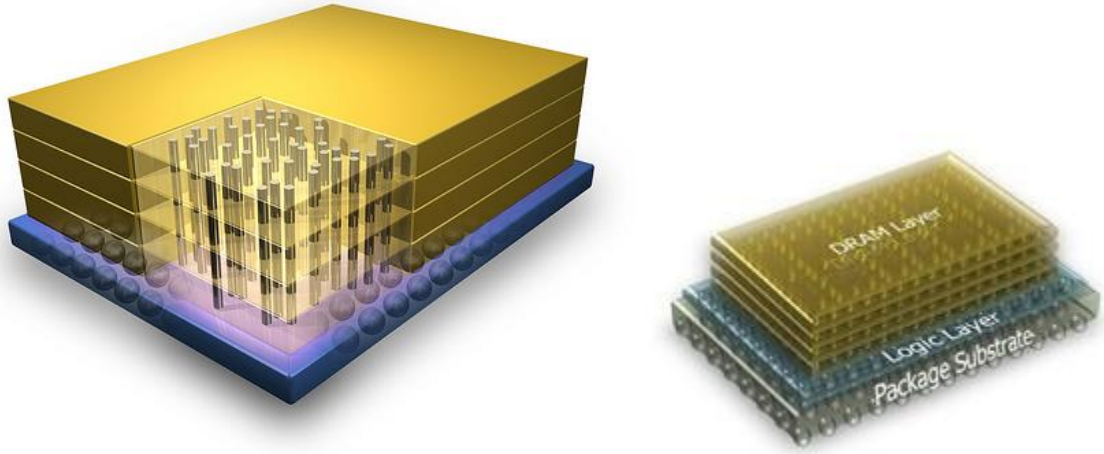


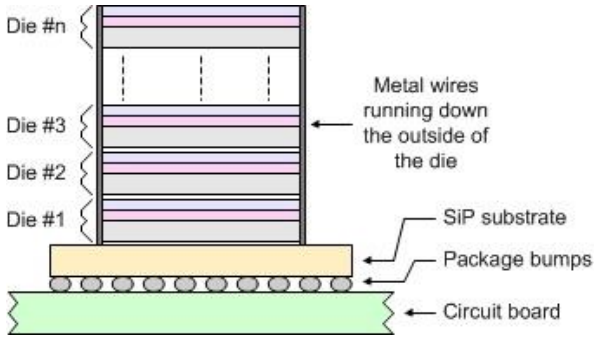
Fig : Micron's Hybrid Memory Cube features a stack of individual chips connected by vertical pipelines or "vias," shown above. IBM's new 3-D manufacturing technology, used to connect the 3D micro structure, will be the foundation for commercial production of the new memory cube.

10.**Ribcage** : A trademark of Staktek Corporation for a 3D memory module design.

11.**UniframeStaktek module** : A trade name for a 3D stack of TSOP memory ICs by Staktek Corporation. A stacked standard TSOP design that offers density improvements of 2-4 times that of standard, single-chip packaging with similar electrical and thermal performance. Available in stacks of 2 through 8 , each module has a memory capacity of 64-256 MB for FLASH, 2-32 MB for SRAM and 32-128 MB for DRAM.

12.**Short Stack** : A method of stacking semiconductor dice vertically, where memory ICs (such as 4 SRAMs) are assembled into a 3D thin-film monolithic package with the same footprint as single SRAM.

The stacks maybe unpackaged for use in hybrid , multichip and chip-on-board applications. Interconnect techniques include wire-bound, tab and flip-chip methods.



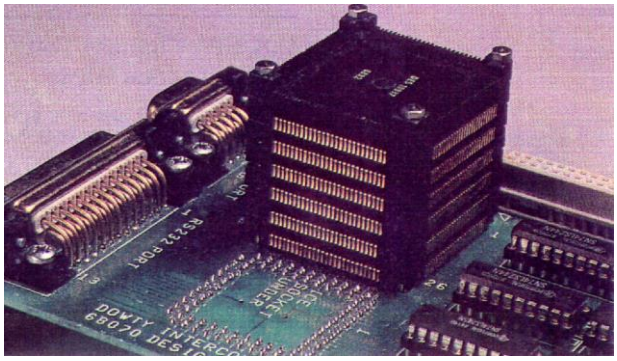


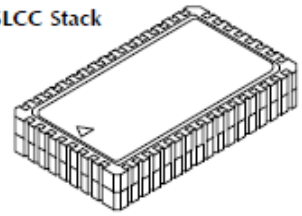
Fig : Connecting dice using wires running down the sides

13. **Stackable leadless chip carrier (SLCC)** :

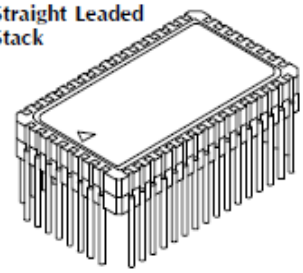
This multi-dimensional module consists of stacked chip carriers. SLCC can achieve a density of 40:1 over conventional packages.

CIRCUIT DENSITY	HIGHEST	STACK	Multi-chip Module using Stackable Leadless Chip Carriers (SLCC)
		DSMCM	Double Sided Multi-chip Modules
		HYBRID	Several Die in 1 Package
	HIGHER	QFP	Quad Flatpack
		PGA	Pin Grid Array
		LCC	Leadless Chip Carrier
		PLCC	Plastic Leadless Chip Carrier
		SOJ	Small Outline Package
		SOIC	Small Outline I.C.
		FP	Flatpack
	LOWER	DIP	Dual In Line Package

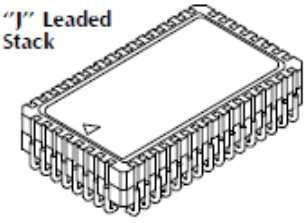
SLCC Stack



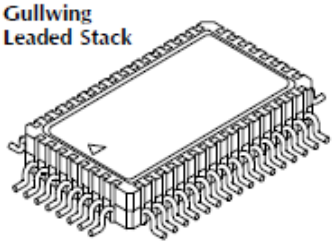
Straight Leaded Stack



"J" Leaded Stack



Gullwing Leaded Stack



FEATURES OFF SLCC's

- Surface Mount technology
- Stackable Ceramic Leadless chip Carrier
- Hermetically Sealed
- Pinout Internally and/or Externally Configurable
- Operates over Full Military Temperature Range
- Typically Single I.C. *(Can Accept Multiple)*
- Can Easily Mirror Pinouts
- Small Size

Packages Available:

48 - Pin SLCC Stack
48 - Pin Straight Leaded Stack
48 - Pin ''J'' Leaded Stack
48 - Pin Gullwing Leaded Stack

- By using SLCCs, the ''Stack'' family of modules offer a higher board density of memory than available with conventional through-hole, surface mount or hybrid techniques.
- Example: The module packs 2-Megabits of High Speed low-power CMOS static RAM in an area as small as 0.463 in2, while maintaining a total height as low as 0.171 inches.
- This SRAMSTACK modules contain two individual 128K x 8 SRAMs, each packaged in a hermetically sealedSLCC, making the modules suitable for commercial, industrial and military applications.

END