Experiment No. 9

Aim: Simulate n type MOSFETs (bulk single gate, Double Gate) to obtain family of I_D-V_G and I_D-V_D characteristics and compare the results obtained.

Software Tool: FETToy simulation tool on available on nanohub.org

Resources / Apparatus Required: Hardware: PC

Theory:
FETToy tool is a numerical simulator that calculate the ballistic I-V characteristics for a conventional MOSFETs, Nanowire MOSFETs and Carbon NanoTube MOSFETs. For conventional MOSFETs, FETToy assumes either single or double gate geometry and for a nanowire and nanotube MOSFETs it assumes a cylindrical geometry.

DOUBLE GATE MOSFET
The concept of a Double-gate MOSFET is that it efficiently controls the channel from gates on both sides of the channel instead of one gate in planar bulk MOSFETs. Controlling the channel by multiple (i.e. double, triple, surround, etc.) gates has its supremacy of better control over the channel inversion, so the short channel effect is reduced. More specifically, reducing the current leakage and eliminating the drain-induced barrier lowering (DIBL) effect are examples of superiority in double-gate MOSFETs.

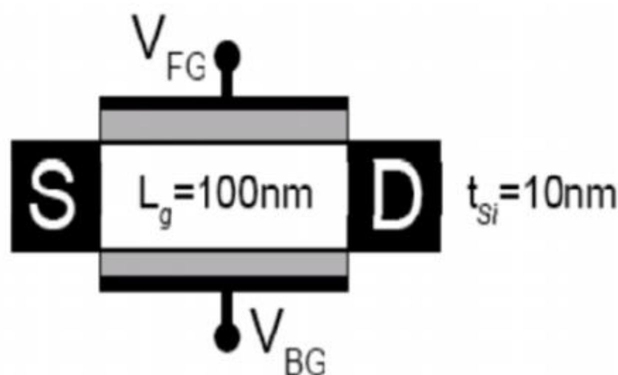

Figure : DG-MOSFET Structure with a Thin Body (t_{si}) and Channel Length (L_g)

The structure of a DG-MOSFET based on the SOI technology is shown in figure above, where two aligned gates are used to modulate electric fields and better manage channel charges from either side. Two gates are used to systematically control the electrostatic coupling, so the amount of current flow in the channel is properly modulated by the electric field. The short channel effect is effectively suppressed for higher currents as compared to a single gate MOSFET. The control of the back-gate enables higher transconductance, allows sharper sub-Threshold slope, and minimizes short channel effects. It has been reported in academic publications that the ideal sub threshold slope of 60 mV/decade is achieved in DG-MOSFETs compared with bulk MOSFETs, which greatly reduce the leakage currents below threshold voltage.

FETToy GUI

FETToy

Device | Models | Environment

Model: Single-Gate MOSFET

Gate Insulator Thickness: 1.5nm

Gate Insulator Dielectric Constant: 3.9

Effective Mass Ratio: 0.19

Valley Degeneracy: 2

Floating Boundary Flag: no

Body Thickness: 10nm

Source Doping Density: 1e+20/cm3

Oxide Dielectric Constant

Gate

Electron Masses in Silicon

SiO_2

T_{ox}

Source

T_{Si}

Channel

Drain

FETToy

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In FETToy models , there are two important parameters such as alphaG and alphaD which can be varied and observed how it affects MOSFET characteristics

Gate control parameter (alphaG) : It is the gate capacitance divided by the sum of the gate, source and drain capacitances. It controls the sub-threshold swing according to S = (2.3kT/q)/ alphaG .

Drain control parameter (alphaD) : It is the gate capacitance divided by the sum of the gate, source and drain capacitances. It controls the drain induced barrier lowering (DIBL) according to DIBL = S* alphaD/(2.3kT/q) , where S is the sub-threshold swing.

When alphaG = 1 and alphaD = 0 , there is complete gate control; the sub-threshold swing is ideal and drain induced barrier lowering (DIBL) is zero.

Question1: Explain the effect of “tox” on I_D-V_G and I_D-V_D characteristics of single gate and double gate MOSFETs ?

Question2 : Explain the effect of “Ɛox” on I_D-V_G and I_D-V_D characteristics of single gate and double gate MOSFETs ?

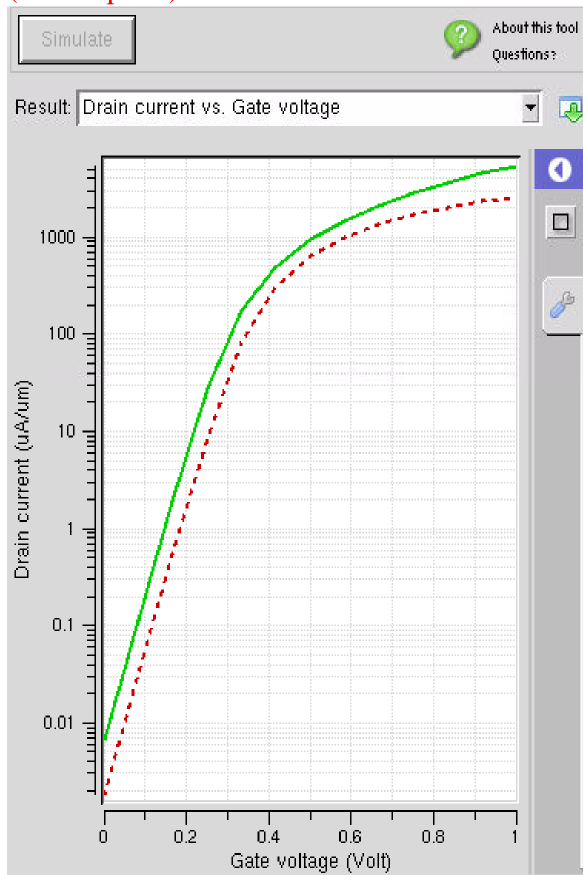
Questions3: For similar parameters and conditions , give reason’s why Double gate MOSFETs have higher current density I_D ?

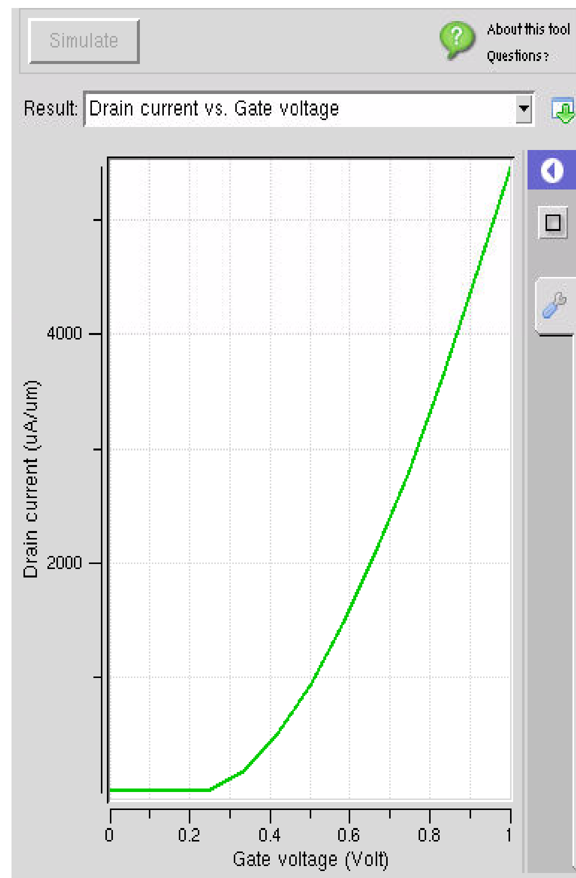
Simulation Plots

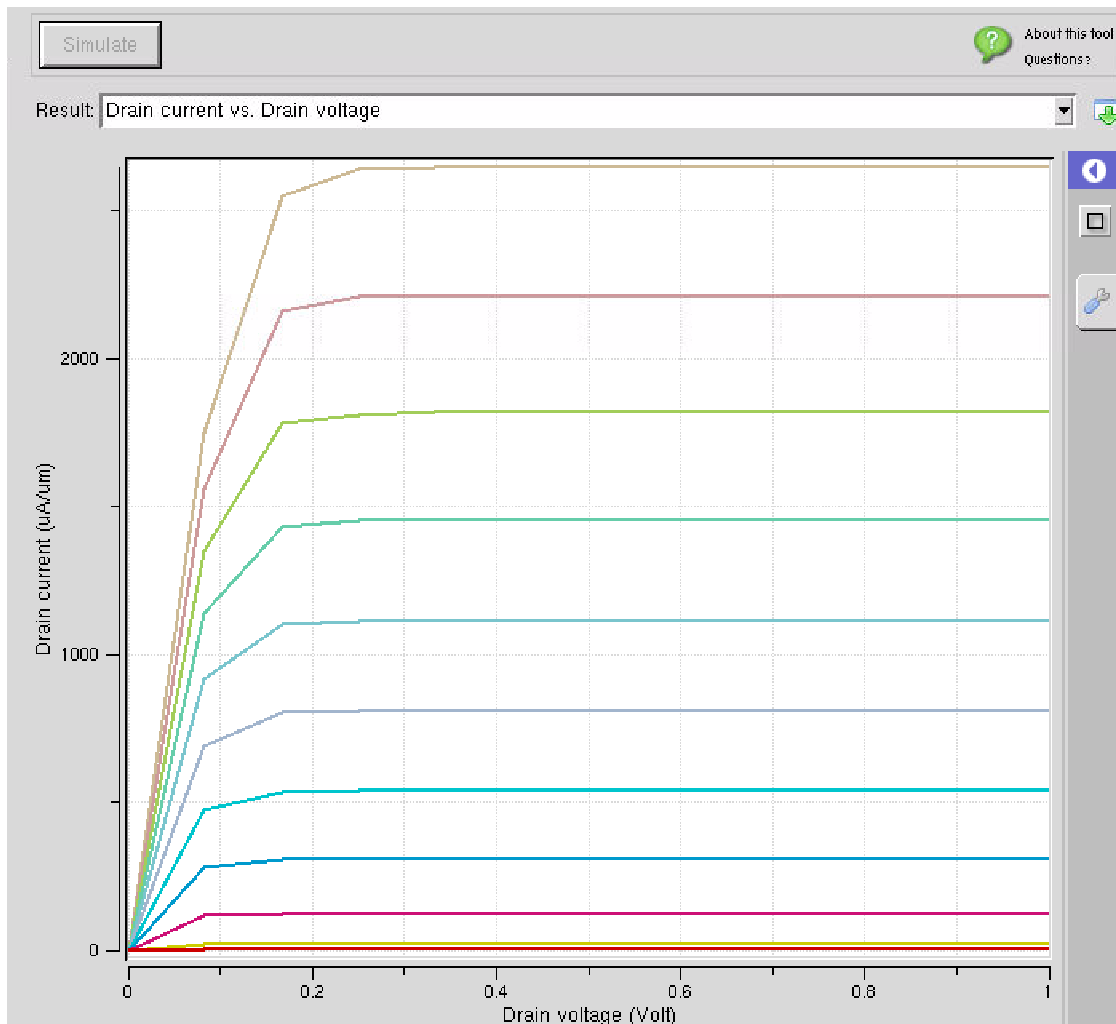
Parameters such as Gate Control Parameter , Drain Control Parameter , gate insulator thickness ‘tox’ , Gate insulator dielectric constant ‘Ɛox’ of SG MOSFET and DG MOSFET are varied and I_D-V_G (Log + Linear) , I_D-V_D plots are simulated from where we can estimate I_{Don} and I_{Doff} current of the SG and DG MOSFET.

Please attach all the plots for single gate and double gate MOSFETS along with the writeup.

Sample Plot (these 3 plots are for single gate MOSFETs for one parameter variations, u’ll have to do this for 2 more parameter variations , and then u will have 3 sets of 3 such plots for Single gate MOSFET (total 9 plots), then u have to repeat this for double gate MOSFETs (total 9 plots)







Conclusion:

Sample conlusion

After analyzing the results it is definitely clear that the drain current characteristics of DG FET are better than of bulk single MOSFET. The presence of double gate drives the drain current to a higher value as compared to SG MOSFET because of the higher resistance due to the substrate present near the channel. The DG FET has lower resistance and the movements of ions are more due to the potential applied from two gate terminals, also in DG FET the channel in is electrostatically isolated from the drain voltage so it gives better output.