Experiment No. 10

Aim: Simulate Silicon Nanowire (SiNW) transistor for different conditions and comment on the results obtained.

Software Tool: FETToy simulation tool available on nanohub.org

Resources / Apparatus Required: Hardware: PC

Theory:
FETToy tool is a numerical simulator that calculate the ballistic I-V characteristics for a conventional MOSFETs, Nanowire MOSFETs and Carbon NanoTube MOSFETs. For conventional MOSFETs, FETToy assumes either single or double gate geometry and for a nanowire and nanotube MOSFETs it assumes a cylindrical geometry.

SILICON NANOWIRES
Silicon nanowires can be prepared with single-crystal structures, diameters as small as several nanometers and controllable hole and electron doping, and thus represent powerful building blocks for nanoelectronics devices such as field effect transistors.

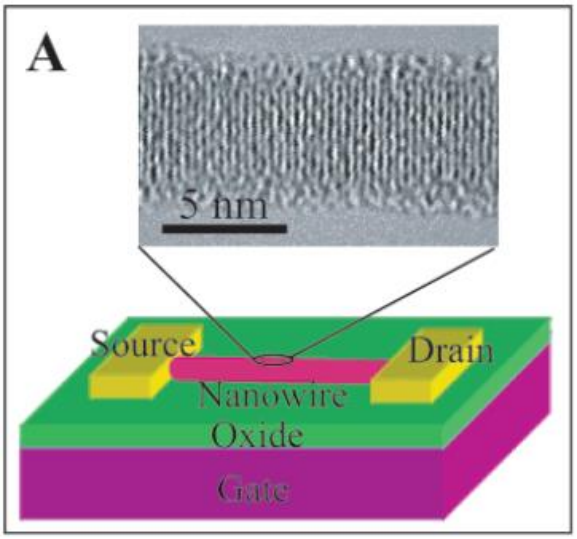
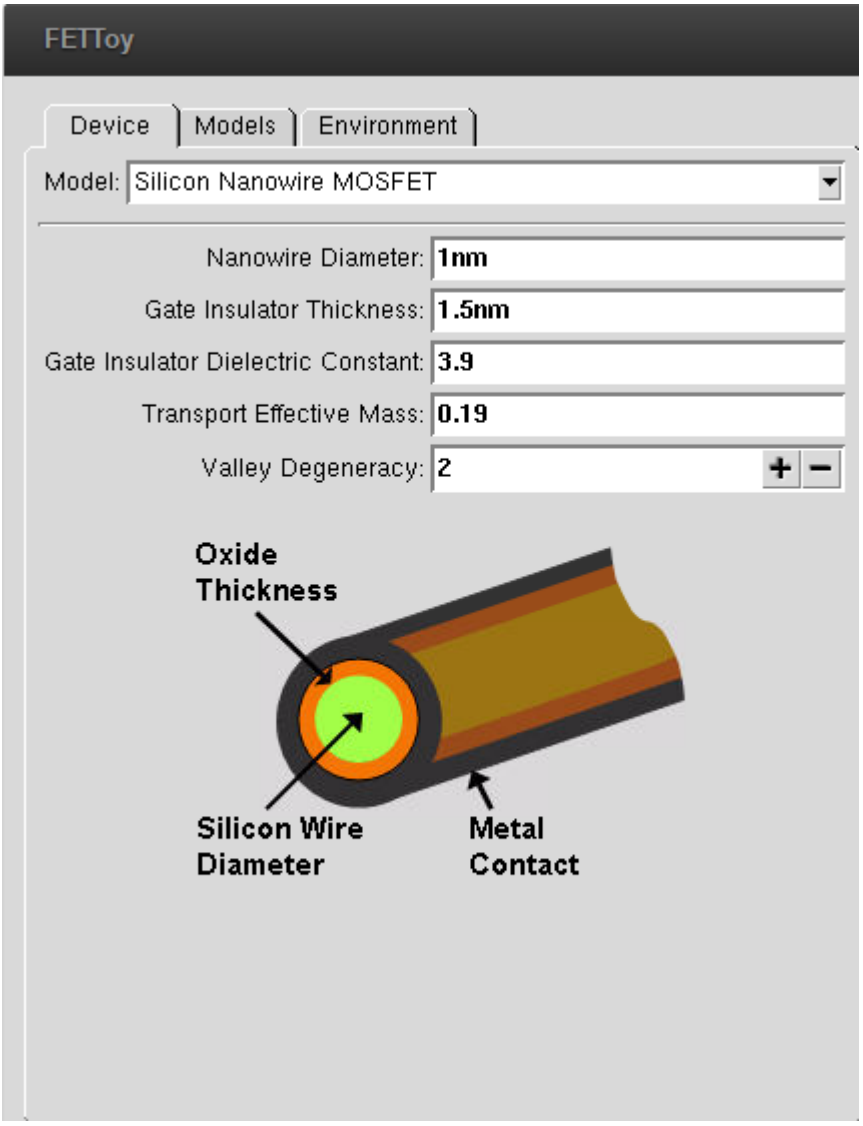


Figure 1. Schematic of a SiNW FET showing metal source and drain electrodes with the NW and contacts on the surface of SiO2/Si substrate.

Semiconductor nanowires (NWs) and carbon nanotubes (NTs) are attractive components for future nanoelectronics since they can exhibit a range of device function and at the same time serve as bridging wires that connect to larger scale metallization. For example, field effect transistors (FETs) have been configured from NWs and NTs by depositing the nanomaterial on an insulating substrate surface, making source and drain contacts to the NW or NT ends, and then configuring either a bottom or top gate electrode (Figure 1). This basic approach may serve as the basis for hybrid electronic systems consisting of nanoscale building blocks integrated with more complex planar silicon circuitry.

SiNW FET results have been scaled using the SOI FET gate length in 100s of nm and gate oxide thickness in few nm. Significantly, the scaled on-state current (Ion) for the SiNW FET is larger than state-of-the-art Si FETs, and moreover the average subthreshold slope approaches the theoretical limit16 and the average transconductance is ca. 10 times larger. These improvements could lead to substantial benefits for high speed and high-gain devices. The SiNW FET devices also have larger leakage currents, but this issue could be addressed by implementing pn-diodes at the source and drain contacts as in conventional MOSFETs. This comparison suggests that efforts to make smaller SiNW FETs and explicitly test scaling predictions could have an important impact in the future.
Comparison of scaled SiNW FET transport parameters with those for state-of-the-art planar MOSFETs show that SiNWs have the potential to exceed substantially conventional devices, and thus could be ideal building blocks for future nanoelectronics.

FETToy GUI



In FETToy models , there are two important parameters such as alphaG and alphaD which can be varied and observed how it affects MOSFET characteristics

Gate control parameter (alphaG) : It is the gate capacitance divided by the sum of the gate, source and drain capacitances. It controls the sub-threshold swing according to S = (2.3kT/q)/ alphaG .

Drain control parameter (alphaD) : It is the gate capacitance divided by the sum of the gate, source and drain capacitances. It controls the drain induced barrier lowering (DIBL) according to DIBL = S* alphaD/(2.3kT/q) , where S is the sub-threshold swing.

When alphaG = 1 and alphaD = 0 , there is complete gate control; the sub-threshold swing is ideal and drain induced barrier lowering (DIBL) is zero.

Question1: Explain the effect of "tox" on I_D-V_G and I_D-V_D characteristics of Si Nanowire MOSFET ?

Question2 : Explain the effect of "Ɛox" on I_D-V_G and I_D-V_D characteristics of Si Nanowire MOSFET ?

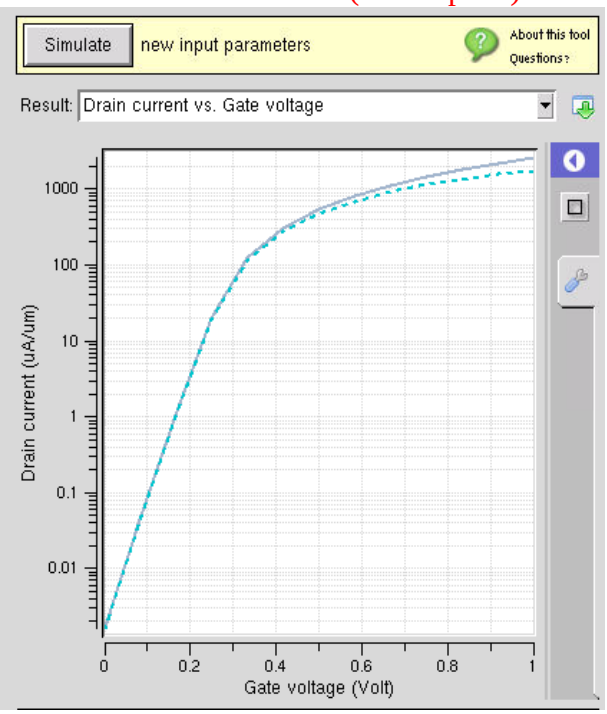
Questions3: Explain the effect of nanowire diameter on I_D-V_G and I_D-V_D characteristics of Si Nanowire MOSFET ?

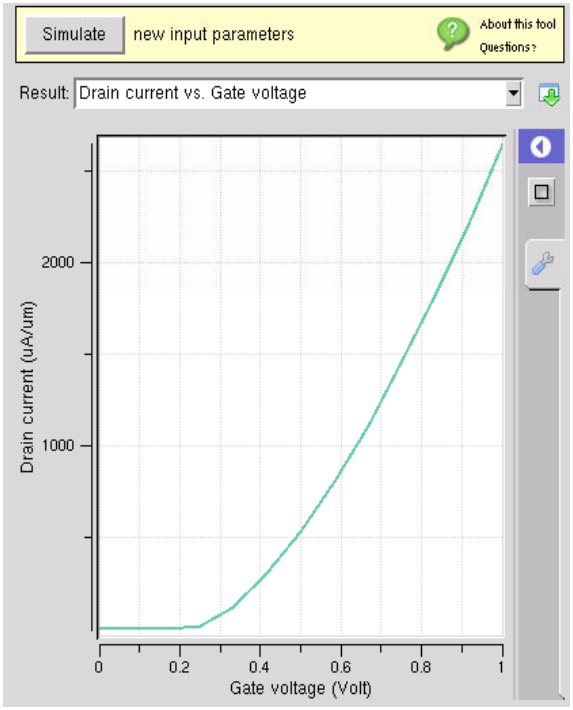
Simulation Plots

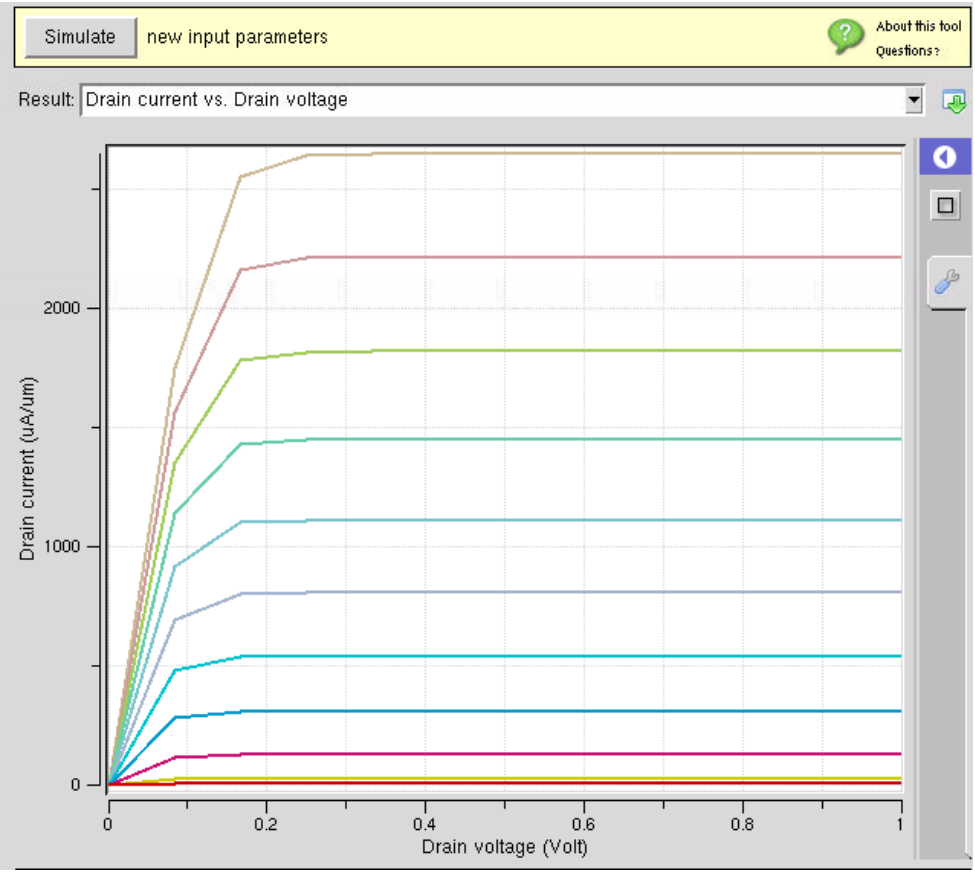
Parameters such as nanowire diameter, gate insulator thickness 'tox' , gate insulator dielectric constant 'Ɛox' of Si Nanowire MOSFET are varied and I_D-V_G (Log + Linear) , I_D-V_D plots are simulated from where we can estimate I_{Don} and I_{Doff} current of the Si Nanowire MOSFET.

Please attach all the plots for Si Nanowire MOSFET along with the writeup.

Sample Plot (these 3 plots are for Si Nanowire MOSFET for one parameter variations, u'll have to do this for 2 more parameter variations , and then u will have 3 sets of 3 such plots for Si Nanowire MOSFET (total 9 plots)







Conclusion:

Sample conlusion

Hence we observed I-V characteristics of silicon nanowire transistor. It is observed that the drain current is increasing rapidly, when diameter of nanowire is increasing for same input conditions