GaAs Technologies

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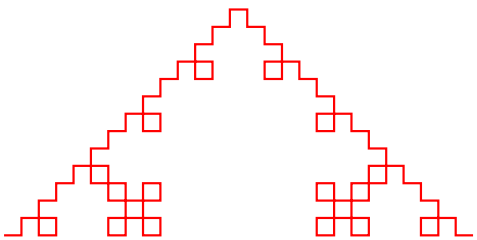

October 9, 2016

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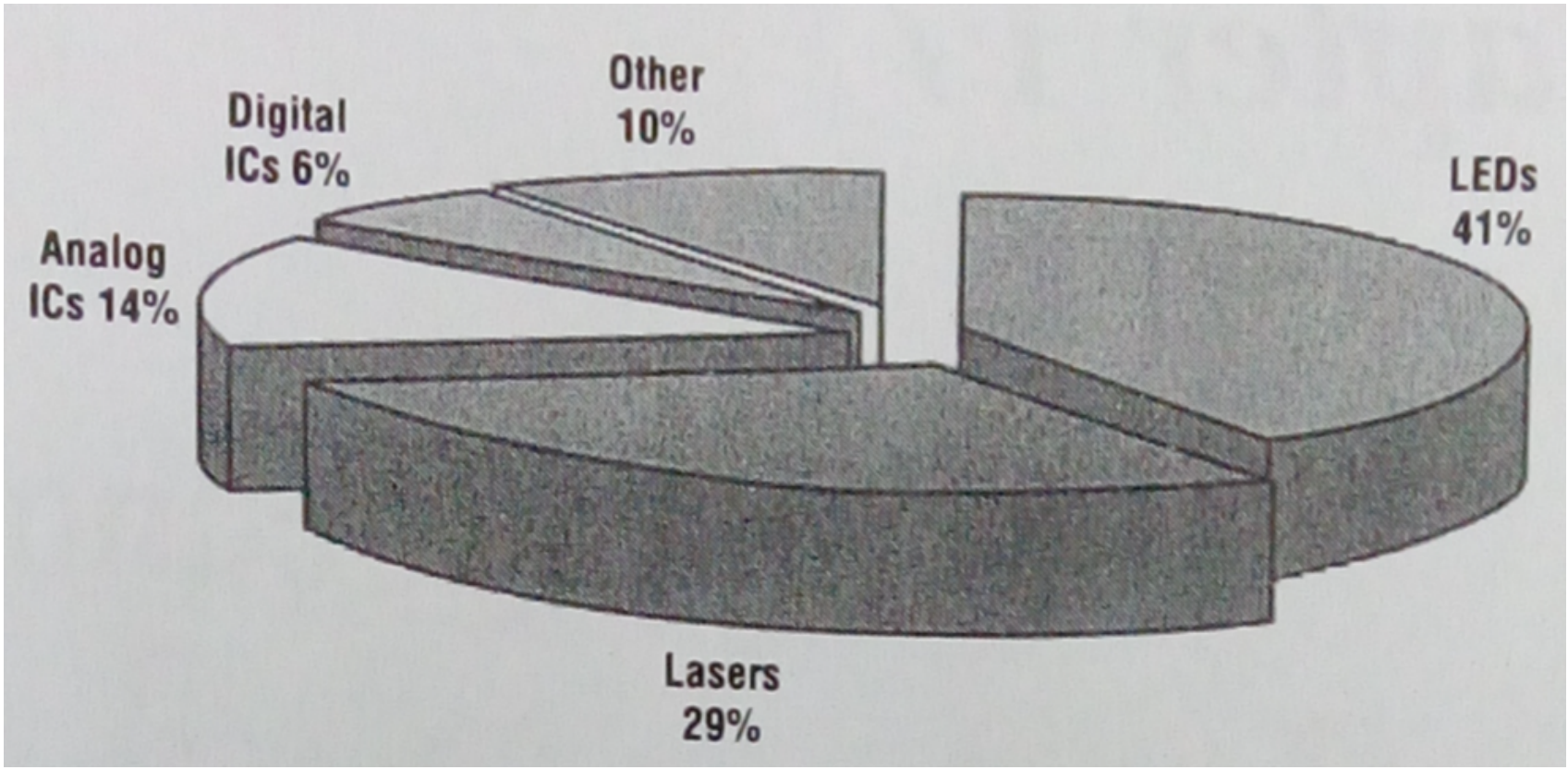
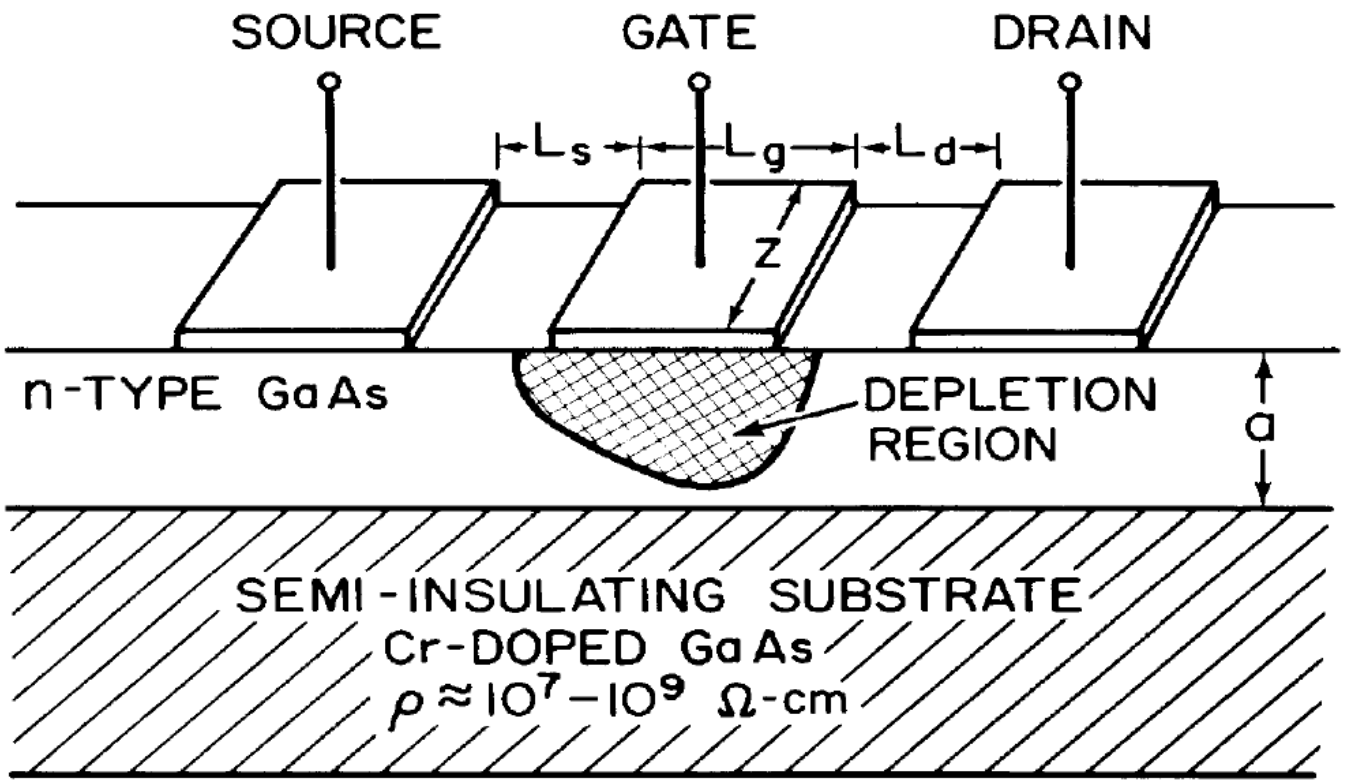
Why Gallium Arsenic ?

- It can be made in form of a very high resistivity semi-insulating substrate. (adv: cuts down capacitances, can be used for high-speed analog applications)
- Low field electron mobility is large (so can make fast devices)
- GaAs is amenable to the growth of heterojunctions.
- Its is a direct band-gap material (this mean that EHP recombination is likely to give off a photon). Hence, popular for making various light emitting structures.

Application Share



Basic MESFET operation

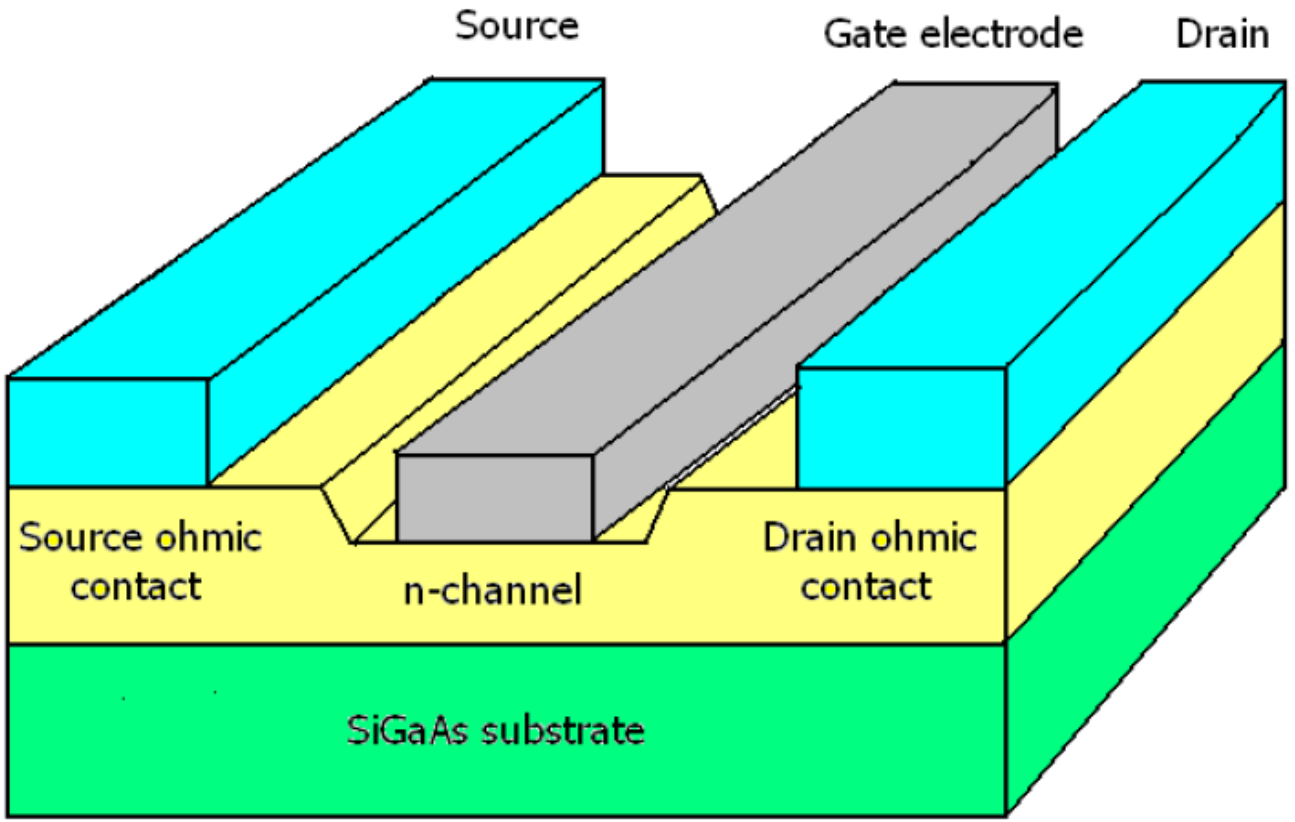


Basic MESFET operation

- N-channel MESFETs are used almost exclusively
- Threshold voltage of MESFET is simpler than that of MOSFET (since there is no oxide to supports a voltage drop)
- For a D-mode MESFET, $V_T = V_{bi} - V_{po}$
- $V_{bi} = \frac{qN_DW^2}{2\epsilon}$ $V_{po} = \frac{qN_Dt^2}{2\epsilon}$

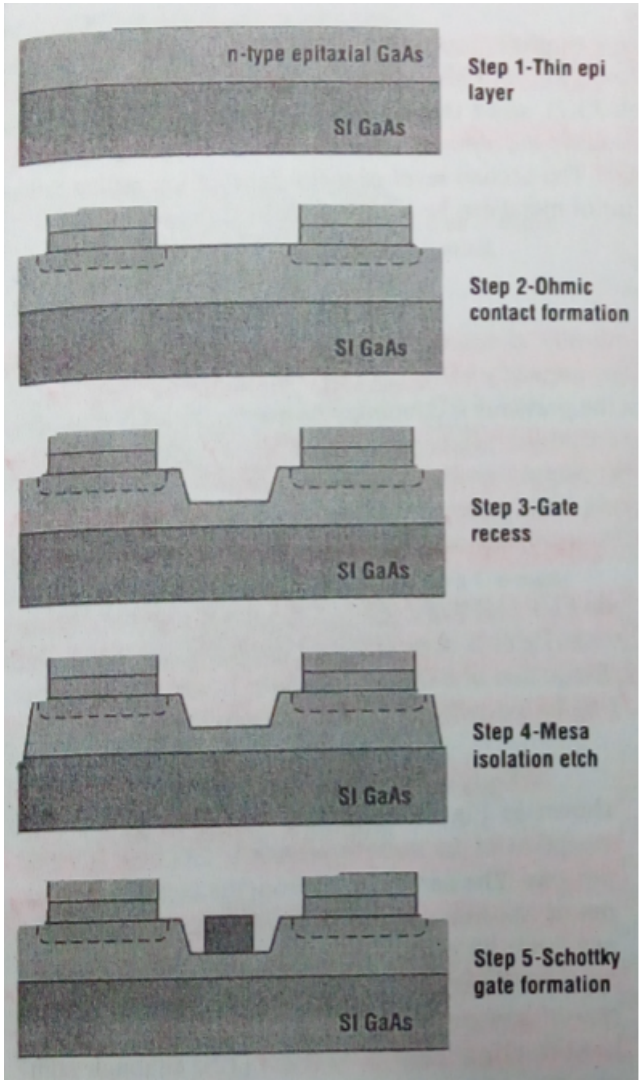
Basic MESFET operation

- I-V characteristics of MESFETs → similar to MOSFETs



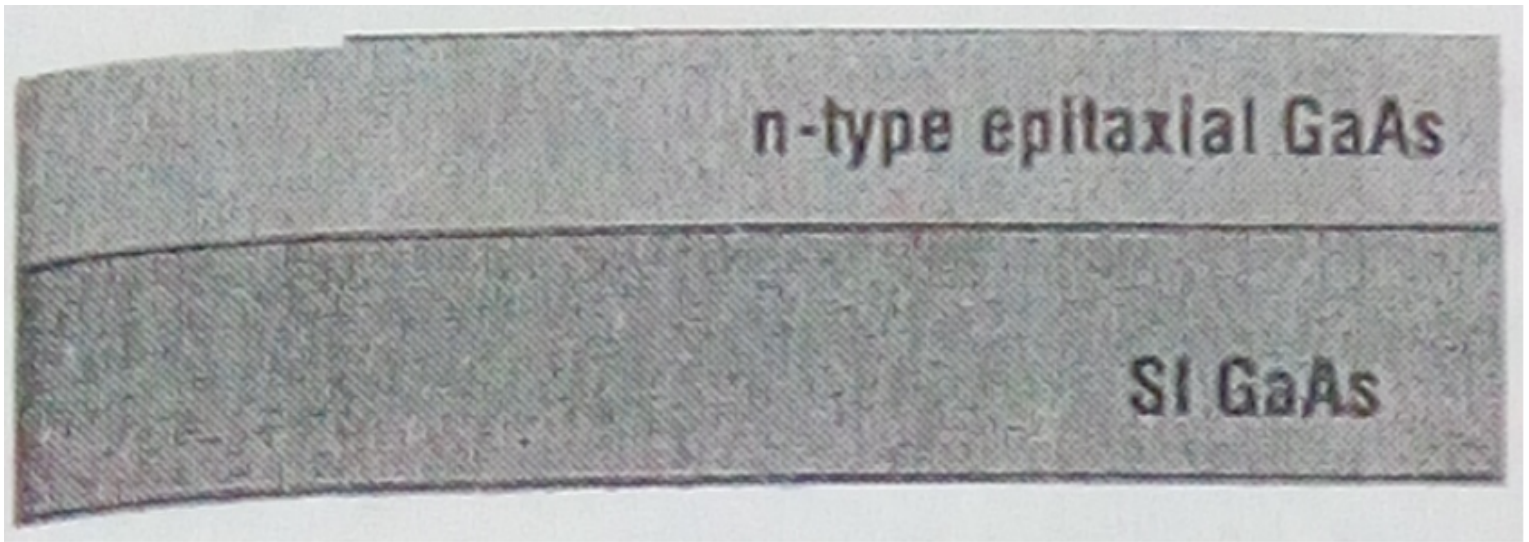
Process flow

- Process flow → D-mode GaAs MESFET technology
- Three or five masking levels → one or two levels of metals needed



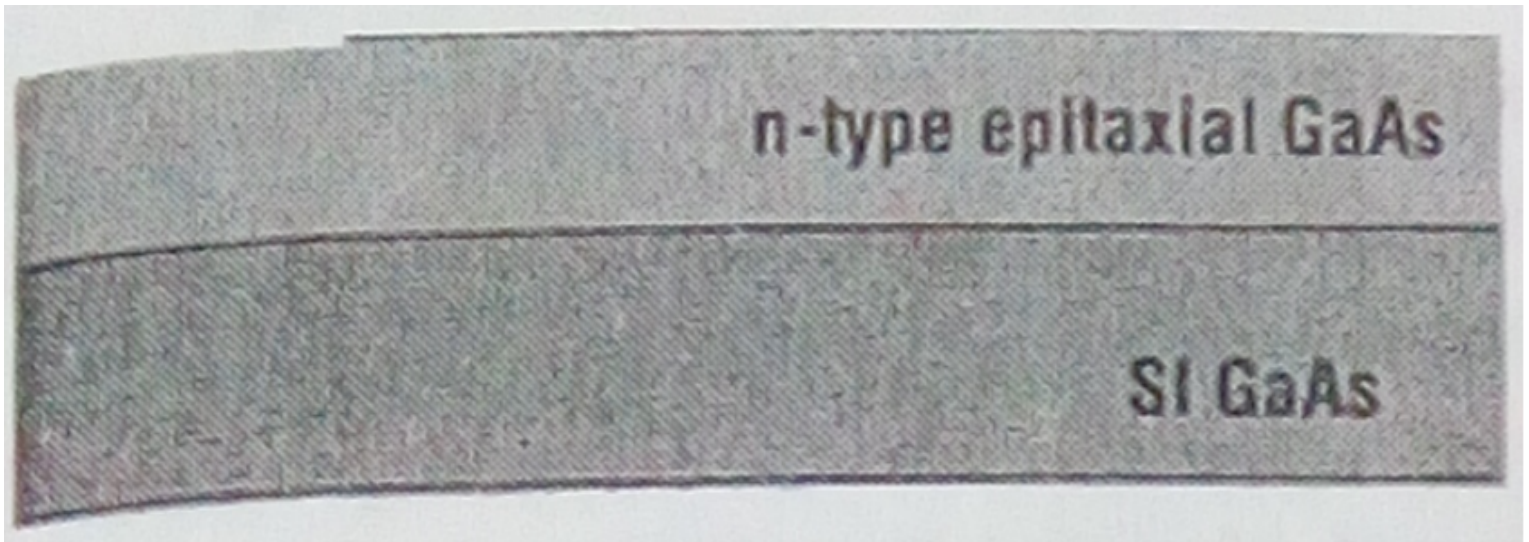
Process flow

- 1st semi-insulating GaAs substrate → coated with thin layer of Si_3N_4 and then implanted with Si.
- Nitride layer → protects wafer from contaminations during implant and → serves as a barrier to the out diffusion of arsenic.



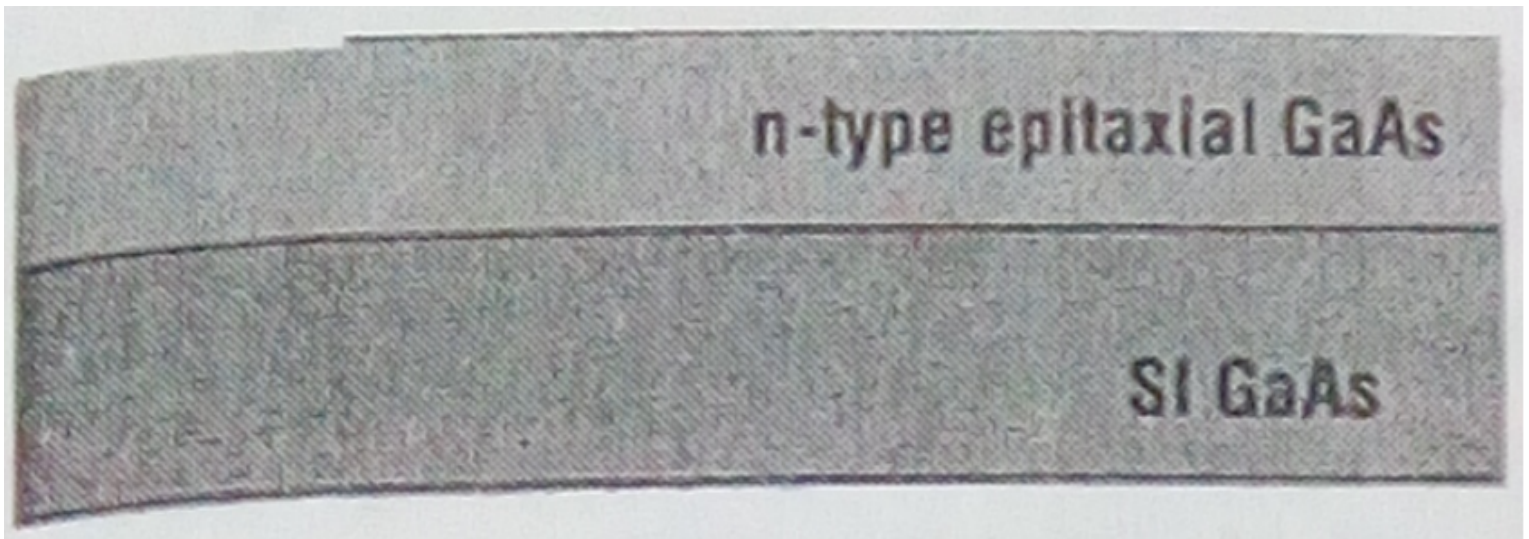
Process flow Step 1: Thin epi layer

- Implanted of Si forms active layer.
- Si implant heavily doped $\rightarrow$ 1 to 6 $\times 10^{17} cm^{-3}$
- Implant activated at high temperature anneal.
- Activation done $\rightarrow$ Furnace or in a rapid thermal processor.
- Furnace activation spec's $\rightarrow 850^{o}C$ for 20 minutes.



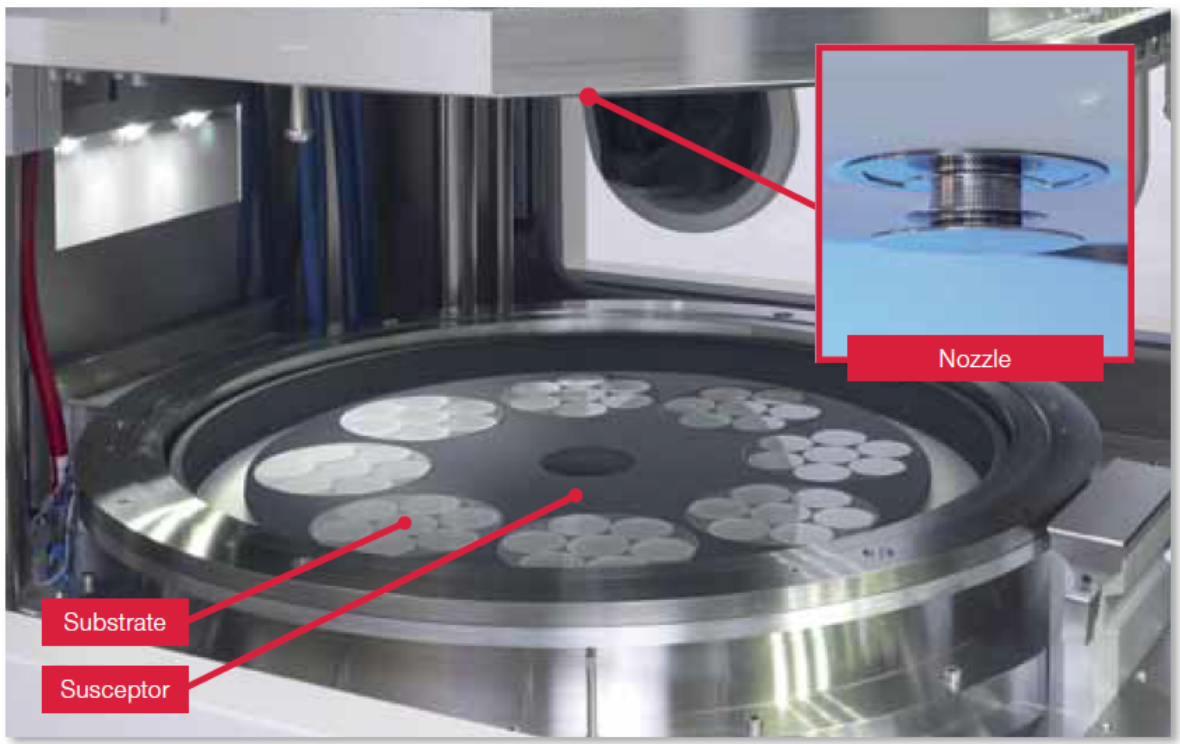
Process flow Step 1: Thin epi layer

- Following the anneal → nitride is removed.
- Alternatively, conducting channel → epitaxial growth.
- N-epitaxial layer is grown by either → Metal organic Chemical vapor deposition (MOCVD) or Molecular beam epitaxy (MBE).



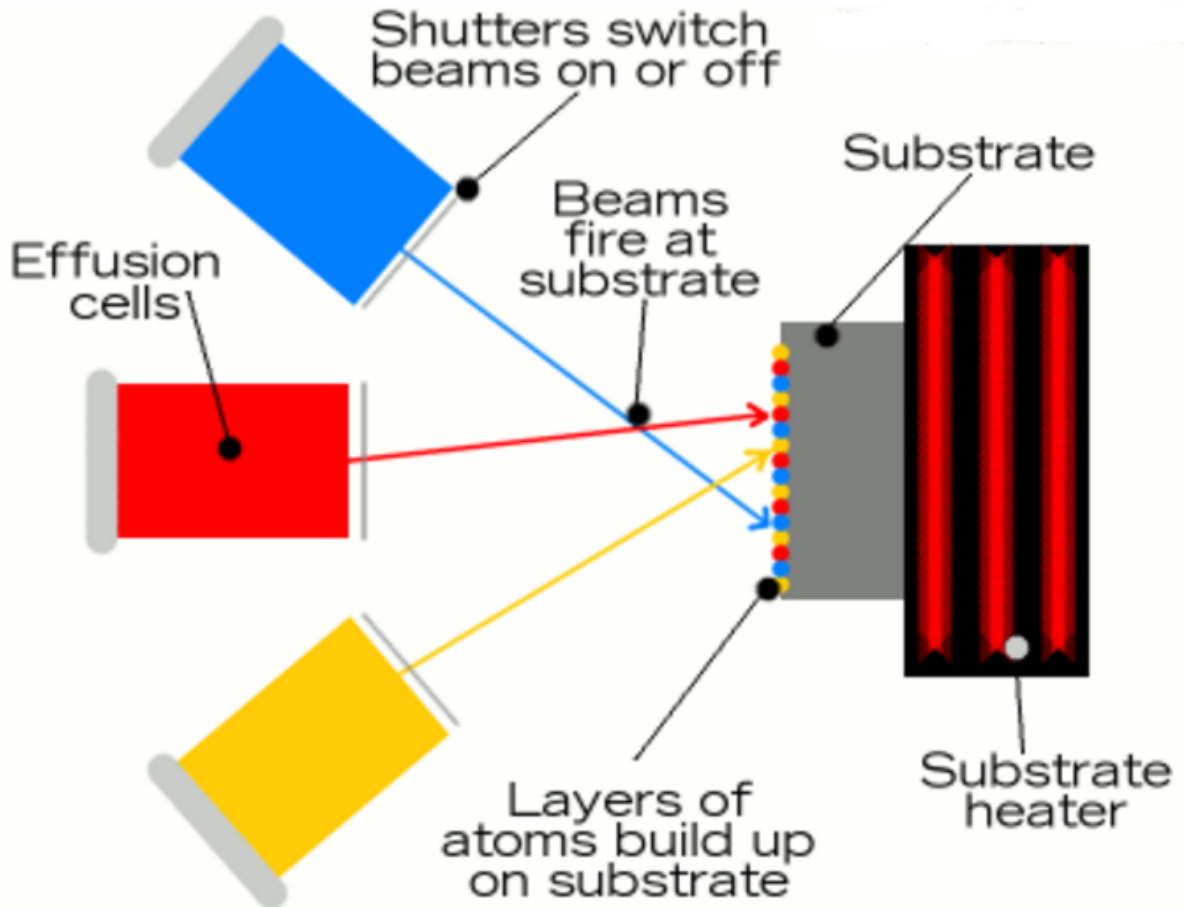
MOCVD

- This is a technique for depositing thin layers of atoms onto a semiconductor wafer.
- Using MOCVD you can build up many layers, each of a precisely controlled thickness, to create a material which has specific optical and electrical properties.



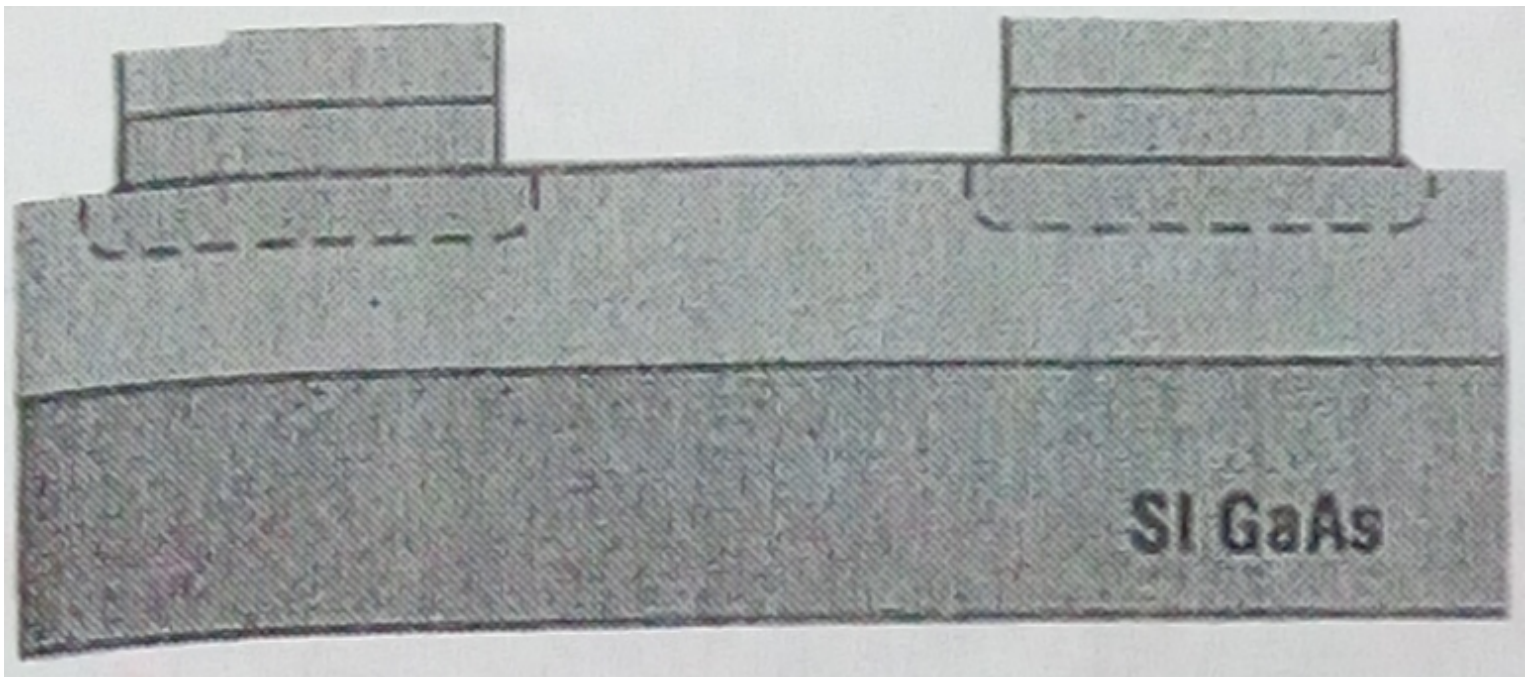
MBE

- Technique to grow crystalline thin films in ultrahigh vacuum (UHV) with precise control of thickness, composition and morphology



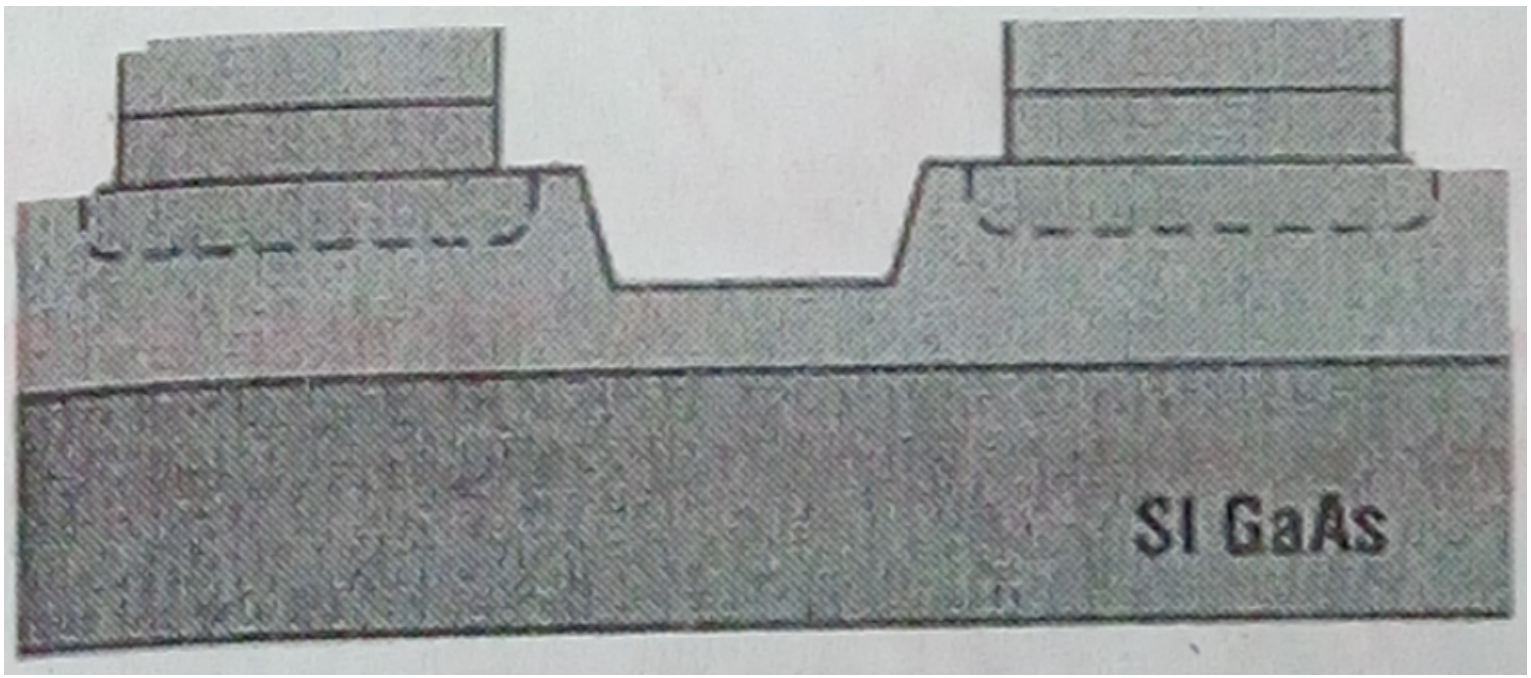
Process flow Step 2: Ohmic contact formation

- Diffused ohmic contacts are then formed by evaporating Ni/AuGe sandwich using a lift-off process.
- Contacts are sintered at 450^{o}C
- Source-to-drain contact separation $\rightarrow$ 3 to 4 μm



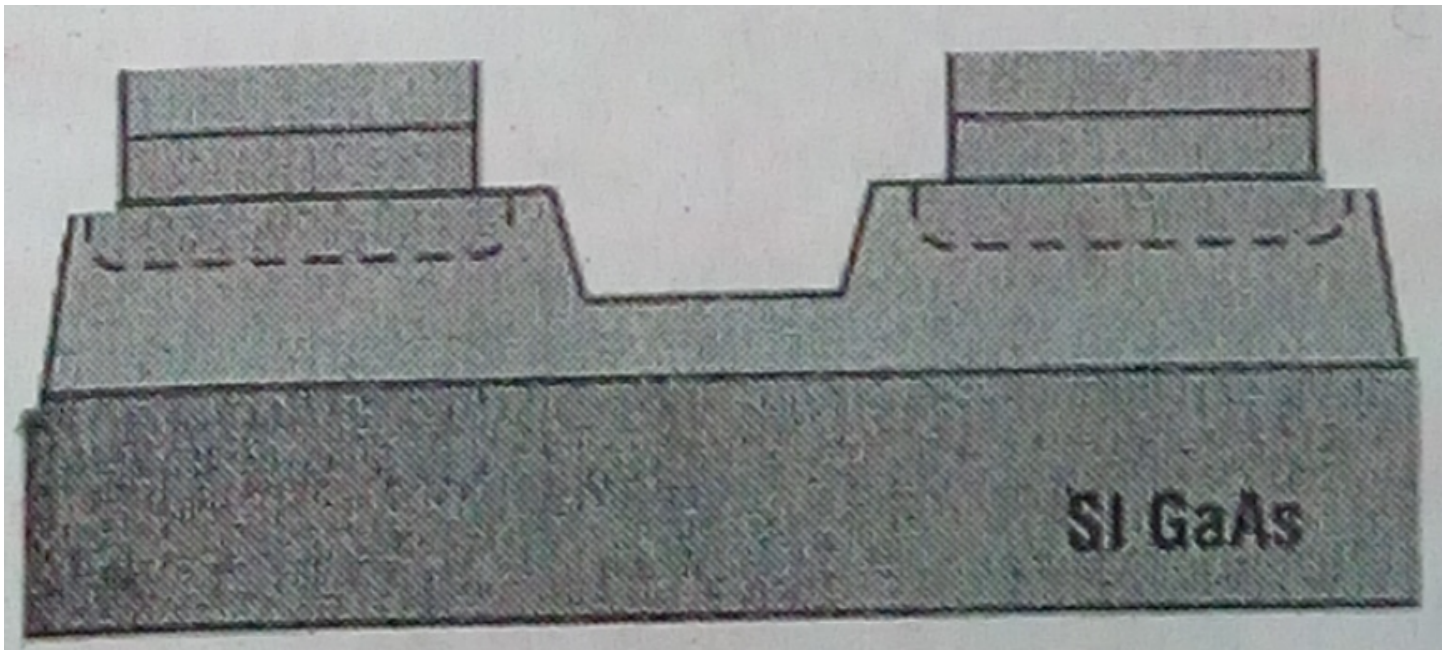
Process flow Step 3: Gate recess

- Next, gate recess → chemical etching.

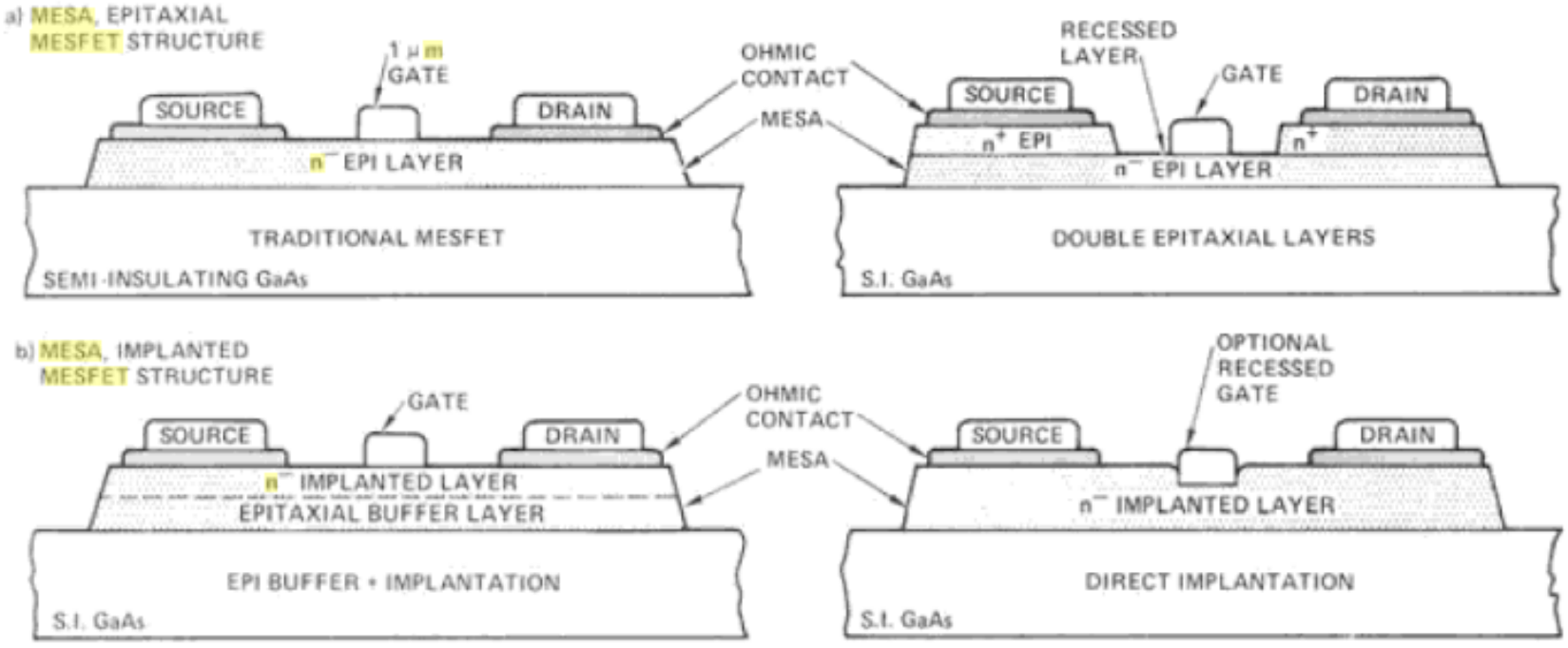


Process flow Step 4: Mesa isolated etch

- Next, the mesas are isolated → wet chemical etching the field regions through the active layer to the SI substrate.
- At this point, pinch-off voltage V_{po} characteristic is measured using mercury probe.
- To adjust pinch-off voltage → recess the channel to the desired value.

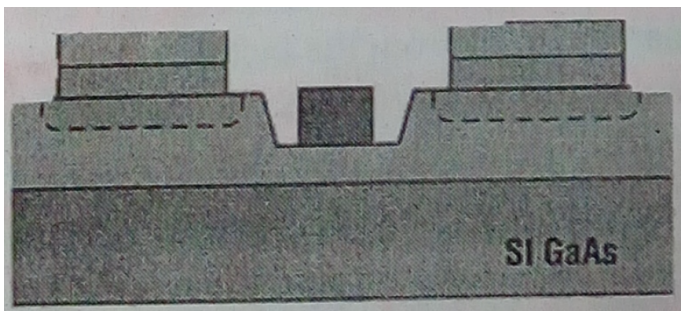


MESA ISOLATED MESFET

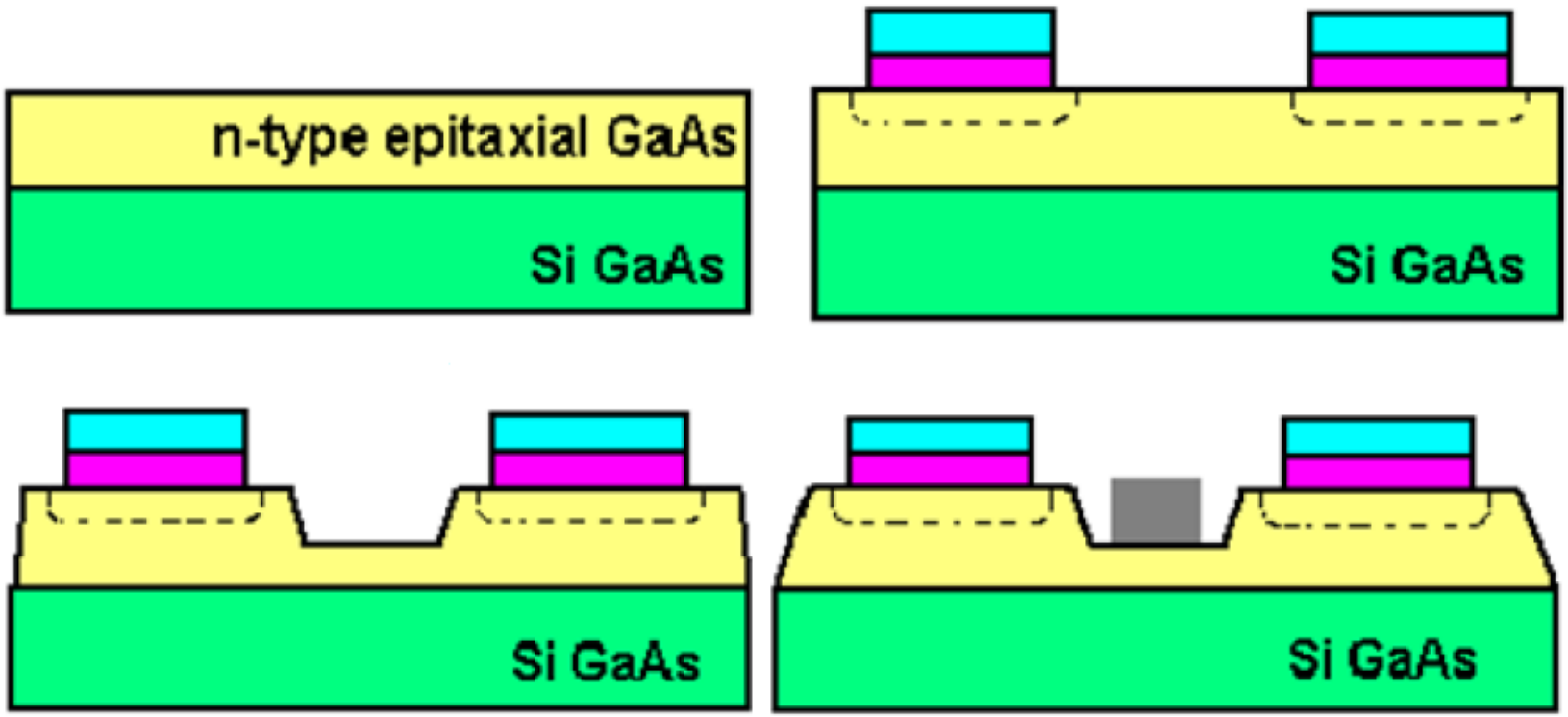


Process flow Step 5: Schottky gate formation

- Schottky gate electrode is deposited.
- Metal must have excellent adhesion to GaAs.
- Popular gate metals for MESFET's → Titanium/platinum/gold Ti/Pt/Au and Titanium/palladium/gold Ti/Pd/Au (Metal Stack)
- Schottky barrier metal is v.thin → $500 - 1000^{o}A$
- Gold serves as low resistance interconnect → $2000 - 5000^{o}A$
- Metal Stack → applied at top of ohmic contact → lowers series resistance.
- 2^{nd} layer of interconnect added is required.



Process flow: Mesa-isolated MESFET.

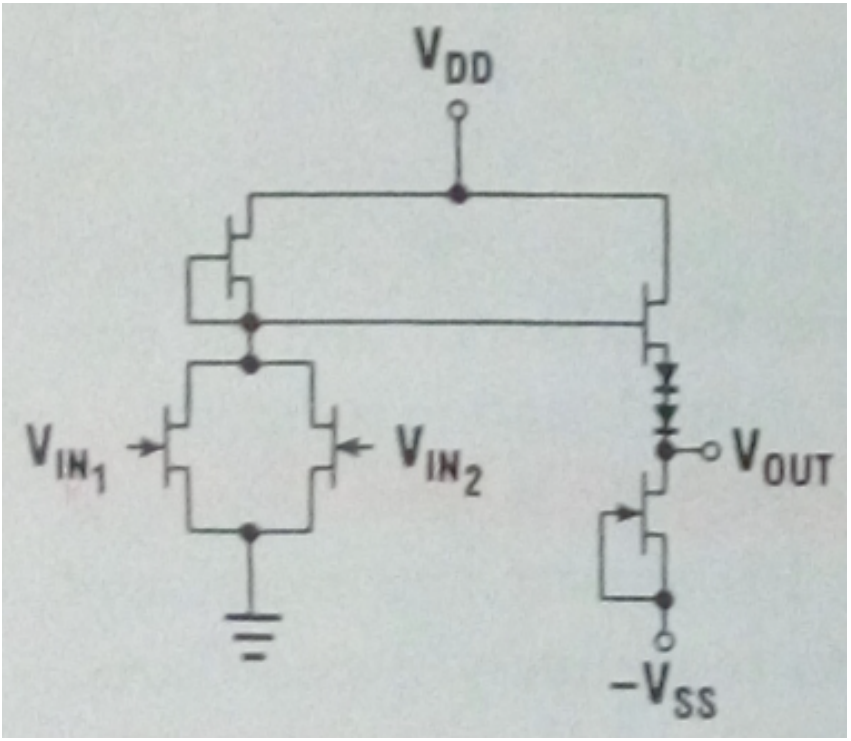


Digital Technologies

- Three design approaches commonly used in GaAs integrated circuits.
- Buffered FET logic (BFL)
- Schottky diode FET logic (SDFL)
- Direct coupled FET logic (DCFL)

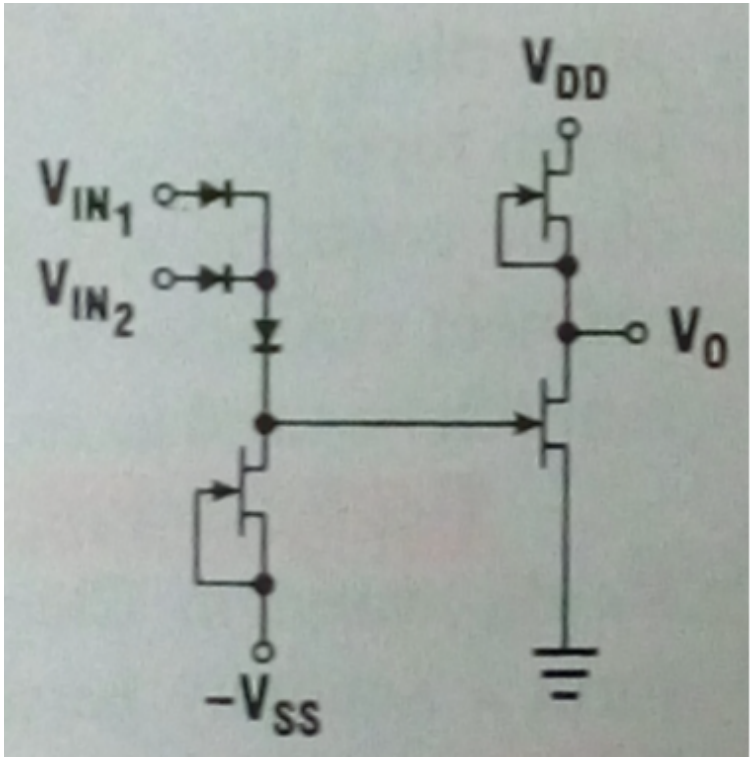
Buffered FET logic (BFL)

- Fastest
- Highest power approach
- Level shifting → 2 diodes near the output → To shift O/P back to I/P level
- Large power dissipation (>5mW per gate)
- Large area require to lay out a gate
- Restricted to small and medium levels of integration



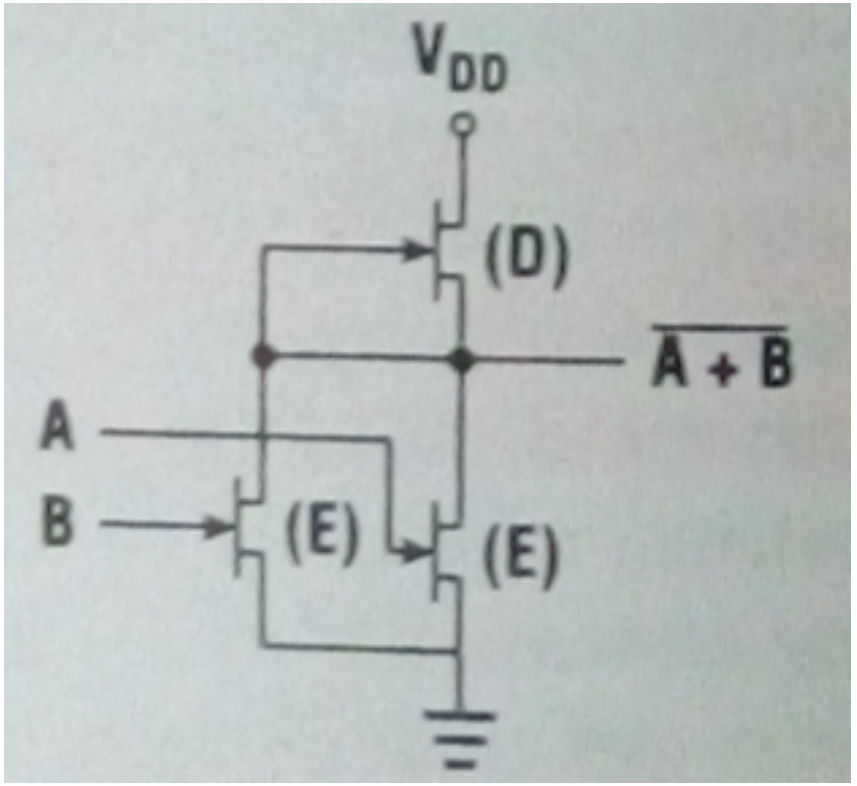
Schottky diode FET logic (SDFL)

- Level shifting → necessitated by use of D-mode FETs
- Level shifting → by diodes at input stage
- Power dissipation (∼5mW per gate)
- Gate delay → twice as large as BFL
- Due to reduce power consumption → ICs with 1000 gates can be built.



Direct coupled FET logic (DCFL)

- Least power consumption < 0.5mW per gate
- O/P of basic inverter structure does not involve any diode drops.
- Thus no level shifting is required.
- Compact layout.
- Noise margins $\rightarrow$ small.
- Gate delays larger than SDFL
- Can make ICs over 65,000 transistors per chip.



Digital Technologies processing

- Direct coupled FET logic (DCFL): Most popular approaches for VLSI GaAs
- DCFT requires simultaneous fabrication of *enhancement* and *depletion* mode transistor.

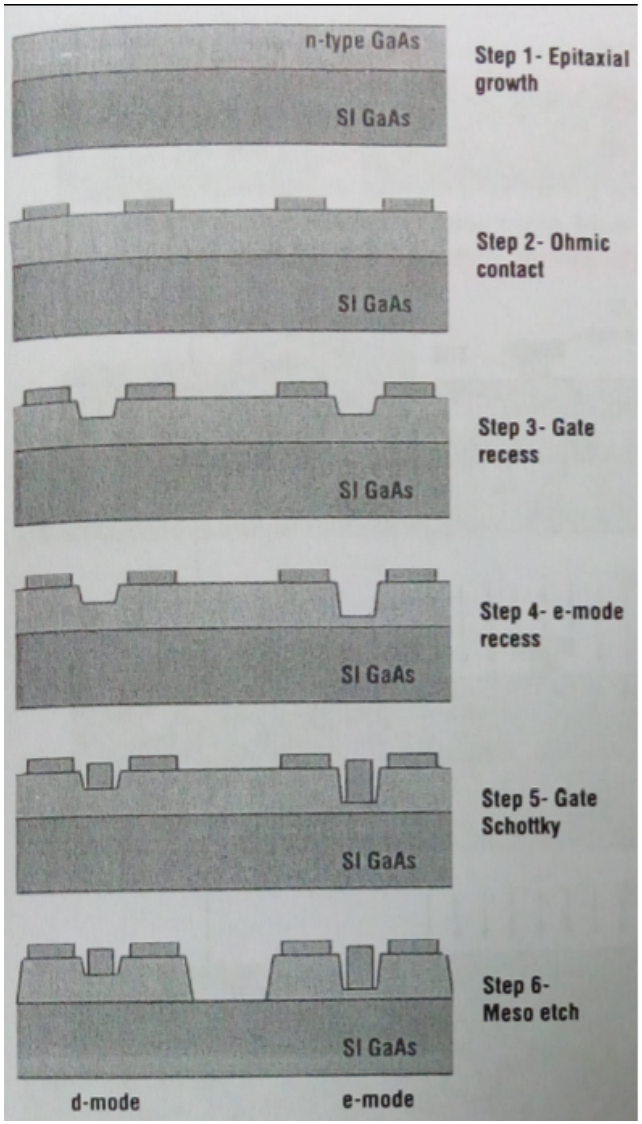
Digital Technologies

$$V_{bi} = \frac{qN_D W^2}{2\epsilon} \qquad V_{po} = \frac{qN_D t^2}{2\epsilon} \qquad V_T = V_{bi} - V_{po}$$

- Threshold voltage V_T for MESFET depends on
  a) Build in voltage V_{bi}
  b) Dopant concentration in the channel N_D
  c) Channel thickness t
- In principle, any of these 3 parameters could be varied in order to achieve an E/D technology. (Varying the channel thickness was initially most popular)

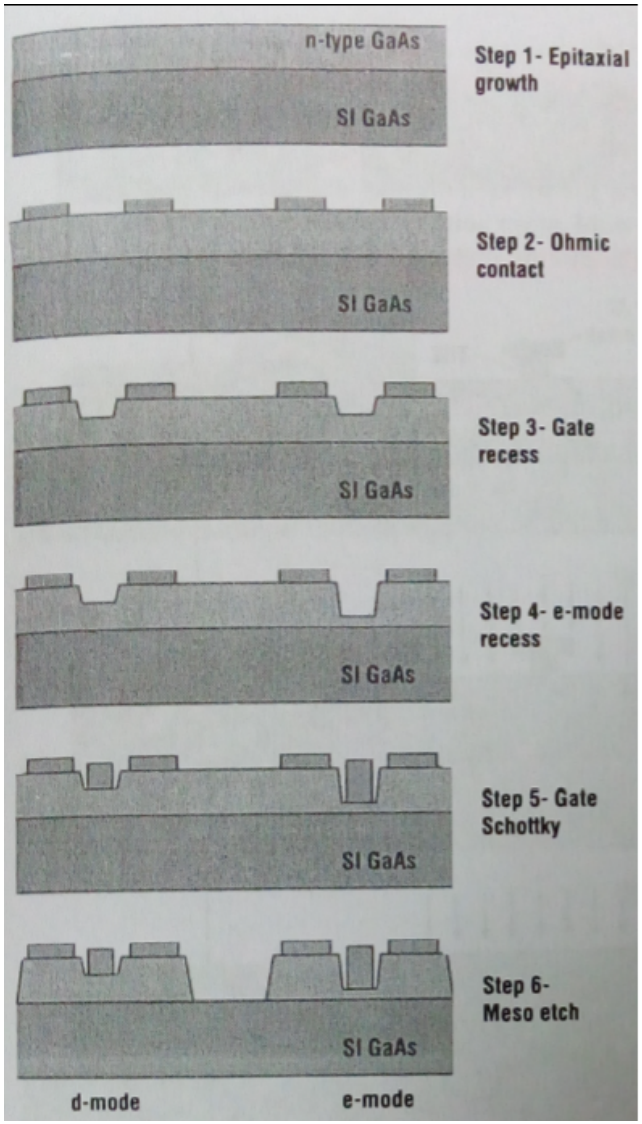
Selective recessing: Etched E/D technology

- Both the devices are recessed to the thickness desired for the D-mode transistors.
- D-mode transistors → masked off with photoresist.
- E-mode transistors are further etched → desired pinch-off voltage.



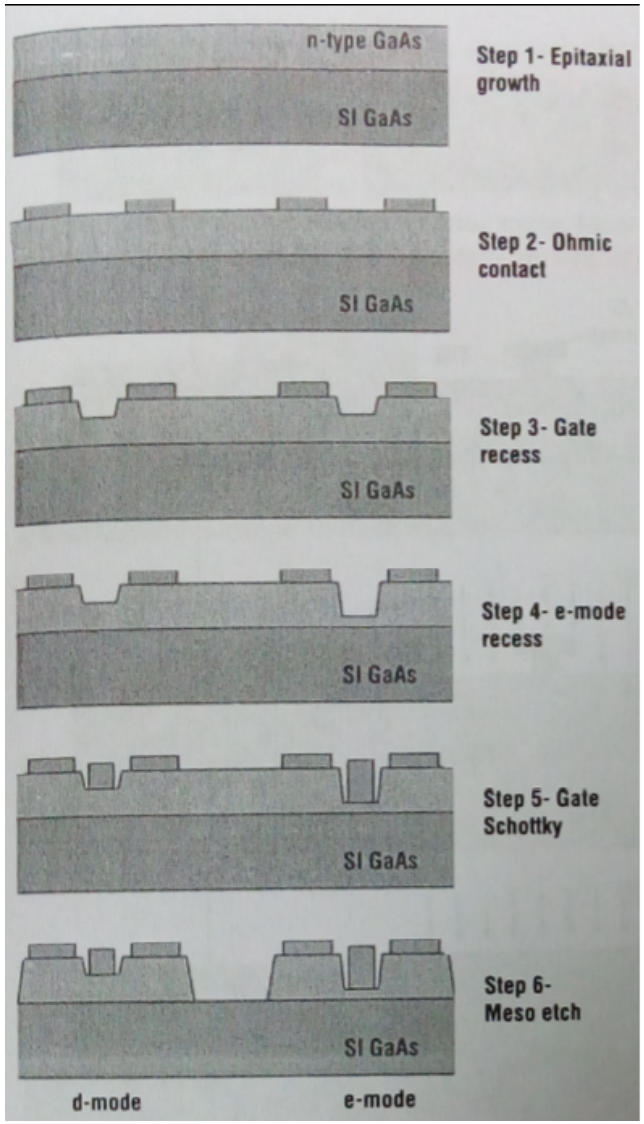
Selective recessing: Etched E/D technology

- **Difficulty**:
  a) DCFT have smaller noise margins, thus requires careful control of the pinch off voltage. (V_{po} varies as square of thickness)
  b) Wet chemical etching to achieve recess is non-uniform.
- Alternate approach to selective recessing $\rightarrow$ Selective implantation.



Selective recessing: Etched E/D technology

- Initial implant replaced by lower concentration implant → to set E-mode threshold.
- E-mode devices areas → masked off.
- D-mode devices → given additional implant to achieve → desired threshold.
- Advantage: Improved uniformity.
- Widely used for E/D technologies.



MESFET PROCESS: NOT SELF ALIGNED ?

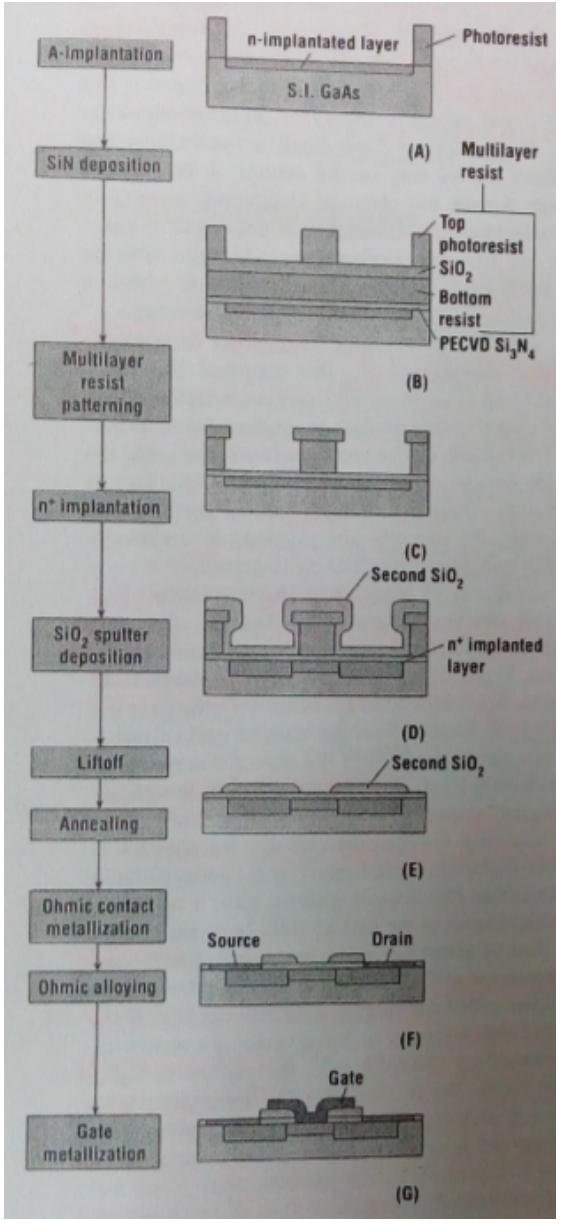
- For MOSFETs, the transistor performance can be degraded by the presence of a series resistance between the source and the drain metal.
- In MESFET GaAs technology , this is MORE severe since the traditional MESFET process is not SELF ALIGNED.
- Primary difficulty in forming self-aligned S/D structures is the lack of insulating layer between the gate and the channel.
- Solution → Use Advanced Gate structures in GaAs such as **Self-aligned gate FET** (SAGFETs).

Self aligned techniques

Two methods of producing self-aligned source/drain contacts to the channel.

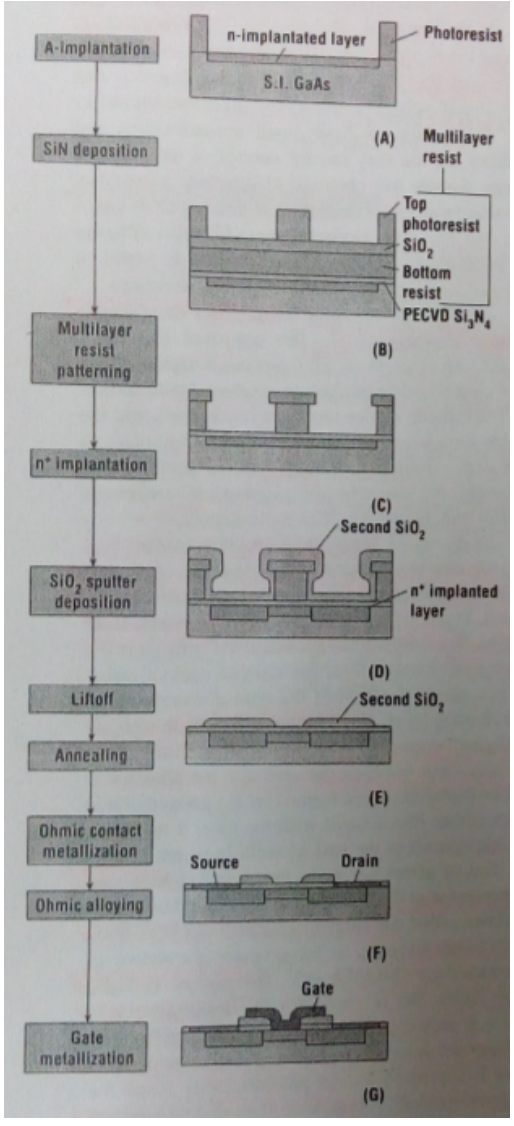
- Self-aligned implantation N^+ technology (SAINT)
- T gate approach

Self aligned implantation N^+ technology



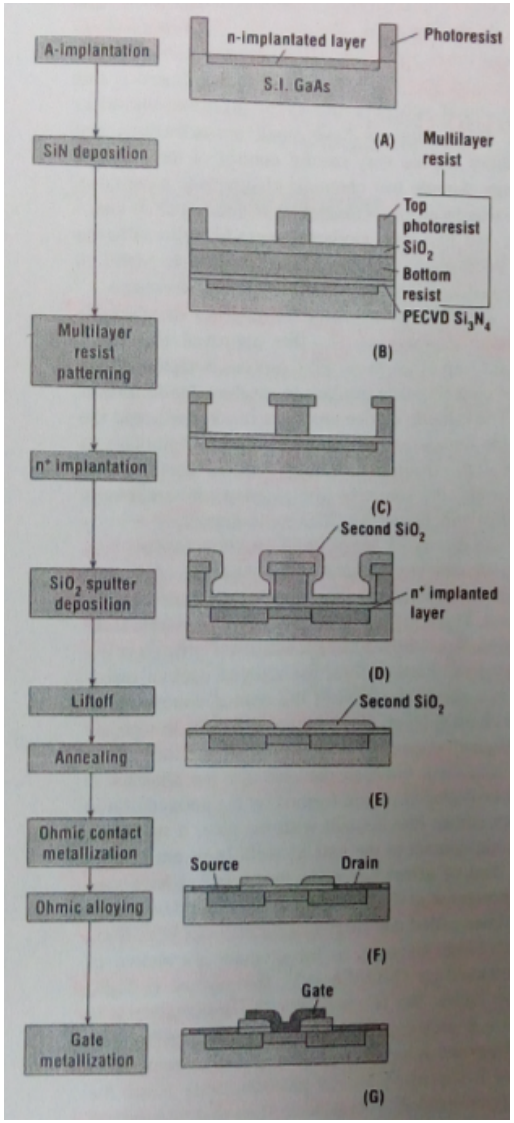
Self aligned implantation N^+ technology

- Surface is passivated with Si_3N_4
- Tri-layer resist sandwich $\rightarrow$ define N^+ implant
- Bottom resist is undercut between 0.1 and 0.2 μm per side
- A dielectric is deposited at low temperature
- Dielectric is lifted off to define the gate region

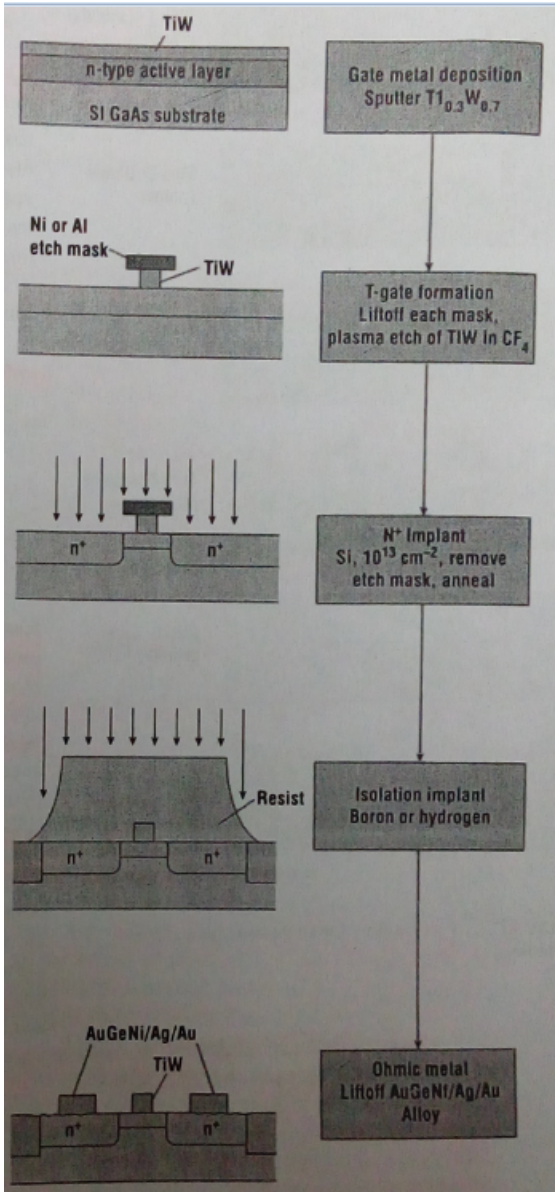


Self aligned implantation N^+ technology

- A high temperature anneal is done to activate the N^+ implant
- A Schottky metal is deposited next for the gate electrode
- Advantages:
  a) Excess leakage is avoided, as dielectric isolates the N^+ from the gate
  b) Process flow does not expose the gate electrode to a high temperature step

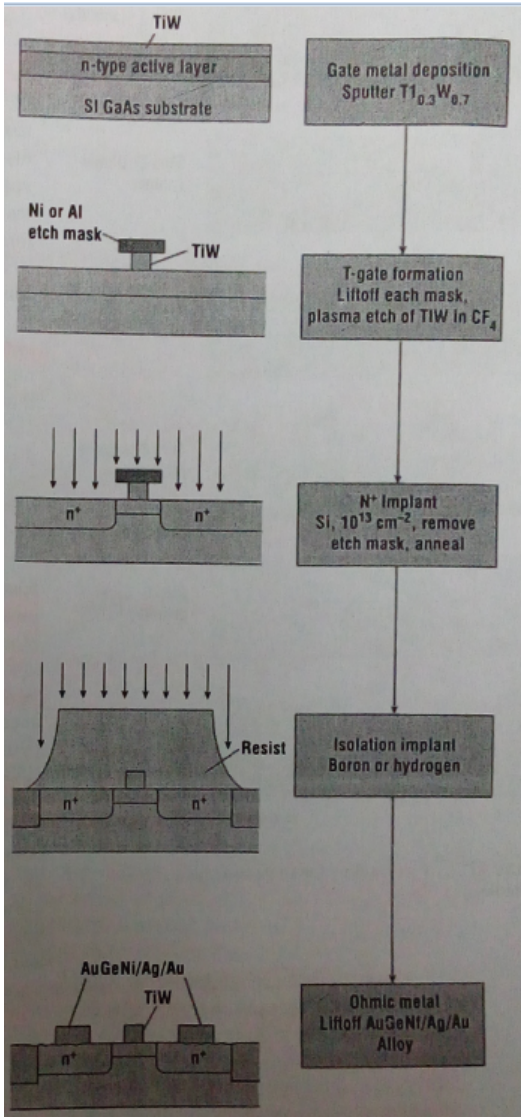


T gate process



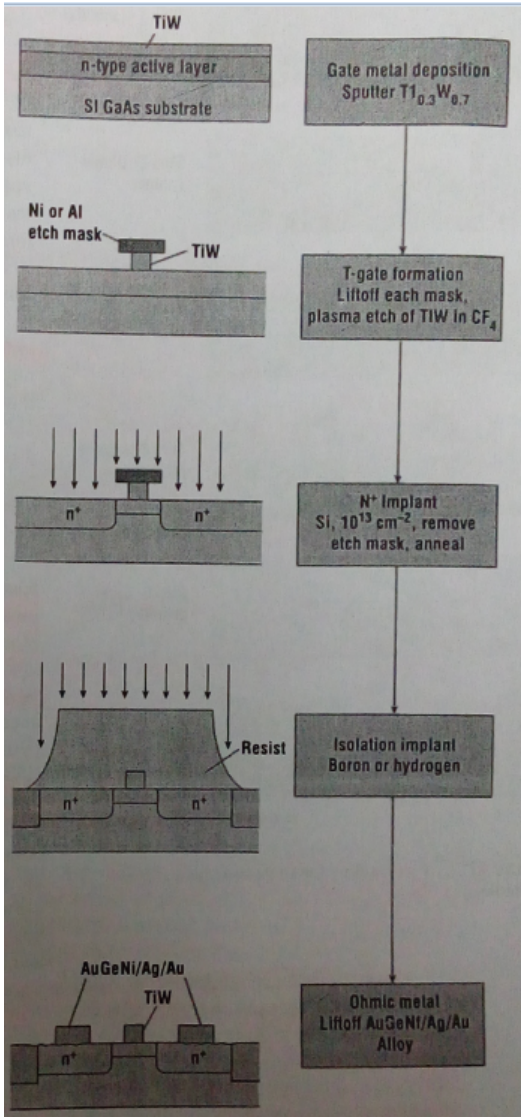
T gate process steps

- Procedure similar to traditional Si technologies.
- Schottky metal applied first.
- 2^{nd} layer above metal may be another metal or may be photo-resist itself.
- Bottom resist is undercut between 0.1 and 0.2 μm per side
- N^+ implantation is next.



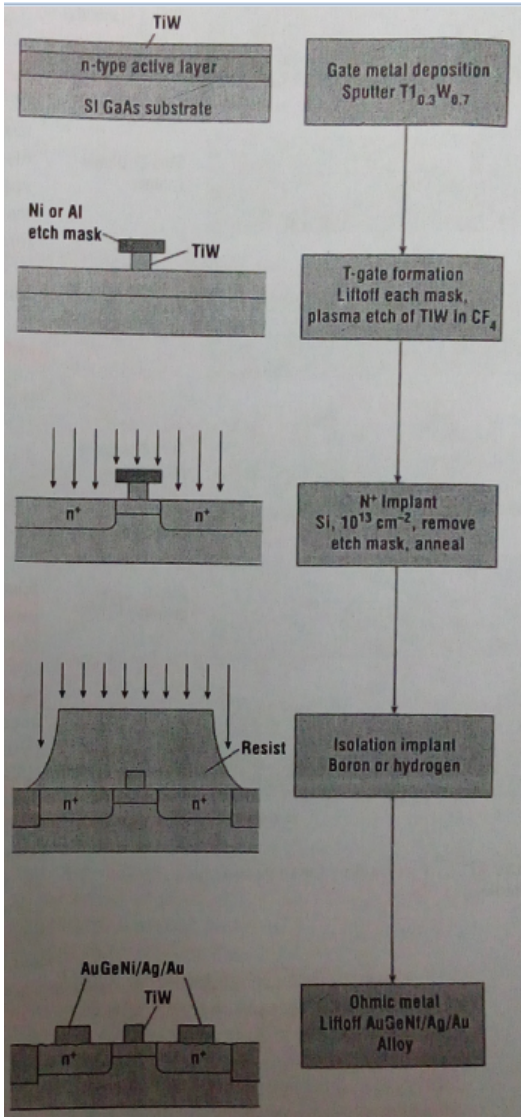
T gate process steps

- Upper masking layer is then removed and a thin Si_3N_4 anneal capping layer is deposited
- Implant is then activated and the nitride patterned to allow the ohmic contact formation
- Ohmic metal is deposited and annealed

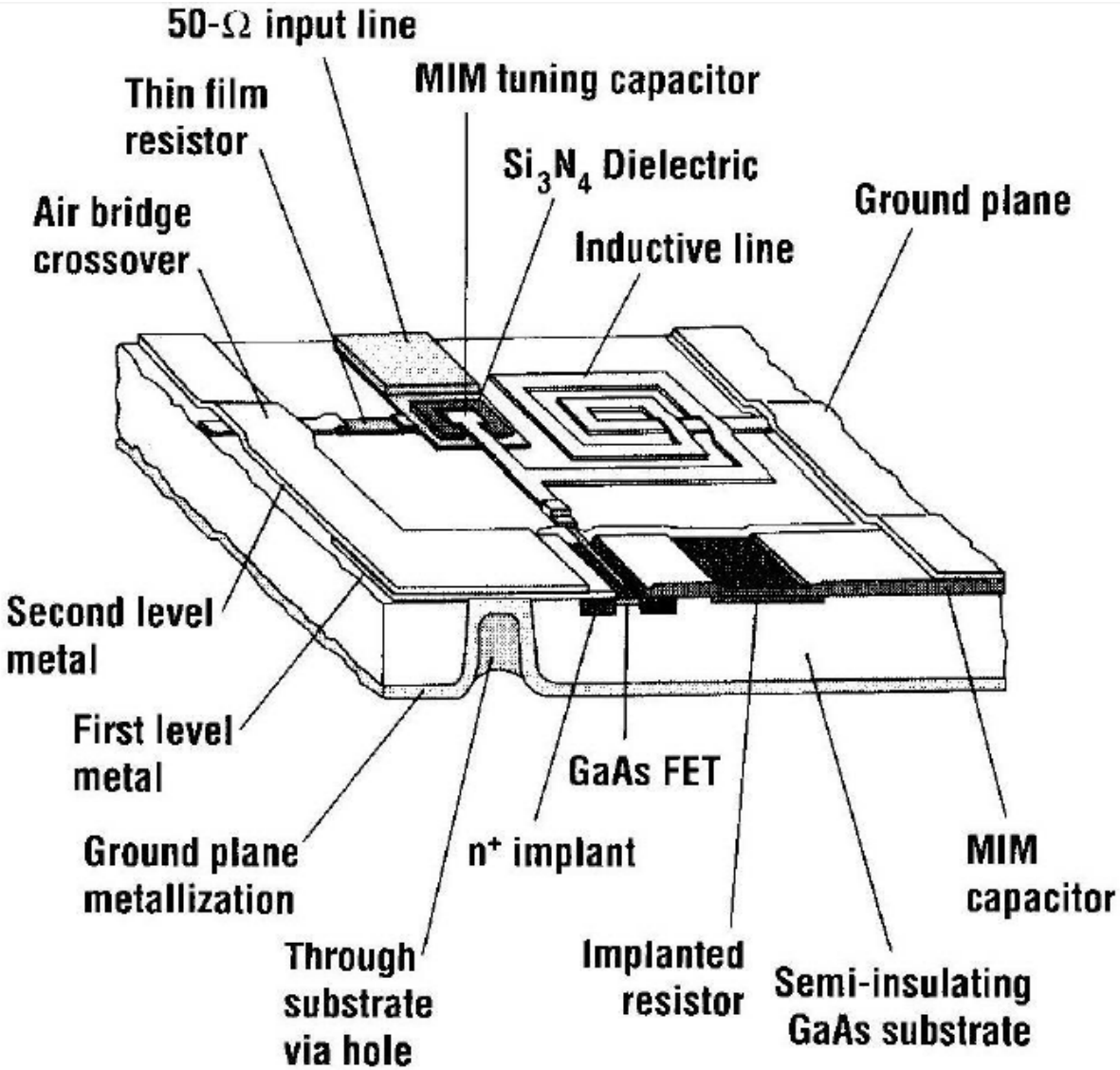


T GATE PROCESS STEPS

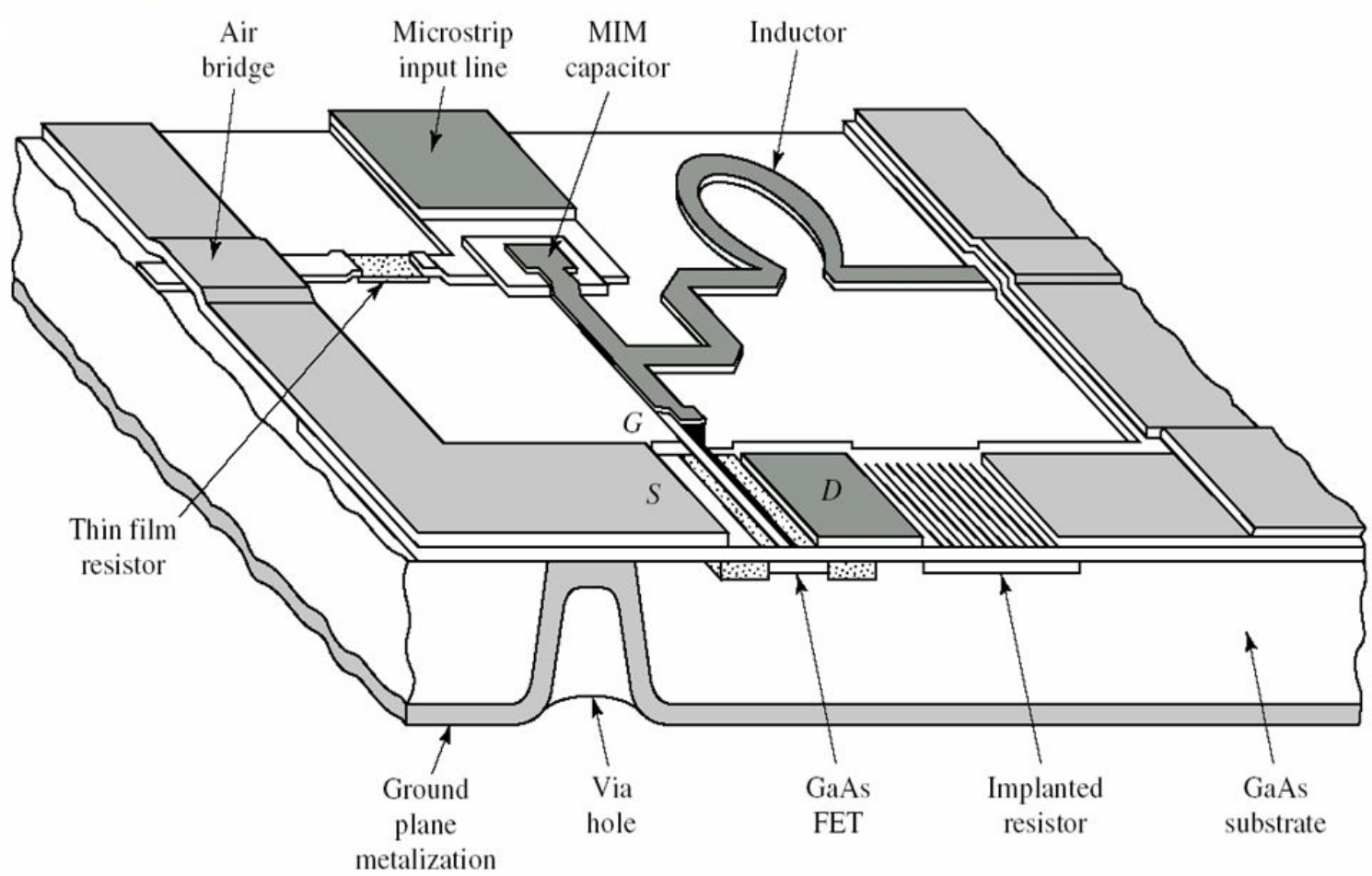
- **Limitations**: Difficult to a find suitable Schottky gate material that will tolerate the high temperature implant activation cycle.
- Most the materials used are refractory metals (ability to withstand heat)or their silicide.
- Popular choices : WSi_2 and $PtSi$



Monolithic Microwave Integrated Circuit(MMIC) Technologies

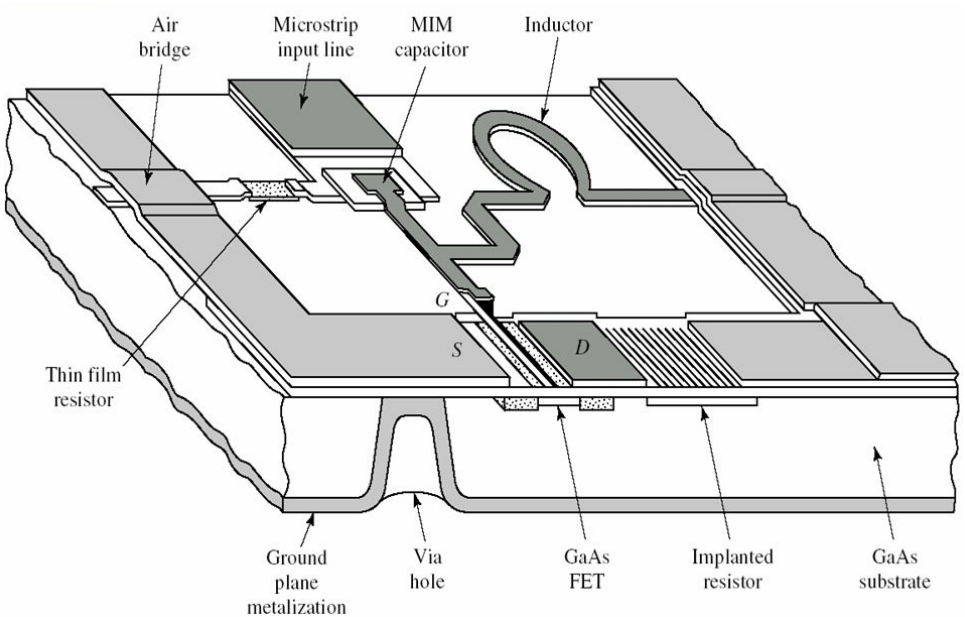


Monolithic Microwave Integrated Circuit(MMIC) Technologies



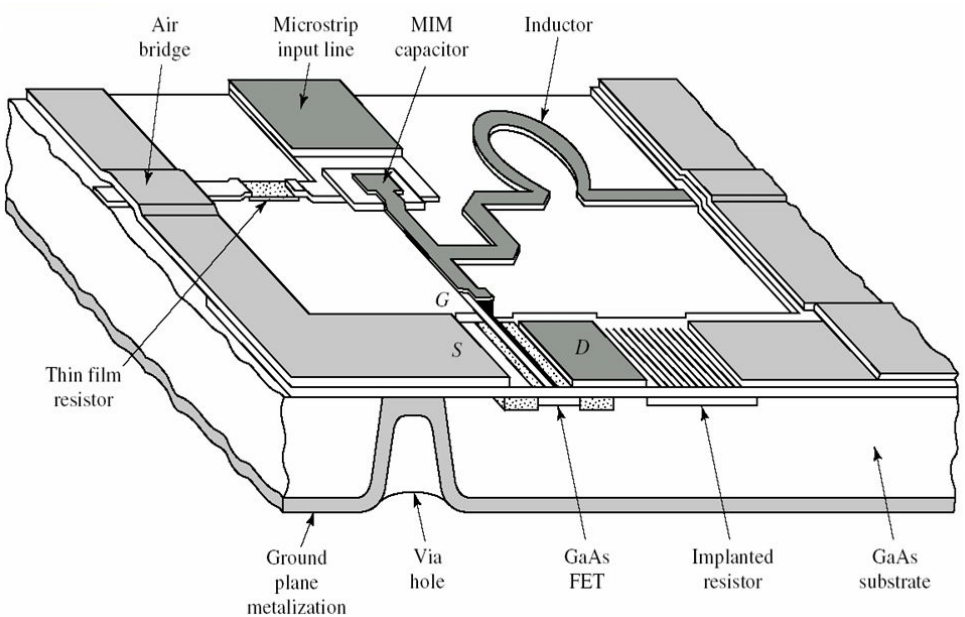
MMIC Technologies

- Covers broad range of circuits range from power amplifier to mixers to transmit/receive modules.
- **Applications:** Cellular phone, direct-broadcast satellite, data links, cable television CATV, radar transmission and detection, and automobile collision avoidance system, etc.



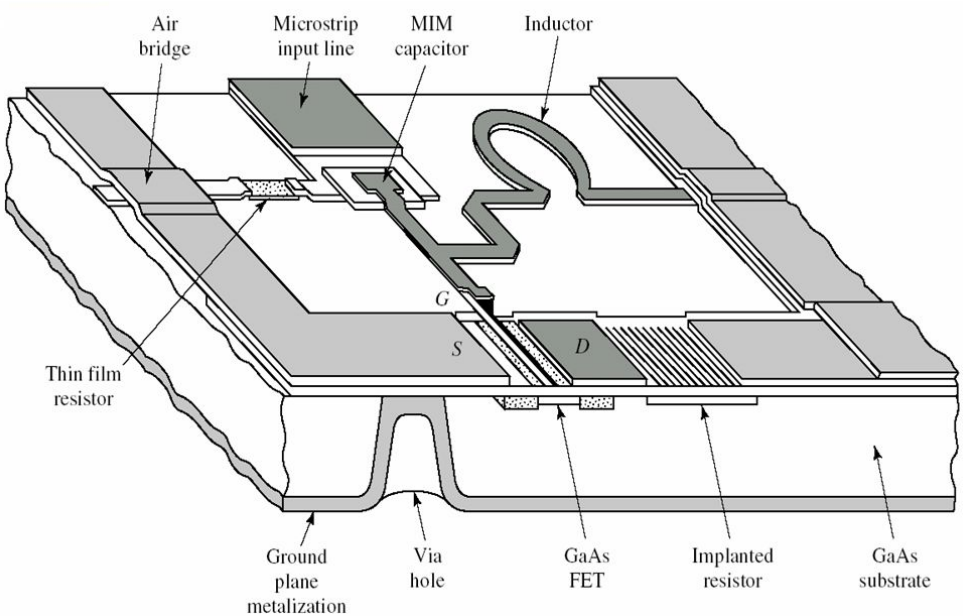
MMIC Technologies

- A typical MMIC consist of some common components such as:
  a) metal insulator
  b) metal MIM capacitor
  c) tuning capacitor
  d) chip resistor
  e) GaAs field effect transistor etc.



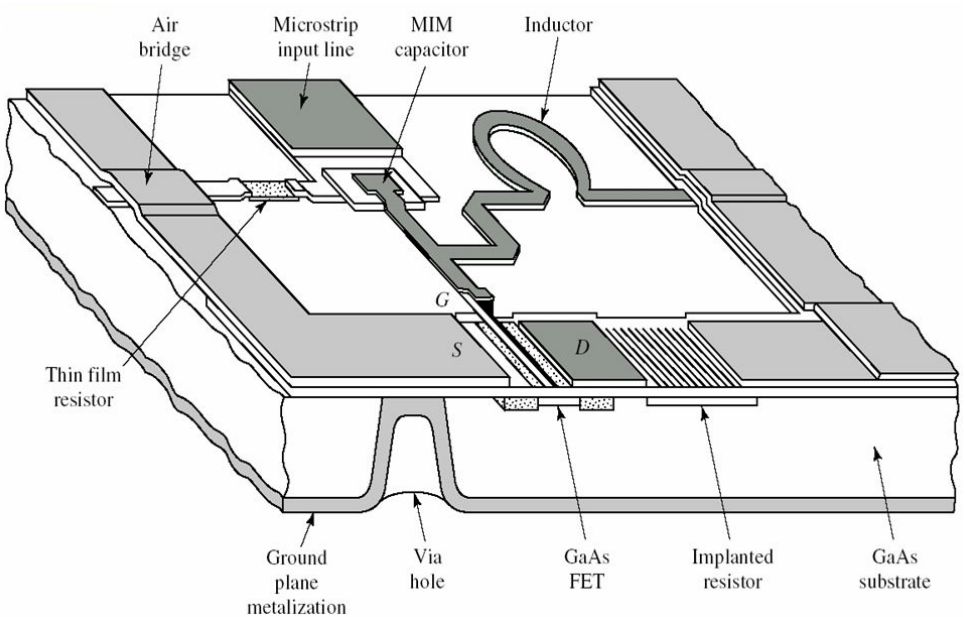
MMIC Technologies

- MMIC's begins with the base metal semiconductor field effect transistor.
- The gate electrode may be non-centered..
- For power application, comb structure may be used for the gate electrode.
- Crucial design aspect → very short L knowing that the unity gain frequency f_T is inversely proportional to the L.



MMIC Technologies

- Short channel length → low noise figure.
- Since the number of transistor count in MMICs is *low*, it is usually fabricated with electron-beam lithography.

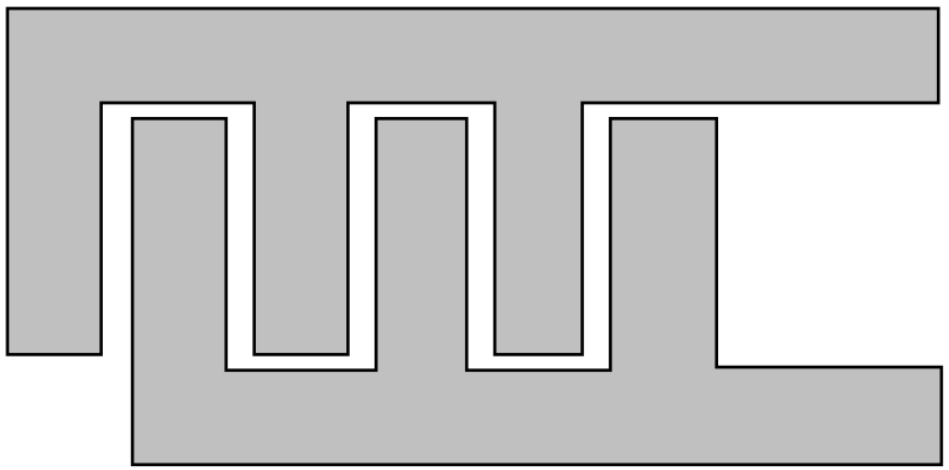


Analog components in MMIC

- Many analog circuits require the use of capacitor and inductor.
- They are used:
  a) To adjust the signal phase.
  b) For impedance matching the source and load.
  c) To filter the signal.

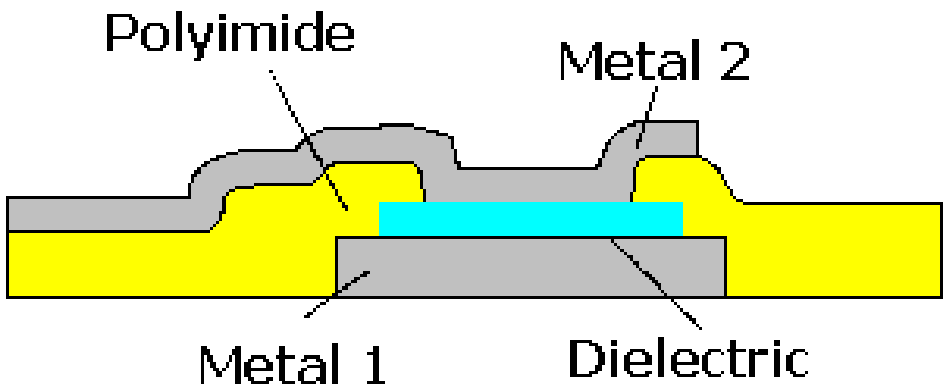
Capacitors in MMIC

- Capacitor may be formed in two ways:
  a) Interdigitated capacitor
  b) Overlay capacitor
- *Interdigitated capacitor* can be formed on a single layer metal but typ have capacitance (< 1.0pF).
- The value of capacitance is determined by the lithographically defined spacing $\rightarrow$ hence dimension difficult to control.



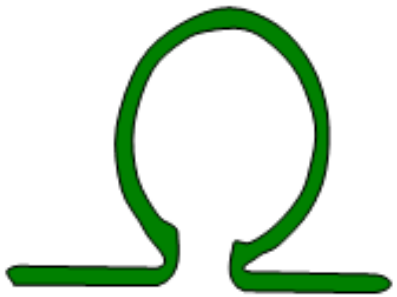
Capacitors in MMIC

- Overlay capacitor → used when *large area* or more *precisely controlled* capacitance is required.
- The common dielectric material for overlay capacitor is silicon nitride Si_3N_4.
- Silicon dioxide SiO_2, Al_2O_3 and polyimide have also been used.

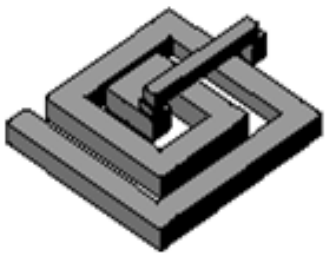


Inductors in MMIC

- Three methods for making inductors in MMICs.
  a) Straight line inductors
  b) Single loop Ω inductors
  c) Spiral inductors
- Metal thickness in all three types is typ → several microns → to reduce resistivity and minimize skin loss.



Loop inductor

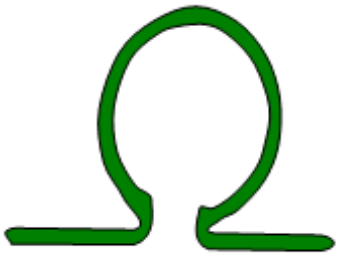


Typical spiral inductor

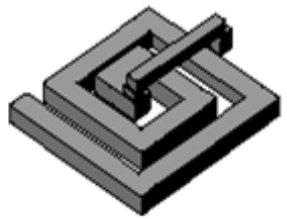
High impedance transmission line inductor

Inductors in MMIC

- ***Straight line inductor*** $\rightarrow$ used for highest frequencies but typ have low inductance ($< 1.0nH$)
- ***Single loop Ω inductors*** $\rightarrow$ easy to form but limited to a few nH.
- ***Spiral inductor*** can be made for L $> 50nH$ but requires two levels of metal with underpass.
- This underpass represents an unwanted capacitance $\rightarrow$ that must be minimized.



Loop inductor

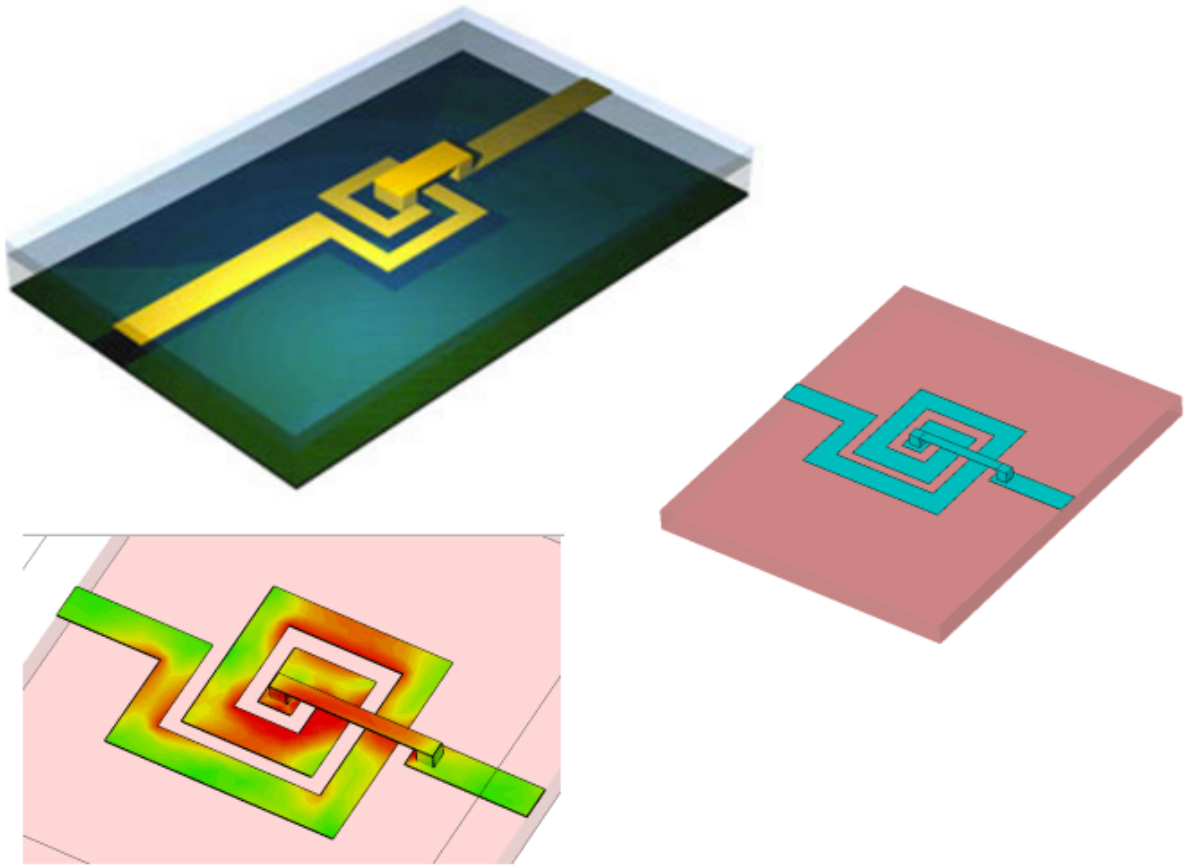


Typical spiral inductor

High impedance transmission line inductor

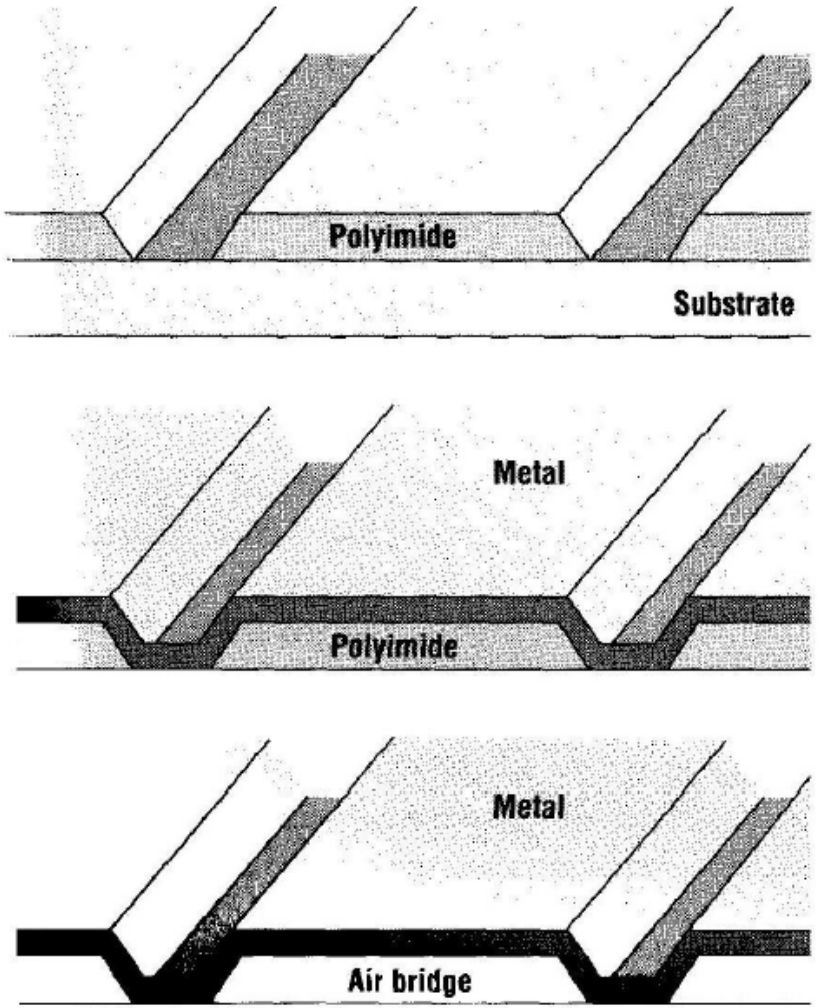
Air Bridge process

- Air bridge process is often used in forming *spiral inductors* in MMIC technology.
- It is typically used to minimize parasitic capacitance.

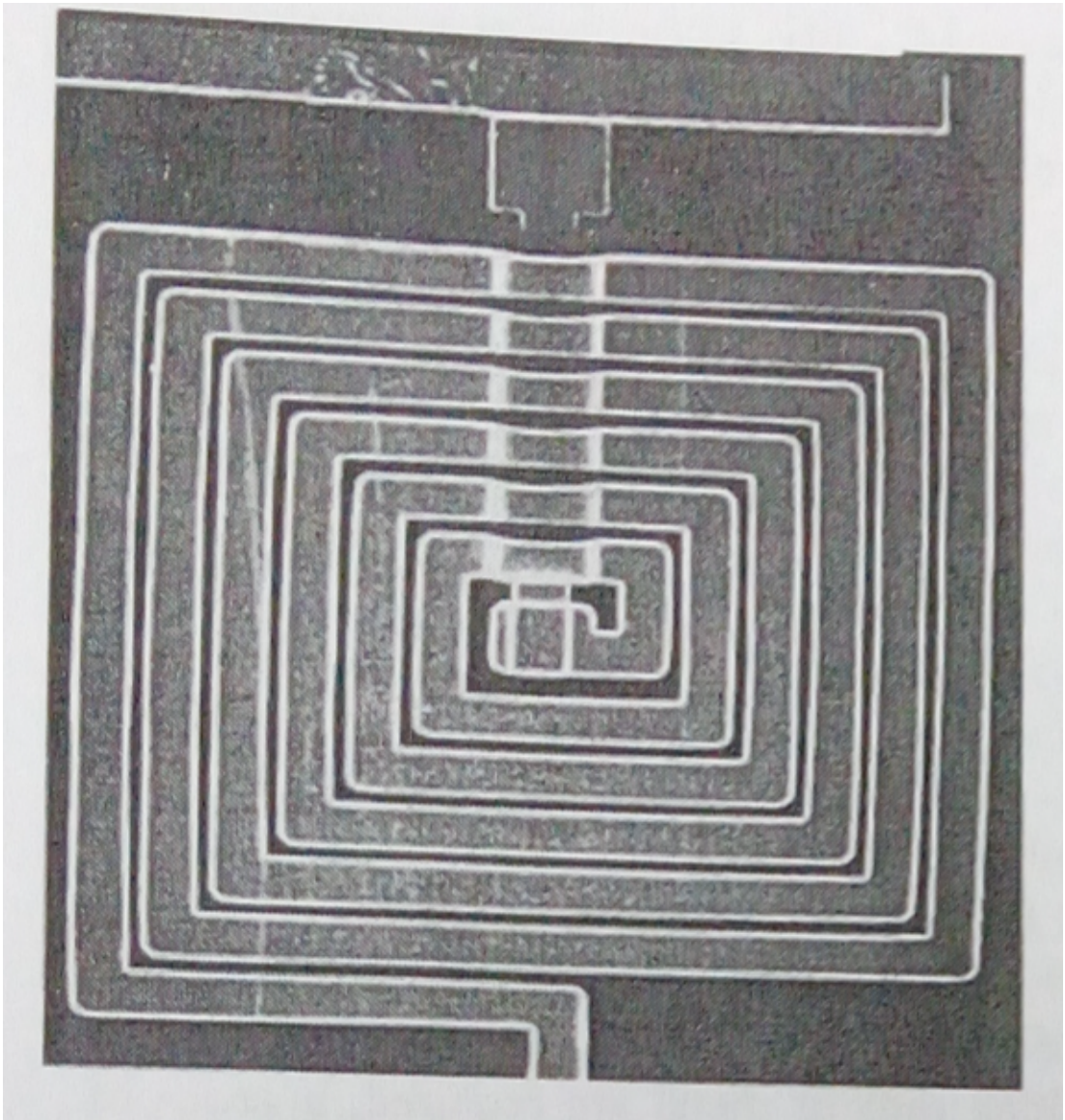


Air Bridge process

- The thick polyimide is patterned on the substrate until exposed substrate.
- Metal deposition is made sufficiently thick to ensure lifting after dissolving the polyimide.
- Air bridges → lowest possible dielectric, rugged and reliable.
- Gold air bridges can be used for small MMIC's because of gold's low resistivity.



Spiral Inductor using Air Bridge

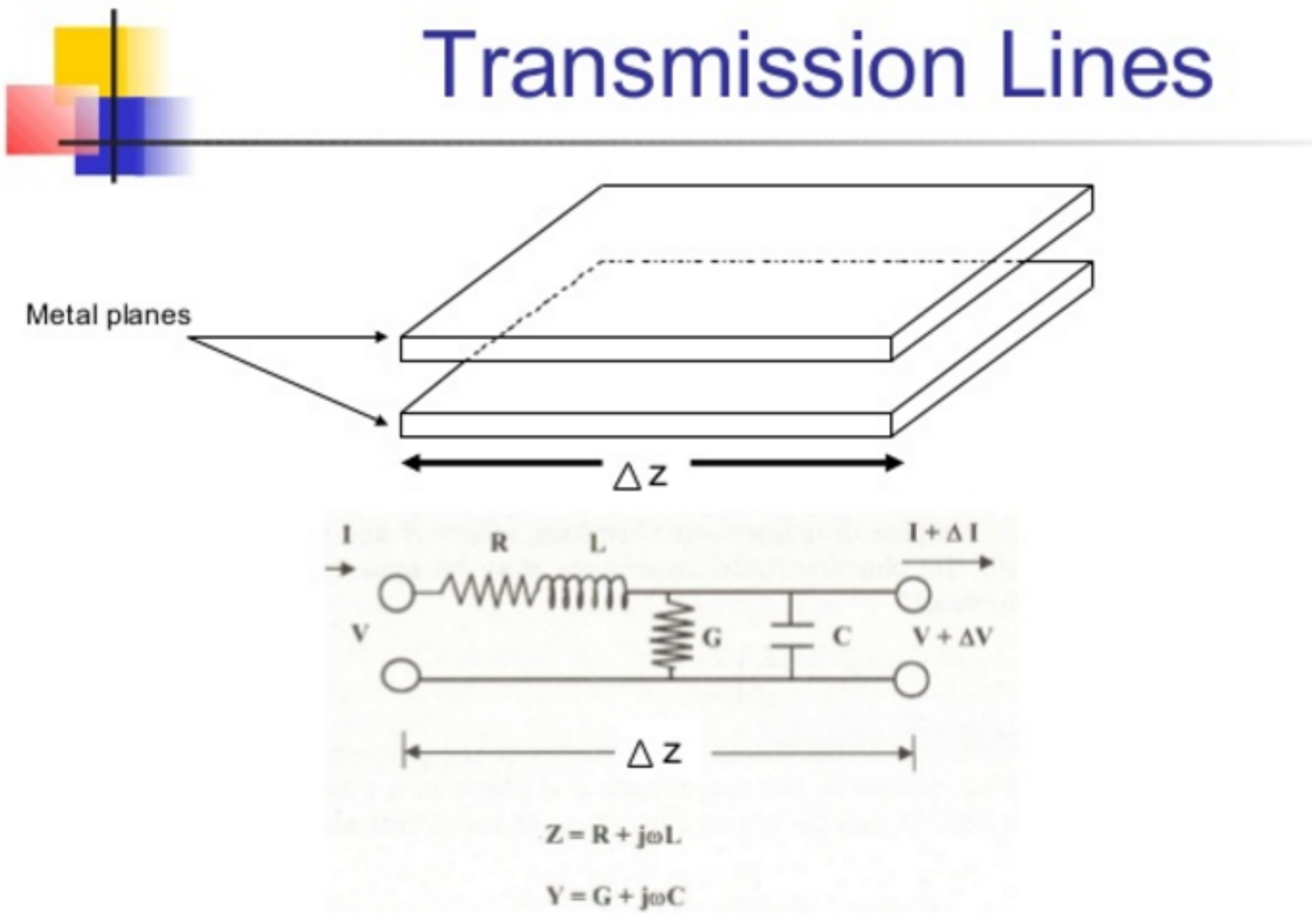


Interconnects in MMIC

What Are RF and Microwaves?

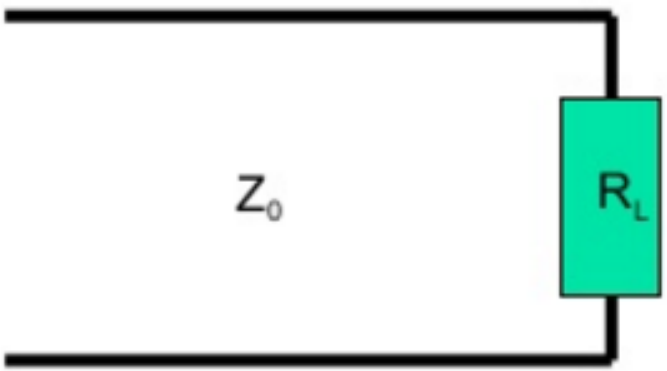
- They are analog signals or AC signals.
- Digital signals are 0's and 1's.
  0 – 0 volt, 1 – 2 volts.
- Wavelengths between 0.1 to 30cm.
- Cell phones are hand held radios. They receive and transmit radio signals.
- Radio waves are electro-magnetic waves.
- An radio antennae is an inductor.

Interconnects in MMIC



Interconnects in MMIC

Impedance Matching



$$\rho \triangleq \frac{V_-}{V_+} = \frac{R_L - Z_0}{R_L + Z_0}$$

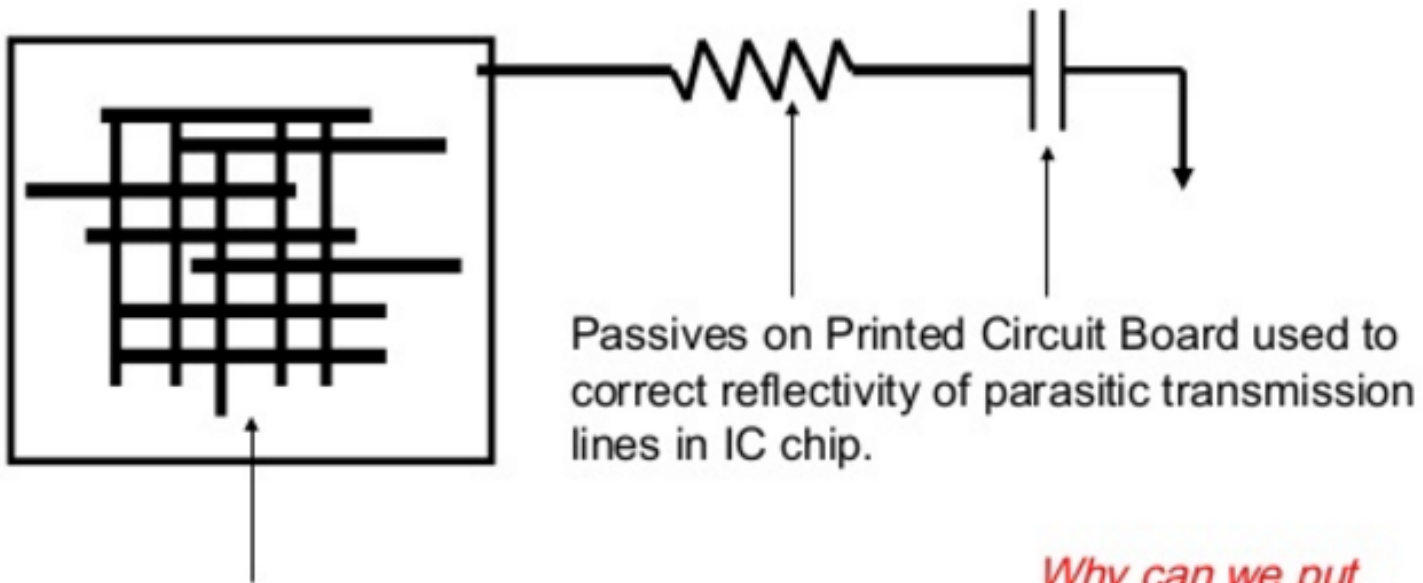
$$\tau \triangleq \frac{V_L}{V_+} = \frac{2R_L}{R_L + Z_0}$$

ρ : **Reflectivity**

τ :**Transmission**

Interconnects in MMIC

IC Chip – Parasitic Transmission Lines

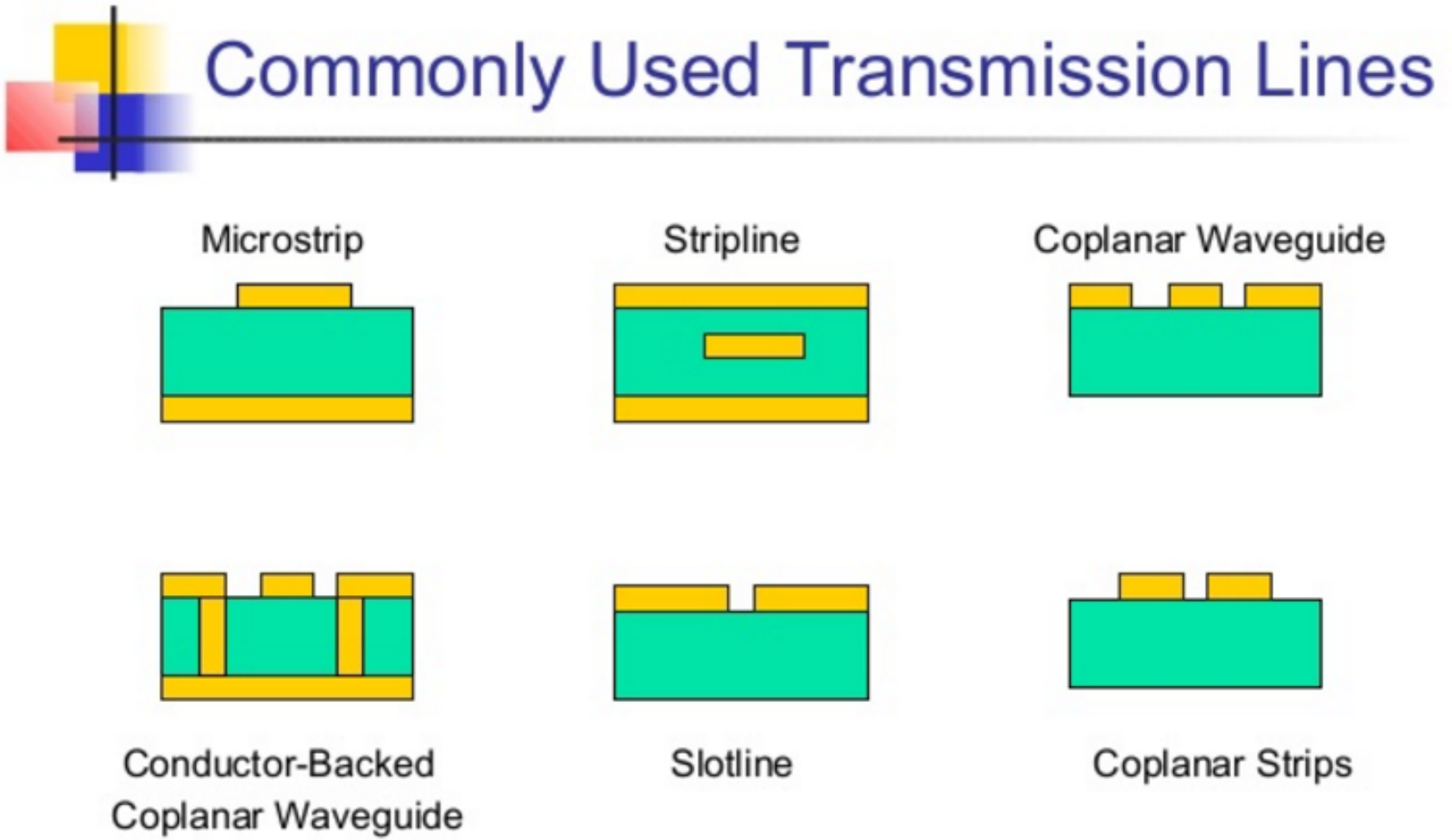


Passives on Printed Circuit Board used to correct reflectivity of parasitic transmission lines in IC chip.

Ex. IC Chip with 4.5 km of metal lines in Pentium.
Metal lines form parasitic transmission lines

Why can we put the passives in the IC Chip?

Interconnects in MMIC

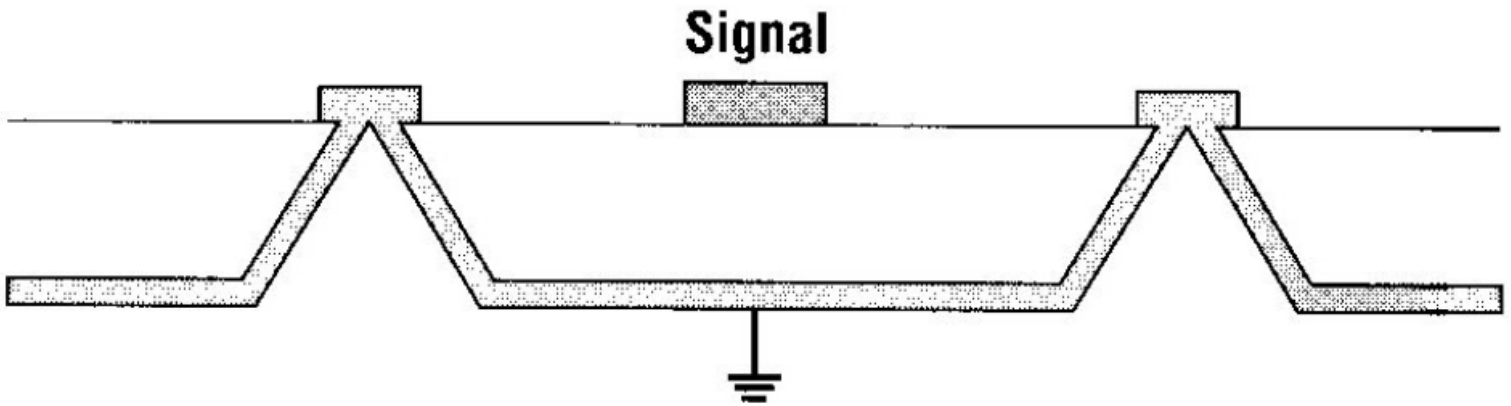


Interconnects in MMIC

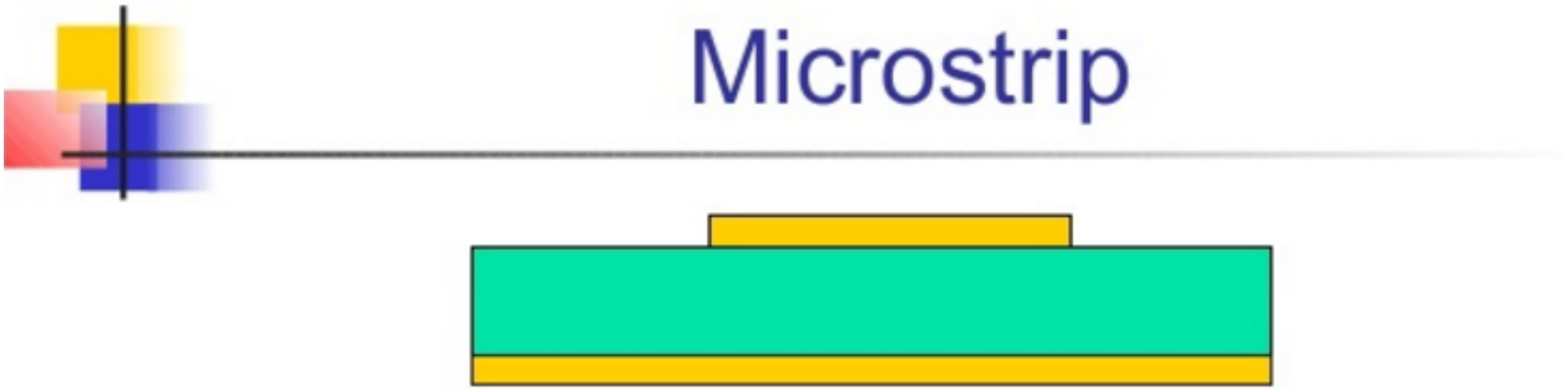
- At high frequency → *Metal interconnect or waveguide* must have a controlled, reproducible impedance.
- Line must be well shielded from each other to avoid cross-talk.
- Line loss must be minimized and finally a stable ground voltage is needed.
- Two choices for fabricating these interconnects:
  a) Coplanar interconnect
  b) Microstrip interconnect

Microstrip Interconnect

- It uses the back of the wafer as ground plane.
- Usually the wafer is thinned from $500\mu m$ to $100\mu m$.
- This is done by lapping in abrasive materials such as alumina and silicon carbide.
- It is then polished using wet chemical.
- The through hole is then patterned and etched with the infrared aligner to make sure front side and backside is aligned.
- The deposition of gold is made with the aid of infrad red IR camera to ensure the microstrip is deposited.



Microstrip Interconnect

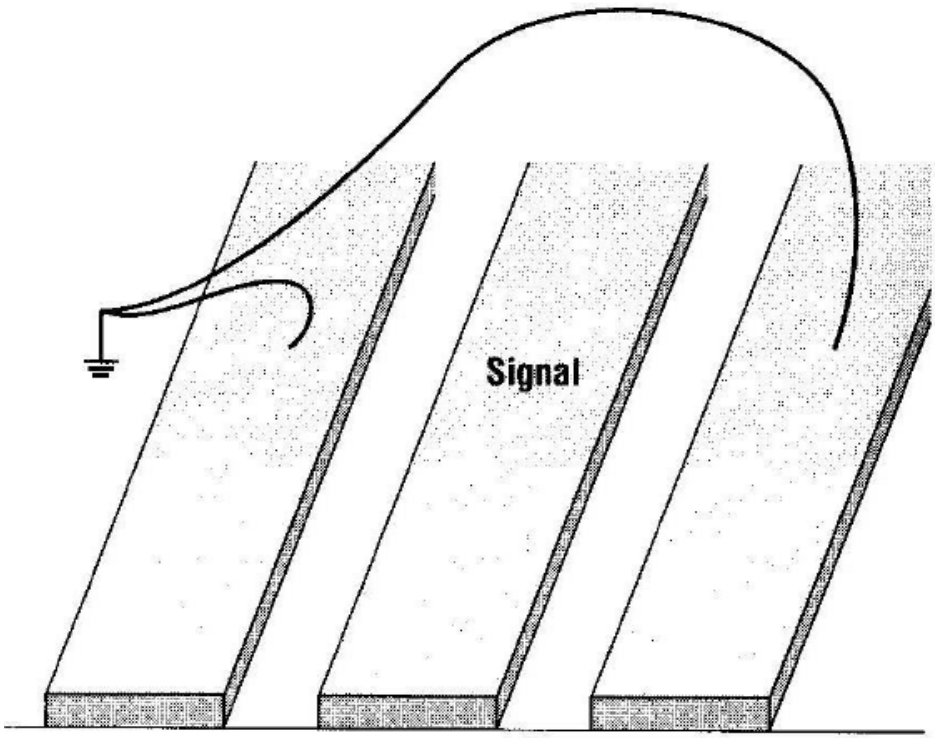


Advantage - Most widely used. Excellent integration with chip and lumped elements. Multilayers are possible. Ground plane isolate the microstrip.

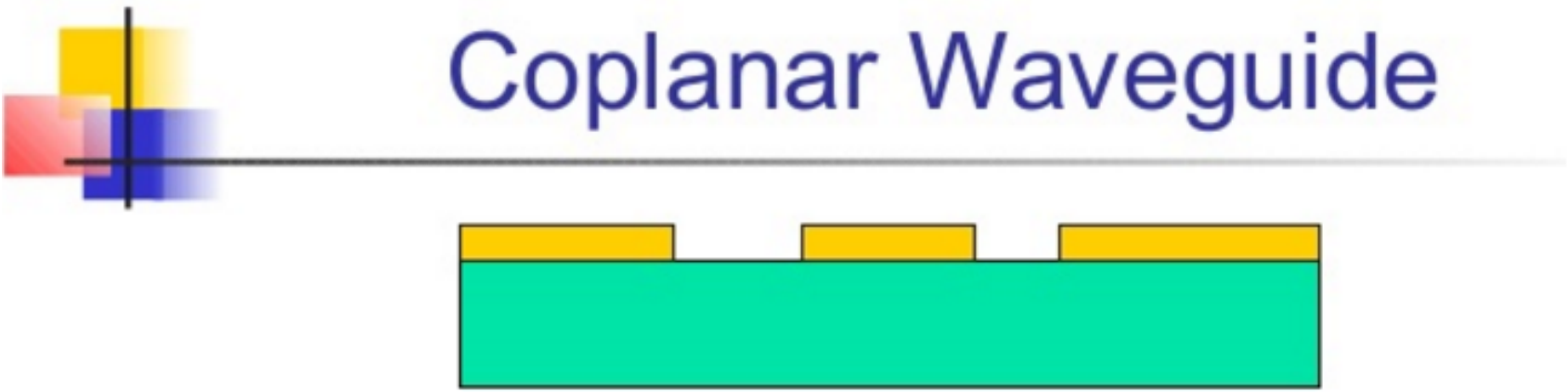
Disadvantage - Line losses are somewhat higher with poorer isolation between circuits. It is unshielded and some radiation occurs for thicker substrates depending on dielectric constant and frequency.

Coplanar Interconnect

- Coplanar waveguide terminates the field lines associated with waveguide with parallel ground lines.
- The line must wide and closed to signal line.
- For low-density MMICs, they may be wire bounded directly to a large ground plane surrounding the chip.



Coplanar Interconnect



Very good integration with chip and lumped elements. Series and shunt connections are relatively easy.

Disadvantage – thick substrates are required to keep structure away from the chasis. Integration with multilayers is poor.