02/10/15

GaAs MESFET Characteristics & Operation

01

- Up to now, in ED course we have been discussing Si based devices (Bipolar based as well MOS based)

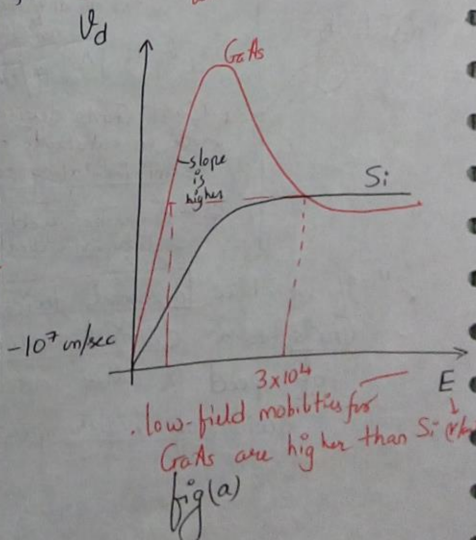
· Property	GaAs	Si
1) Bandgap	1.42eV direct ↳ CB minima & VB maxima are both at the same momentum, so one can use it for opto-electronic devices	1.1 eV indirect ↳ cannot be used for opto-electronic devices
2) Low-field mobility of electrons	5000 cm^2/V-sec for $N_d = 10^{17}/cm^3$ 8000 cm^2/V-sec for undoped GaAs ↳ Now, we have device like HEMT using GaAs, where the $\bar{e}$'s actually flow in the undoped part of GaAs giving rise to such high mobilities.	800 cm^2/V-sec for $N_d = 10^{17}/cm^3$
3) Saturat^n velocity 'v_d'	~10^7 cm/sec v_d ← achieved at lower E-field → means lower vtgs applied across device ⇒ means devices can be operated at lower vtgs ⇒ means u require less power	~10^7 cm/sec

higher bandgap means it can be used at higher temp^r
· Adv: GaAs

disadv: ↓ difficult to make ohmic contacts (can be overcomed thr improved technology)

Nowadays, a lot of opto-electronics IC's are been fabricated, where u have both the IC/slg processing ckty as well as the sensor (optical) in the same chip. → For that purpose, GaAs will obviously be advantageous.

Adv: ↓ utilised to make very Fast logic ckt.



· low-field mobilities for GaAs are higher than Si (v_d)

fig(a)

→ In Si MOSFET device, the ēs only close to 'D' end may be travelling at saturatn velocity.

→ In GaAS FET, the carriers in major portⁿ of the channel will be travelling at saturatn velocity in GaAs devices.

Properties	GaAs	Si
4) Peak velocity	- 2×10^7 cm/sec ↳ can also be utilized if used properly to make high speed devices	—
5) Low-field hole mobility	$250\ cm^2/V\text{-}sec$ "Poor" for $N_d = 10^{17}/cm^3$ Disadv: GaAs cannot be used to make complimentary ckt devices like CMOS in Si	$\sim 300\ cm^2/V\text{-}sec$ for $N_d = 10^{17}/cm^3$
6) Substrate Resistivity	→ GaAs device can be made on undoped GaAs sample. ↳ Not only that, resistivity of sample can be high. 10^6 to 10^8 Ω/cm → Most GaAs devices are made on substrate called "semi-insulating" substrates. Adv: It can be used to isolate individual devices, not only that, since they are made on high 'R' substrate's, the parasitic capacitance from the device to the substrate is v.v.low.	Low

↳ bcoz of this reducted in parasitic capacitance's, the device "can be operated at higher frequencies"

• "If we have n-channel device, where carriers are electron's GaAs has a distinct advantage over Si in terms of speed & this can be utilised to realize devices of higher speed.

Properties	GaAs	Si
7) Surface States densities ⇓ They are the unsaturated "dangling bonds" on the surface of the material. and becoz of that what u have is → When u make a device, these gives rise to some "surface charges"! These "surface charges" play a role in device operatn.	~ 10^{12} /(cm^2 eV) Disadv: · Effect of surface states is that in GaAs, → 1) It is difficult to make ohmic ~~contacts~~ contacts (becoz they result in "Fermi-level pinning" ie fermi-level is pinned at one particular level at the surface when u make a metal contact. (But can make ohmic contact's on a highly doped GaAs substrate) eg Gate ohmic contact. 2) Becoz of this "Fermi-level pinning", one cannot really have "inversion layers" in GaAs substrate, like u have in a MOSFET (Si devices), so it is much difficult to make a MOSFET on GaAs, becoz it v.difficult to "invert" the surface. So, u cannot have this Enhancement type MOSFET devices in GaAs, as you have in Si.	~ 10^{10} /(cm^2 eV) So, becoz of these two problems (ie large no of surface states & native oxide problem), we cannot have "MOSFET" type of devices in GaAs.
8) Native oxide	→ Unstable Disadv:	Stable (thermally grown oxides used in Si devices) eg MOSFET → oxide in Si devices

→ In a MOSFET, we require an "oxide" structure, require a "native oxide". Now GaAs Native oxide is very unstable → It cannot be used for any pratical devices

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- Since, MOSFET cannot be made in GaAs, →
  → So, devices which is used in GaAs for integrated ckts (IC) is the "MESFET" & not the MOSFET.
  typedevices
  → It's a "Field-effect transister"!

- In MESFET, but we do not have a "MOS" structure, as in a MOSF, but we have a "metal-semiconducter junction"

Now, let's discuss this particular device "MESFET" we look at the different properties of this device and then we shall see how this device's can be used to make integrated ckt.

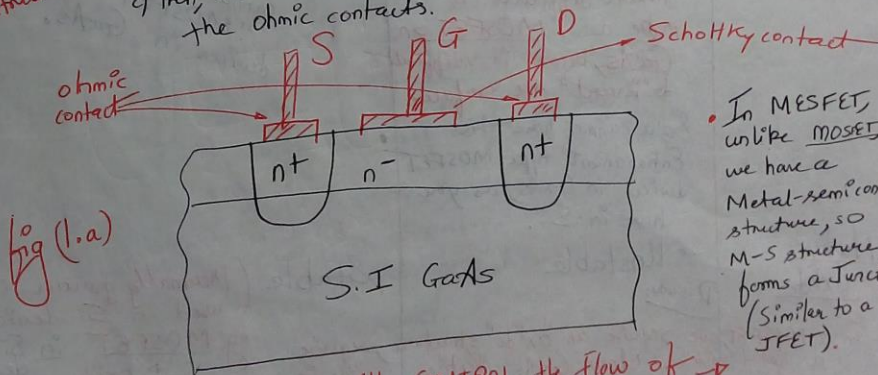
- MESFET ~~~~ made use of GaAs

  Let see how a MESFET actually looks like.

  Let see how a MESFET can be made.

→ Two ways in which a MESFET can be made.

1st case: (1st structure)
a) We start with semi-insulating GaAs is made (Lightly doped n^-) implant
b) Then, shallow 'n' type implants (n^+) → This is to make
c) Then, we make heavy dope implants the ohmic contacts.



- In MESFET, unlike MOSFET, we have a Metal-semiconductor structure, so M-S structure forms a Junction. (Similar to a JFET).

→ This M-S J^n which will CONTROL the flow of → current (carriers e^-s) from the 'S' to the 'D'

2nd Structure: MESFET: → made on epitaxial wafer (here we do not have to carry out the implantations) 05

Structure

1. Start with S.I. GaAs
2. On which a lightly doped n GaAs is made
3. On top, which we have heavily doped 'n' GaAs
4. Now recess etching is done, on the surface to make 'S' & 'D'.

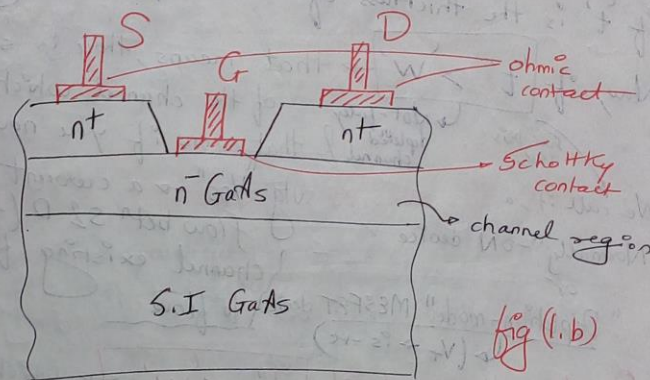


fig (1.b)

. Now let us see how the device (MESFET) operates.

→ "MESFET operation:-

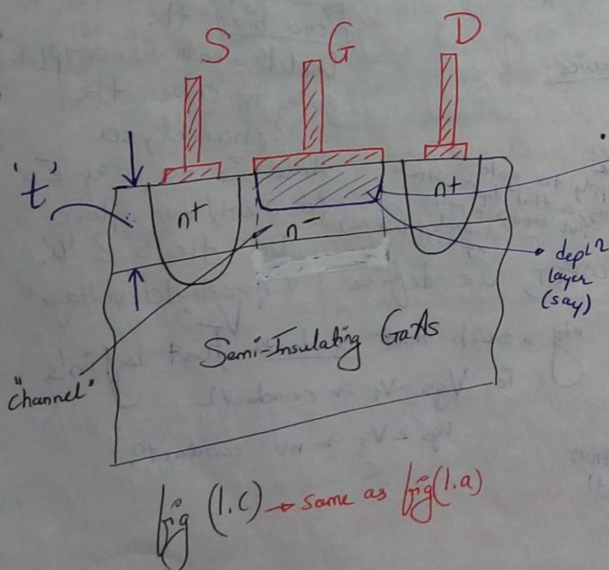


fig (1.c) → same as fig (1.a)

. Now this M-S J^n behaves almost like a ($p-n$ J^n) or (a p^+-n J^n), so there will be a "built-in" potential "V_{bi}". and becoz of this builtin potential → there is going to a depletn layer (here)

. Now, say width of depl^n layer is 'W'.

→ Now, W can be related to V_{bi} (by solving poisson's eq^n):

So, $$V_{bi} = \frac{qNW^2}{2\epsilon}$$

or

$$W = \sqrt{\frac{2\epsilon_s V_{bi}}{qN}}$$

where, N is the doping conc^n
ϵ → permittivity

Refer (1.C) figure (For this page's explanatⁿ)

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• If 't' is the thickness of (n^-) layer in fig (1.C)

→ Now, if 't' > 'W' → that means, there is still a part of the channel which is "undepleted" & that means if you now apply vtg "V_{DS}" → a current (e⁻s) can flow betⁿ S & D (there is a channel existing for current to flow.

↳ Not-fully depleted channel

For this case, We call it a "Normally"-ON device or "Depletion-mode" MESFET device

↳ (V_T → is -ve)

→ On the other hand, if 't' < 'W'. → which means, that deplⁿ width 'W' due to built-in potential is much larger than the thickness 't' of the channel, then at Zero bias, the Depletⁿ width is completely going to cover the channel, so there is no way e⁻s (current) can flow betⁿ the 'S' & 'D'.

We this case We call it a "Normally"-off device or "Enhancement-mode" device

↓

(V_T is +ve)

↓

"Forward bias gate vtg" (apply the gate vtg, so that deplⁿ width is just enough to cover channel region (thickness))

→ For these device, like MOSFET, we define "Threshold voltage" "V_T" such that conductⁿ just begin's

V_T → is that V_{gs} vtg

↓

gate to-source at which deplⁿ width just cover the channel region of thickness (t)

ie $V_{gs} > V_T$ → conductⁿ

$V_{gs} < V_T$ → no conductⁿ

- Related to MESFET, we also define "Pinch-off vtg" "V_{po}"

V_{po} → which is the vtg across the depl^n region just sufficient to cover the thickness of the channel region 't'.

$$V_{po} = \frac{qNt^2}{2\epsilon}$$

Now, Threshold vtg (V_t) of this device is given by,

$$V_T = V_{bi} - V_{po}$$

→ ie extra-vtg ie reqd to pinch-off the whole channel.

- For enhancement type device (MESFET), "t < W" → the doping conc^n 'N' shld be small

$$W = \sqrt{\frac{2\epsilon_{Si} V_{bi}}{qN}}$$

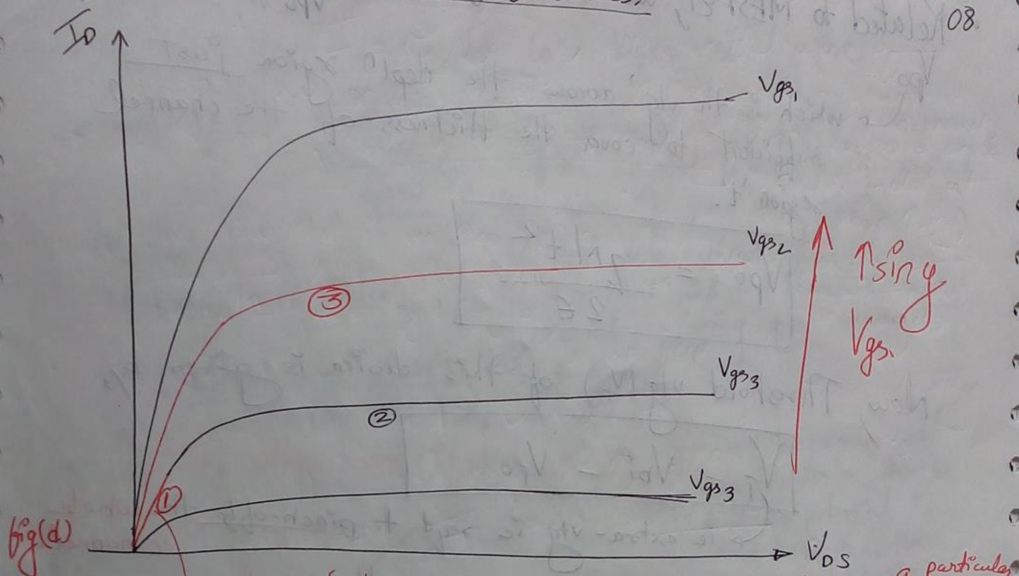
→ For same V_{bi}, if 'N' is same, 'W' will be large

(So, either we can make t small or 'W' large by making 'N' small).

- To We want to make a depl^n-mode MESFET, we have 't' large or 'N' large
  ↳ doping conc^n.

→ Normally, it is easier to fabricate deplet^n mode devices than enhancement-mode device (becoz u require much greater control in making E-mode MESFETs in fabricat^n process)

• MESFET's I-V characteristics:-



→ Suppose, we have a 'D'-mode device, where V_T is -ve and at ~~zero bias~~ a particular bias the channel already (↳ depln) exist, (Refer fig(1.c)).

so current can flow,

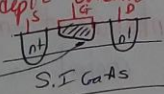
Now, if we apply V_{DS}, I can flow thr the channel.

$$I = Aqnv \quad (\to \text{velocity}) \quad = AqNv$$

↳ concn of carrier ≈ N → doping concn

So, this basically behaves like a "resistance", & we apply a D-S vtg V_{DS}, at a particular V_{gs} → then as we ↑se V_{DS}, I_D is going to rise linearly. initially.

• But as we are ↑sing V_{DS}, the 'D'-end vtg is ↑sing → which means (it will R.B M-S jn, so the depln width of channel is going to keep widening at the D-end.



• Now, since there widening of Depl^n width at 'D' end → it means that $I = AqNv$, cross-sect^al area of current flow reduces. ⇒ (If we must have a constant current flowing thro' the channel) 09

→ If A reduces, velocity 'v' then has to keep ↑sing (This happen's becoz Electric-field at 'D' end keeps ↑sing)

• But, we know that if we keep on → ↑sing the velocity (v) it will reach → saturat^n (Refer pg 1, fig (a)) Note: (E-field is not constant thro'out the channel)

• So, what happens is initially as we keep on ↑sing V_{DS}, becoz of the reduct^n in 'A', current I_D does not rise linearly (but sub-linearly) & finally when velocity of (e's) 'v_d' reaches saturat^n → current 'I_D' also saturates (Part ② in fig d) (but slightly ↑se) → (similar to CLM in MOSFET) (since, here in MESFET also effective channel length reduces)

→ Now, if we take a higher gate vtg, (+ve V_{gs}) current 'I_D' is going to ↑se more becoz (part ③) (for a higher V_{gs} vtg, the depl^n width in the channel is going to be less, ⇒ the initial cross-sect^n of 'A' of current flow is going to be more)

→ Refer fig (d), the Nature of I-V charact^r of MESFET is valid for both Enhancement & depl^n-mode devices. → Quite similar to that of MOSFET

{ eg if we have a D-mode MESFET, it means that the current flow I_D will exist if even when $V_{gs} < 0$. }