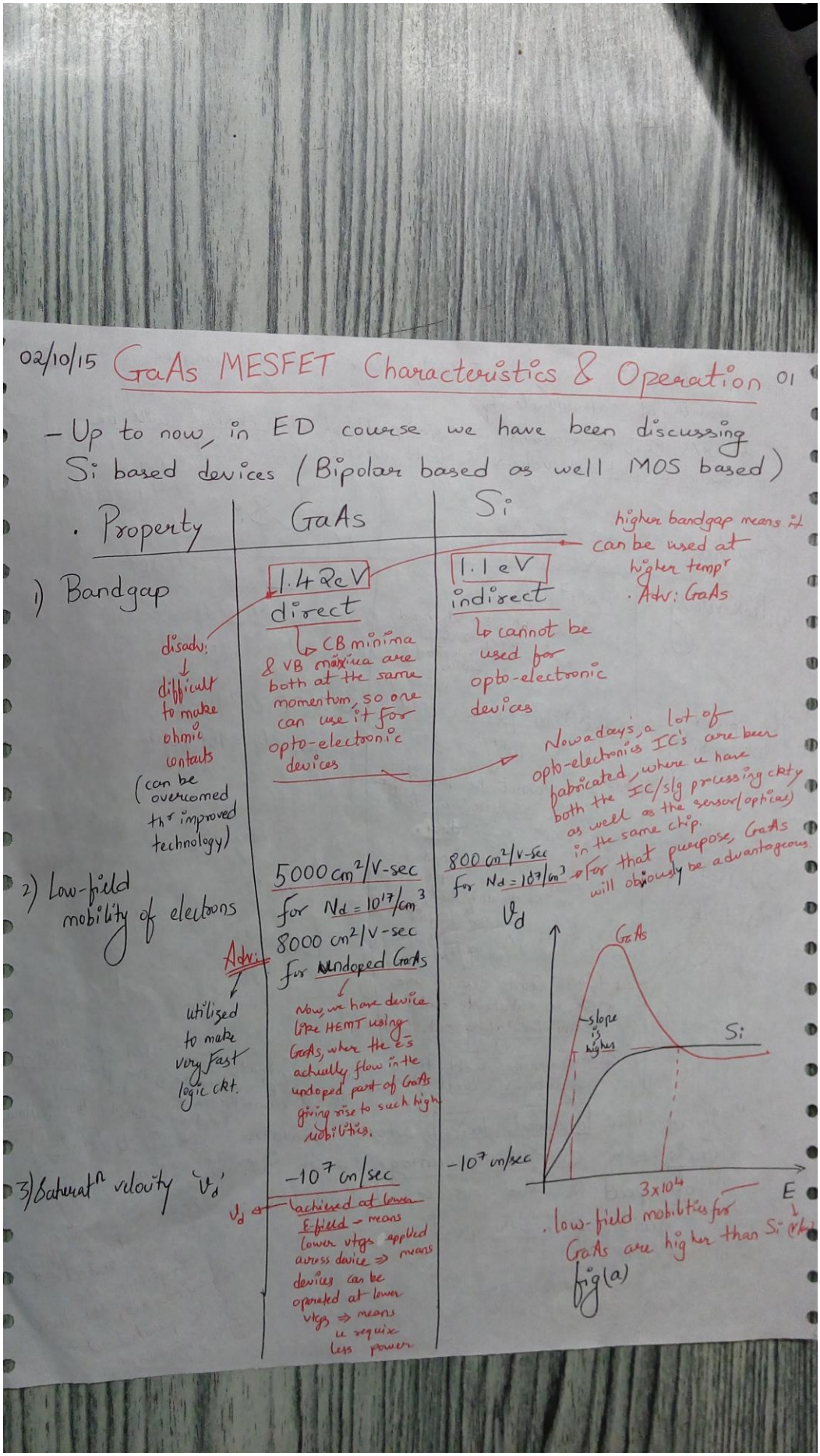
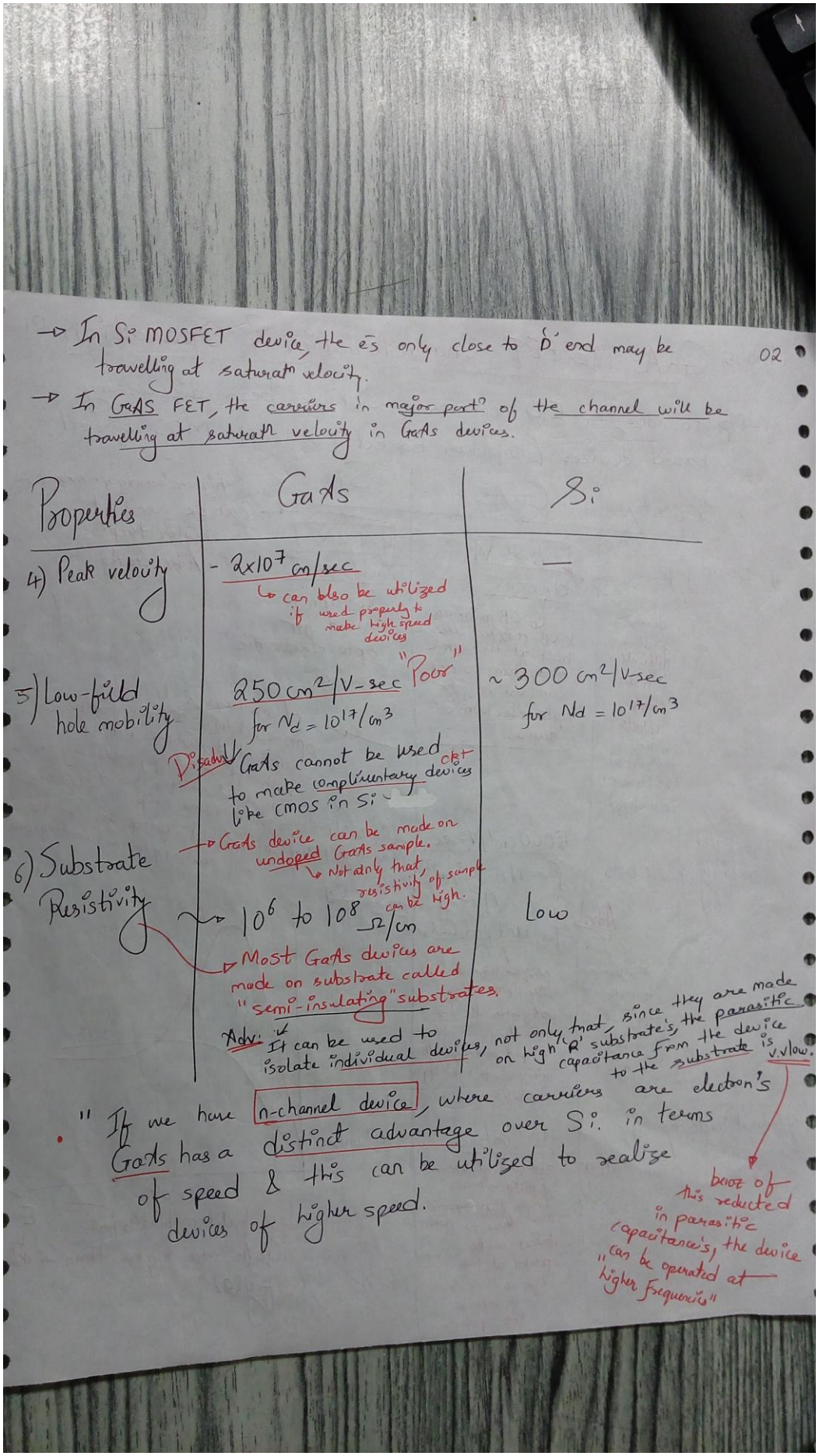

02/10/15 GaAs MESFET Characteristics & Operation 01
- Up to now, in ED course we have been discussing Si based devices (Bipolar based as well MOS based)
Property
GaAs
Si
1) Bandgap
1.42eV direct
CB minima & VB maxima are both at the same momentum, so one can use it for opto-electronic devices
1.1eV indirect
cannot be used for opto-electronic devices
higher bandgap means it can be used at higher temp. Adv: GaAs
disadv: difficult to make ohmic contacts (can be overcomed thr improved technology)
Nowadays, a lot of opto-electronics IC's are been fabricated, where u have both the IC/s/g processing ckts as well as the sensor/optics in the same chip. For that purpose, GaAs will obviously be advantageous.
2) Low-field mobility of electrons
5000 cm²/V-sec for Nd = 10¹⁷/cm³
8000 cm²/V-sec for Undoped GaAs
800 cm²/V-sec for Nd = 10¹⁷/cm³
Adv: utilized to make very fast logic ckt.
Now we have device like HEMT using GaAs, where the e⁻s actually flow in the undoped part of GaAs giving rise to such high mobilities.
3) Saturatn velocity 'Vd'
~10⁷ cm/sec achieved at lower E-field - means lower vtgs applied across device ⇒ means devices can be operated at lower vtgs ⇒ means u require less power
Vd
GaAs
Si
slope is higher
~10⁷ cm/sec
3x10⁴
E
. low-field mobilities for GaAs are higher than Si
fig(a)



→ In Si MOSFET device, the $\bar{e}$s only close to 'D' end may be travelling at saturatn velocity. 02

→ In GaAs FET, the carriers in major part of the channel will be travelling at saturatn velocity in GaAs devices.

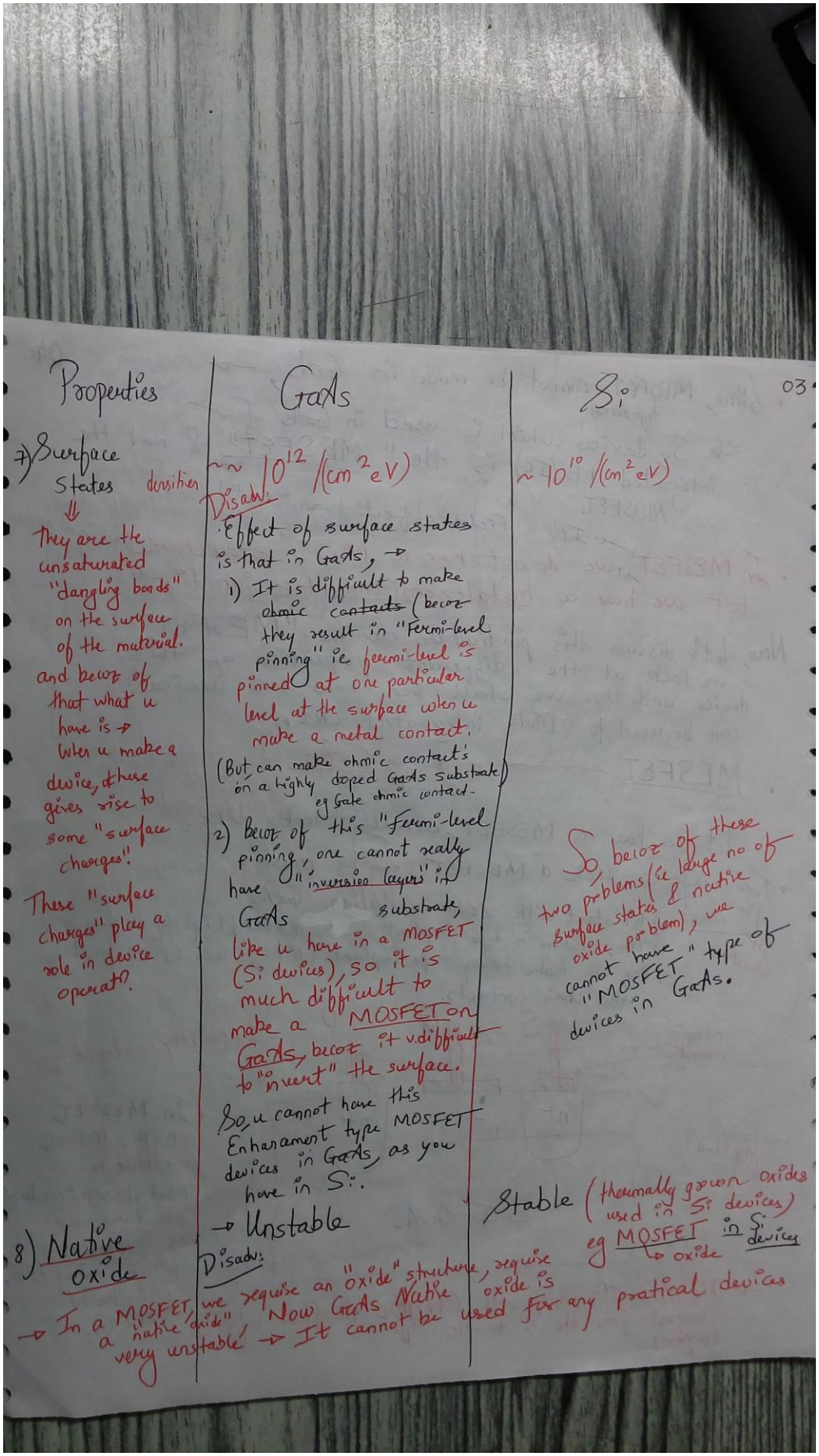
Properties	GaAs	Si
4) Peak velocity	2×10^7 cm/sec ↳ can also be utilized if used properly to make high speed devices	—
5) Low-field hole mobility	250 $cm^2/V\text{-}sec$ "Poor" for $N_d = 10^{17}/cm^3$	~ 300 $cm^2/V\text{-}sec$ for $N_d = 10^{17}/cm^3$
6) Substrate Resistivity	→ GaAs device can be made on undoped GaAs sample. ↳ Not only that, resistivity of sample can be high. ~ 10^6 to 10^8 Ω/cm → Most GaAs devices are made on substrate called "semi-insulating" substrates.	Low

Disadv: GaAs cannot be used to make complimentary ckt devices like CMOS in Si.

Adv: It can be used to isolate individual devices, not only that, since they are made on high 'R' substrate's, the parasitic capacitance from the device to the substrate is v.low.

" If we have n-channel device, where carriers are electron's GaAs has a distinct advantage over Si. in terms of speed & this can be utilized to realise devices of higher speed.

Benefit of this reduced in parasitic capacitance's, the device can be operated at higher frequencies"



Properties | GaAs | Si | 03

7) Surface States density

They are the unsaturated "dangling bonds" on the surface of the material. and becoz of that what u have is → When u make a device, these gives rise to some "surface charges".

These "surface charges" play a role in device operation.

~ 10^{12} /(cm² eV)

~ 10^{10} /(cm² eV)

Disadv:

- Effect of surface states is that in GaAs, →
  1) It is difficult to make ohmic contacts (becoz they result in "Fermi-level pinning" ie fermi-level is pinned at one particular level at the surface when u make a metal contact.
  (But can make ohmic contacts on a highly doped GaAs substrate) eg Gate ohmic contact.
  2) Becoz of this "Fermi-level pinning", one cannot really have "inversion layers" in GaAs substrate, like u have in a MOSFET (Si devices), so it is much difficult to make a MOSFET on GaAs, becoz it v.difficult to "invert" the surface.

So, u cannot have this Enhancement type MOSFET devices in GaAs, as you have in Si.

So becoz of these two problems (ie large no of surface states & native oxide problem), we cannot have "MOSFET" type of devices in GaAs.

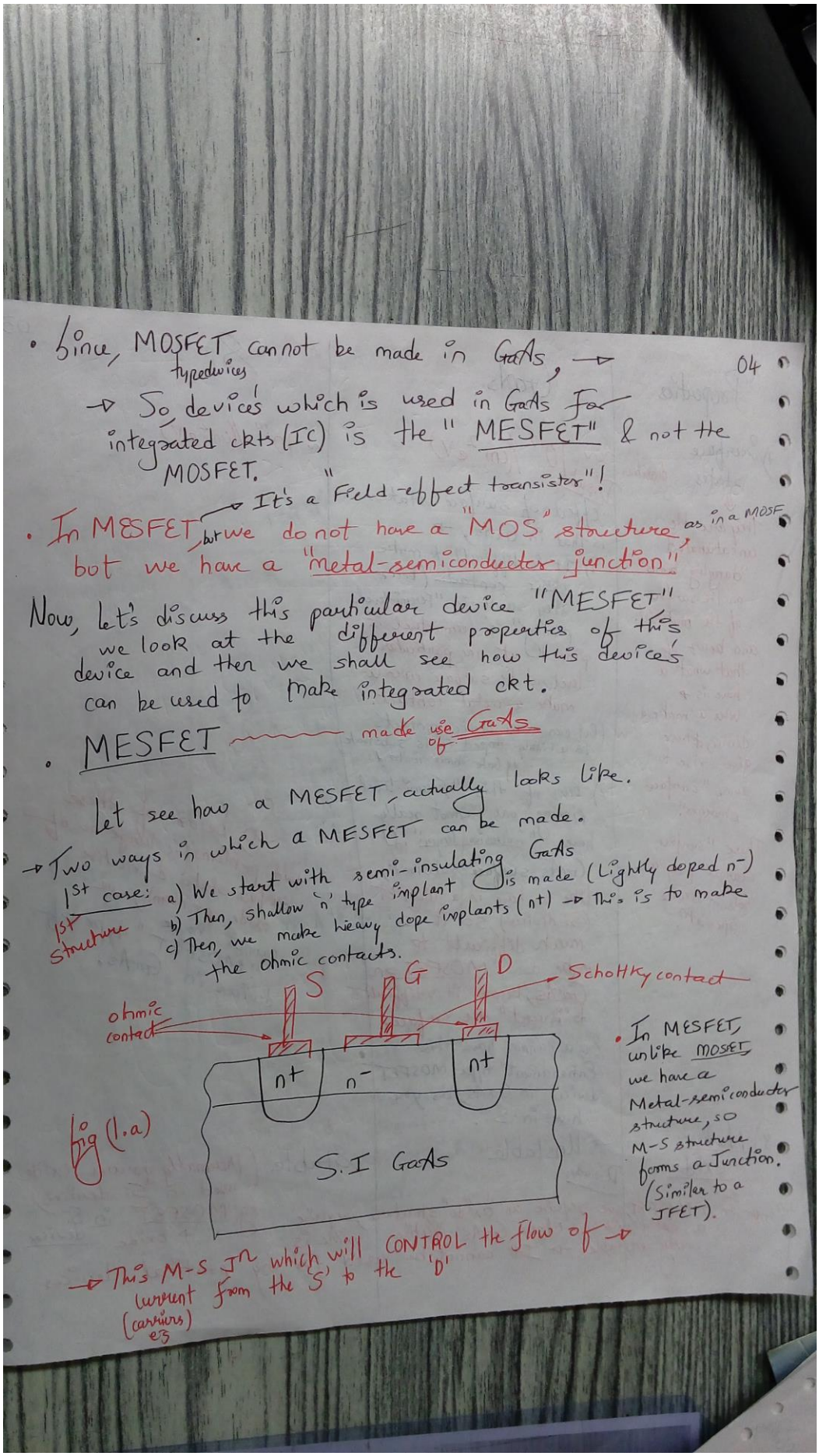
→ Unstable

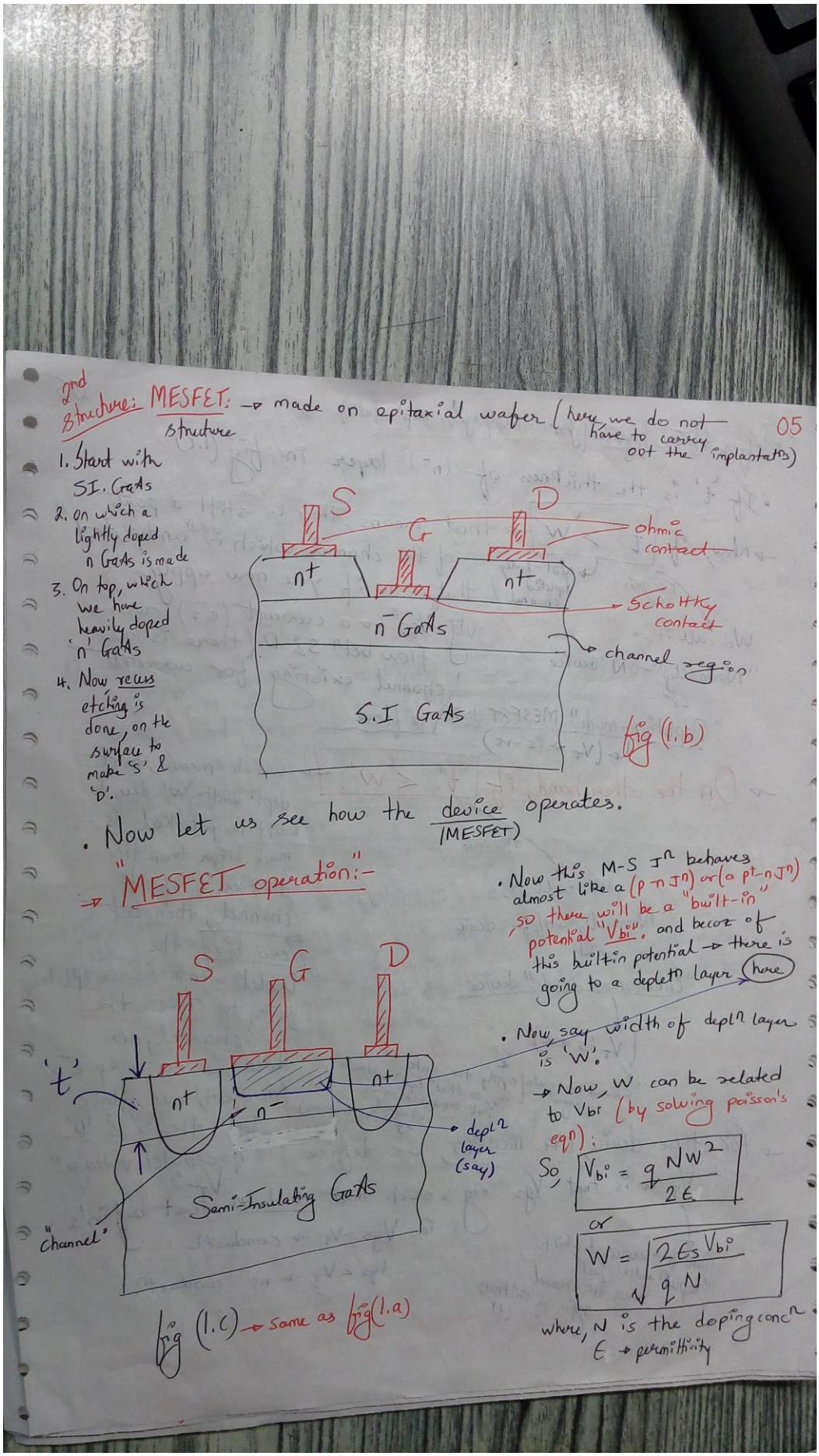
8) Native oxide

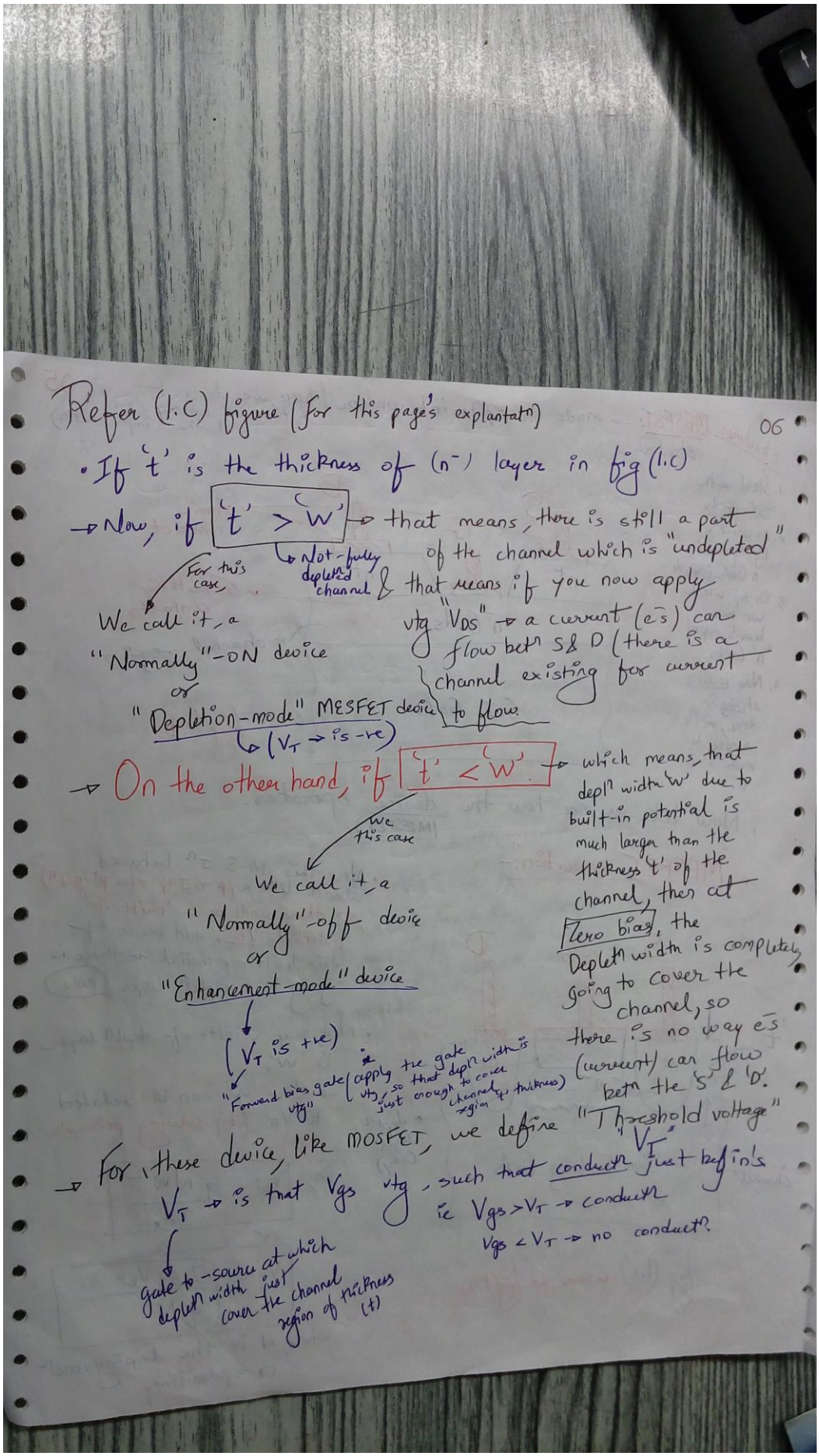
Disadv:

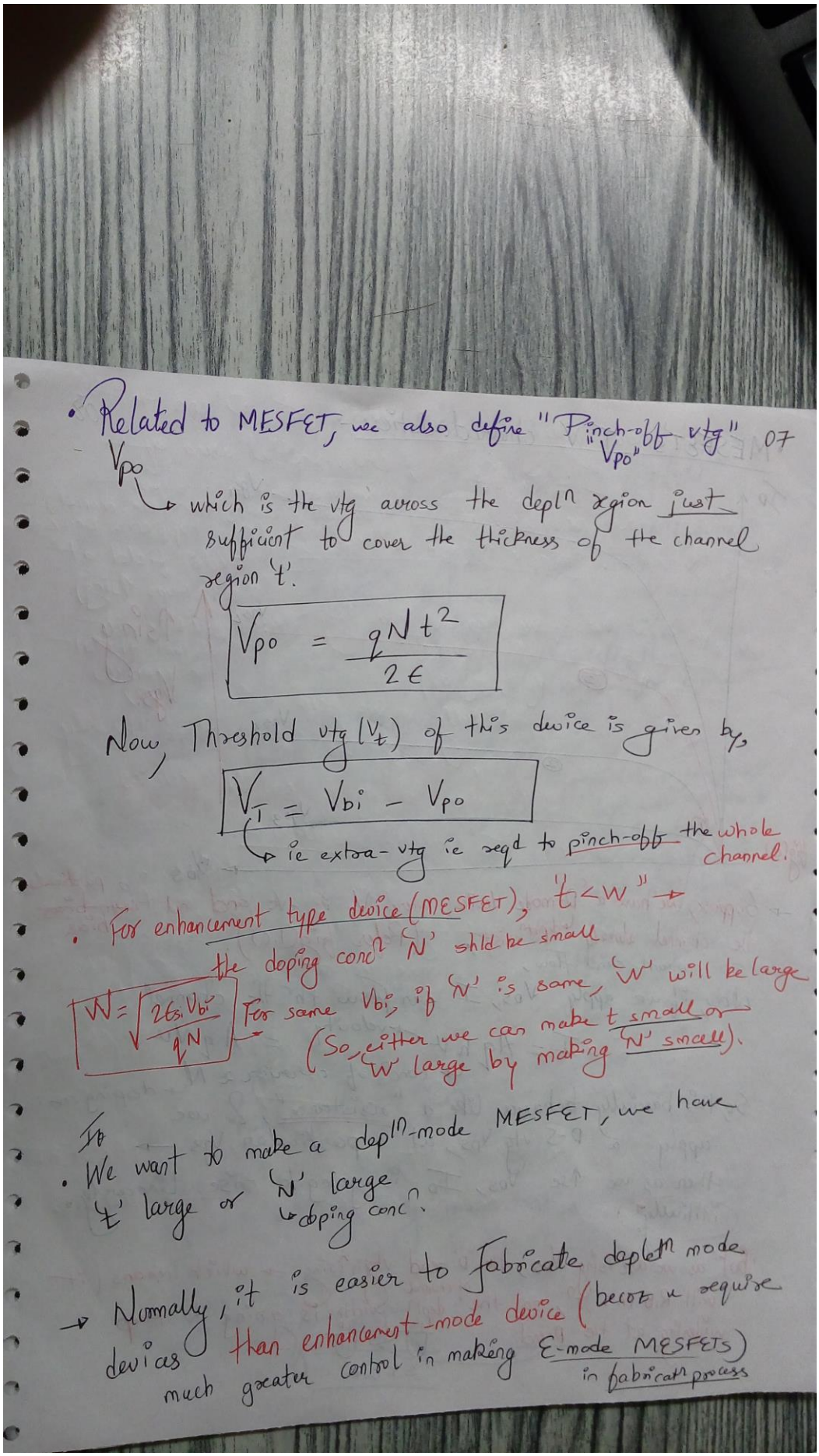
→ In a MOSFET, we require an "oxide" structure, a "native oxide" Now GaAs Native oxide is very unstable → It cannot be used for any pratical devices

Stable (thermally grown oxides used in Si devices) eg MOSFET → oxide in Si devices


• Since, MOSFET cannot be made in GaAs, → 04
typedevices
→ So, devices which is used in GaAs for integrated ckts (IC) is the "MESFET" & not the MOSFET.
It's a "Field-effect transister"!
• In MESFET, but we do not have a "MOS" structure, as in a MOSF
but we have a "metal-semiconductor junction"
Now, let's discuss this particular device "MESFET" we look at the different properties of this device and then we shall see how this devices can be used to make integrated ckt.
• MESFET made use of GaAs
Let see how a MESFET, actually looks like.
→ Two ways in which a MESFET can be made.
1st case: a) We start with semi-insulating GaAs
1st structure b) Then, shallow 'n' type implant is made (Lightly doped n⁻)
c) Then, we make heavy dope implants (n+) → This is to make the ohmic contacts.
S
G
D
Schottky contact
ohmic contact
n+
n⁻
n+
S.I GaAs
fig (1.a)
• In MESFET, unlike MOSFET, we have a Metal-semiconductor structure, so M-S structure forms a Junction. (Similar to a JFET).
→ This M-S JN which will CONTROL the flow of current (carriers e⁻s) from the 'S' to the 'D'


2nd Structure: MESFET:
Structure
→ made on epitaxial wafer (here we do not have to carry out the implantations)
05
1. Start with SI. GaAs
2. on which a lightly doped n GaAs is made
3. On top, which we have heavily doped 'n' GaAs
4. Now recess etching is done, on the surface to make 'S' & 'D'.
S
G
D
ohmic contact
Schottky contact
n+
n+
n⁻ GaAs
channel region
S.I GaAs
fig (1.b)
. Now let us see how the device (MESFET) operates.
→ "MESFET operation":-
. Now this M-S Jn behaves almost like a (p-n Jn) or (a p+-n Jn) so there will be a "built-in" potential "Vbi". and becoz of this built in potential → there is going to a depletn layer (here)
. Now, say width of depln layer is 'W'.
→ Now, W can be related to Vbi (by solving poisson's eqn):
So, Vbi = q N W² / 2ε
or
W = √(2εs Vbi / q N)
where, N is the doping conc^n
ε → permittivity
S
G
D
't'
n+
n⁻
n+
depln layer (say)
Semi-Insulating GaAs
"channel"
fig (1.c) → same as fig (1.a)


Refer (1.C) figure (for this page's explantn)
06
• If 't' is the thickness of (n⁻) layer in fig (1.C)
→ Now, if 't' > 'w' → that means, there is still a part of the channel which is "undepleted" & that means if you now apply vtg "VDS" → a current (e⁻s) can flow betn S & D (there is a channel existing for current to flow
Not-fully depleted channel
For this case,
We call it, a "Normally"-ON device or "Depletion-mode" MESFET device
(VT → is -ve)
→ On the other hand, if 't' < 'w' → which means, that depln width 'w' due to built-in potential is much larger than the thickness 't' of the channel, then at Zero bias, the Depletn width is completely going to cover the channel, so there is no way e⁻s (current) can flow betn the 'S' & 'D'.
We this case
We call it, a "Normally"-off device or "Enhancement-mode" device
(VT is +ve)
"Forward bias gate vtg" (apply the gate vtg, so that depln width is just enough to cover channel (t) thickness region)
→ For these device, like MOSFET, we define "Threshold voltage" VT
VT → is that Vgs vtg, such that conduct just begin's
ie Vgs > VT → conduct
Vgs < VT → no conduct.
gate to-source at which depletn width just cover the channel region of thickness (t)



• Related to MESFET, we also define "Pinch-off vtg" V_{po} 07

V_{po} → which is the vtg across the depln region just sufficient to cover the thickness of the channel region 't'.

$$V_{po} = \frac{qNt^2}{2\epsilon}$$

Now, Threshold vtg (V_t) of this device is given by,

$$V_T = V_{bi} - V_{po}$$

↳ ie extra-vtg ie reqd to pinch-off the whole channel.

• For enhancement type device (MESFET), "t<W" →

the doping conc^n 'N' shld be small

$W = \sqrt{\frac{2\epsilon_s V_{bi}}{qN}}$ For same V_{bi}, if 'N' is same, 'W' will be large

(So, either we can make t small or 'W' large by making 'N' small).

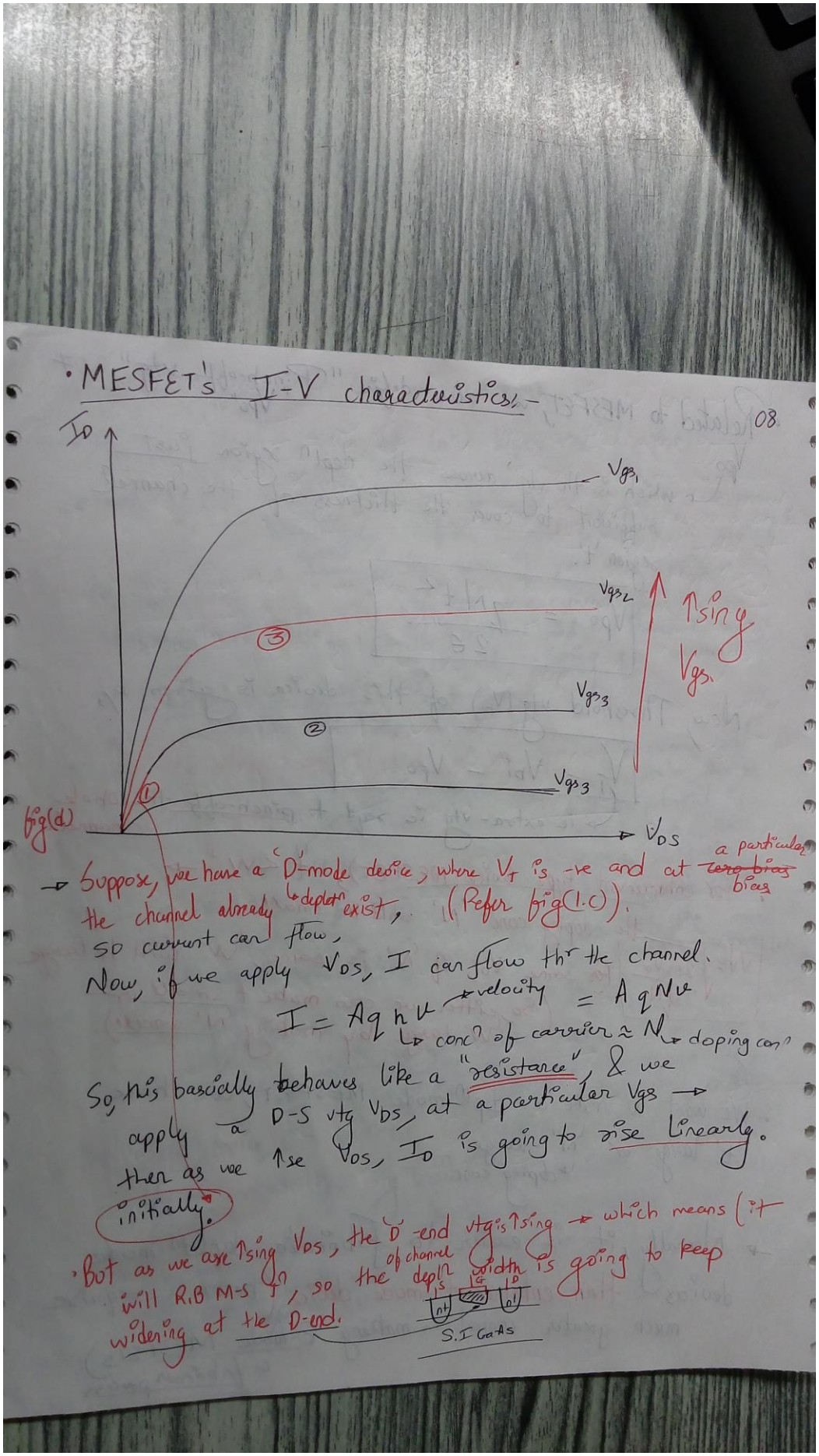
To

• We want to make a depln-mode MESFET, we have

't' large or 'N' large

↳ doping conc^n.

→ Normally, it is easier to fabricate depletn mode devices than enhancement-mode device (becoz v reqd much greater control in making E-mode MESFETs in fabricatn process


• MESFET's I-V characteristics -
08
I_D
V_{gs_1}
V_{gs_2}
V_{gs_3}
V_{gs_3}
↑sing V_{gs}
③
②
①
fig(d)
V_{DS}
→ Suppose, we have a 'D'-mode device, where V_T is -ve and at a particular bias the channel already depletn exist, (Refer fig(1.c)).
So current can flow,
Now, if we apply V_{DS}, I can flow thr the channel.
$I = A q n v$ → velocity $= A q N v$
↳ conc' of carrier ≈ N_d ↳ doping conc'
So, this basically behaves like a "resistance", & we apply a D-S vtg V_{DS}, at a particular V_{gs} → then as we ↑se V_{DS}, I_D is going to rise linearly.
initially.
• But as we are ↑sing V_{DS}, the 'D' end vtg is ↑sing → which means (it will R.B M-S J^n, so the depltn width of channel is going to keep widening at the D-end.
G
S
D
n+
n
S.I GaAs

- Now, since there widening of Depl^n width at 'D' end → it means that $I = AqNv$, cross-sect^al area of current flow reduces. ⟹ (If we must have a constant current flowing thro't the channel)
- → If A reduces, then velocity 'v' has to keep ↑sing (This happen's becoz Electric-field at 'D' end keeps ↑sing)
- But, we know that if we keep on ↑sing the velocity (v) it will reach → saturat^n (Refer pg 1, fig (a)) Note: (E-field is not constant thro'out the channel)
- So, what happens is initially as we keep on ↑sing V_{DS}, becoz of the reduct^n in 'A', current I_D does not rise linearly (but sub-linearly) & finally when velocity of (e's) 'V_d' reaches saturat^n → current 'I_D' also saturates (but slightly ↑se) (Part ② in fig d) → (similar to CLM in MOSFET) (since, here in MESFET also effective channel length reduces)
- → Now, if we take a higher gate vtg, (+ve V_{gs}) current 'I_D' is going to ↑se more becoz (part ③) (for a higher V_{gs} vtg, the depl^n width in the channel is going to be less, ⟹ the initial cross-sect^n of 'A' of current flow is going to be more)
- → Refer fig (d), the Nature of I-V charact^r of MESFET is valid for both Enhancement & depl^n-mode devices. → Quite similar to that of MOSFET

{ eg if we have a D-mode MESFET, it means that the current flow I_D will exist if even when $V_{gs} < 0$. }