The detailed minutes of orientation program are as follows:

Subject: IC Technology

Mod No.	Unit No.	Topics	Remarks	Hrs
1		**Environment and Crystal Growth for VLSI Technology**		8
	1.1	**Environment:** Semiconductor technology trend, Clean rooms, Wafer cleaning	INUP Program website Ref. 1 (By Plummer) Chapter 4 (RCA cleaning)	
	1.2	**Semiconductor Substrate:** Phase diagram and solid solubility, Crystal structure, Crystal defects, Czochralski growth, Bridgman growth of GaAs, Float Zone growth, Wafer Preparation and specifications	Ref. 2 (By S.A.Campbell) Chapter 2	
2		**Fabrication Processes Part 1**		10
	2.1	**Deposition:** Evaporation, Sputtering and Chemical Vapor Deposition	Ref. 2 (By S.K.Gandhi)	
	2.2	**Epitaxy:** Molecular Beam Epitaxy, Vapor Phase Epitaxy, Liquid Phase Epitaxy, Evaluation of epitaxial layers	Ref. 2 (By S.K.Gandhi)	
	2.3	**Silicon Oxidation:** Thermal oxidation process, Kinetics of growth, Properties of Silicon Dioxide, Oxide Quality, high κ and low κ dielectrics	Ref. 4 (By S.M.Sze)	
	2.4	**Diffusion:** Nature of diffusion, Diffusion in a concentration gradient, diffusion equation, impurity behavior, diffusion systems, problems in diffusion, evaluation of diffused layers	Ref. 2 (By S.K.Gandhi)	
	2.5	**Ion Implantation:** Penetration range, ion implantation systems, process considerations, implantation damage and annealing	Ref. 2 (By S.K.Gandhi)	
3		**Fabrication Processes Part 2**		10
	3.1	**Etching:** Wet chemical etching, dry physical etching, dry chemical etching, reactive ion etching, ion beam techniques	Ref. 2 (By S.K.Gandhi)	
	3.2	**Lithography:** Photoreactive materials, Pattern generation and mask making, pattern transfer, Electron beam, Ion beam and X-ray lithography	Ref. 2 (By S.K.Gandhi)	
	3.3	**Device Isolation, Contacts and Metallization:** Junction and oxide isolation, LOCOS, trench isolation, Schottky contacts, Ohmic contacts, Metallization and Packaging	Ref. 2 (By S.A.Campbell)	
	3.4	**CMOS Process Flow:** N well, P-well and Twin tub		
	3.5	Design rules, Layout of MOS based circuits (gates and combinational logic), Buried and Butting Contact	NMOS &CMOS design rules. One question 10 marks in paper.	
4		**Measurements, Packaging and Testing**		10

	4.1	**Semiconductor Measurements:** Conductivity type, Resistivity, Hall Effect Measurements, Drift Mobility, Minority Carrier Lifetime and diffusion length	Ref. 7 (By M.S.Tyagi), Chapter 20	
	4.2	**Packaging:** Integrated circuit packages, Electronics package reliability	Ref. 9 (By G.R.Blackwell) -Chapter 3	
	4.3	**Testing:** Technology trends affecting testing, VLSI testing process and test equipment, test economics and product quality	Ref.10 (By M.L.Bushnell)-Chapter 1, 2, 3	
5		**SOI, GaAs and Bipolar Technologies**		8
	5.1	**SOI Technology:** SOI fabrication using SIMOX, Bonded SOI and Smart Cut, PD SOI and FD SOI Device structure and their features	Ref. 5 (By K. Bernstein) Chapter 2, 2.2, 2.3	
	5.2	**GaAs Technologies:** MESFET Technology, Digital Technologies, MMIC technologies, MODFET and Optoelectronic Devices	Ref. 2 (By S.A.Campbell) Chapter 17	
	5.3	**Silicon Bipolar Technologies:** Second order effects in bipolar transistor, Performance of BJT, Bipolar processes and BiCMOS	Ref. 2 (By S.A.Campbell) Chapter 18	
6		**Novel Devices**		6
	6.1	**Multigate Device:** Various multigate device configurations (device structure and important features)	Ref. 6 (By Jean P. Colinge) Chapter 1	
	6.2	**Nanowire:** Fabrication and applications	Ref. 8 (By James E. Morris) Chapter 15	
	6.3	**Graphene Device:** Carbon nanotube transistor fabrication, CNT applications	Ref. 8(By James E. Morris) Chapter 10, 12, 16	

Suggestions:

1. The theory paper should comprise of 80% theory questions, 10% questions on layout and rest 10% on numerical.
2. Numerical should be asked from the following modules only- 1.2, 2.3, 2.4, 4.1
3. In the modules 5 & 6, related to technologies and novel devices, the discussion should be confined to structure, advantages, disadvantages and applications of devices.
4. The List of experiments and the related soft wares proposed by the experts are attached herewith.